Advanced Engineering Forum *Online: 2012-09-26*
ISSN: 2234-991X, Vols. 6-7, pp 542-546
doi:10.4028/www.scientific.net/AEF.6-7.542

Embedded Real-Time Image Processing System Based on DM6446 + FPGA Architecture

Zhang Baofeng[a], Yang Yi[b], Zhu Junchao[c], Li Cui[d]

Tianjin Key Laboratory for Control Theory & Applications in Complicated Systems, Tianjin University of Technology, Tianjin, China

[a]zhangbaofeng@263.net,[b]abcd19852002@yahoo.com.cn,[c]zhujunchao@sina.com, [d]cekonglicui@163.com

Keywords: real-time image processing; embedded; real-time; DaVinci technology; image preprocessing

Abstract. To solve the traditional image processing system problem such as large in size, high power consumption and poor real-time, an embedded real-time image processing system is designed based on TMS320DM6446+FPGA architecture. DM6446 as the core of the system is responsible for the scheduling, image processing algorithms, image output; field programmable gate array (FPGA) is responsible for capturing real-time image data, image preprocessing. The paper describes the principle of the real-time image processing system. The experiment proved that the system can achieve real-time acquisition, processing and output of image data in 20 frames per second.

Introduction

With the rapid development of image processing technology, continuously improve the performance requirements of image processing systems, especially real-time performance [1]. For real-time processing of large number of image data, the system needs high computing speed and large memory. The vast majority of the image processing systems are based on a traditional PC or multi-CPU architecture [2], but this type of image processing system in terms of resource allocation and volume are redundant and bloated and inflexible, high power consumption, is not suitable for the portable platform [3]. Embedded systems as a high level of integration and application platform of hardware and software can be cut, with a practical, low cost, small size, easy to expand, low power consumption [4]. In high-speed image processing, DSP (digital signal processor) Can provide support of the complex structure of the algorithm processing [2]; image pre-processing large volumes of data requiring high processing speed, but the algorithm is relatively simple and suitable for the use of FPGA hardware implementation [5]. DaVinci chip, high-performance digital signal processing system on a chip, is designed for image processing. Its dual-core architecture (ARM+DSP) can be qualified for a complex system administration tasks, but also to meet the needs of real-time complex algorithms [6]. This paper draw on the respective advantages of the DSP and FPGA in image processing, and describes an embedded real-time image processing system, in order to solve the problem of real-time image processing and low power.

The DM6446 is a typical and widely used DaVinci chip, the main function modules of the system circuit design is based on this chip. Taking into account the convenience of expansion, according to the different functions in the system and taking into account the type of signal frequency, the system is designed into four separate functional modules; image processing and control module, image acquisition and pre-processing module, power module, and the corresponding interface extension. Image processing and control module is based on the DM6446 chip as the core of complex algorithms for image processing, scheduling control and output functions, signal processing frequencies up to 810 MHz [7]; power supply module for the entire system to provide 3.3V, 1.8V 1.2V supply voltage; image acquisition and pre-processing module to complete high-precision acquisition and preprocessing functions for image data. Fig. 1 shows the system block diagram which is composed of the image processing and control module, power module, and image acquisition and pre-processing module .

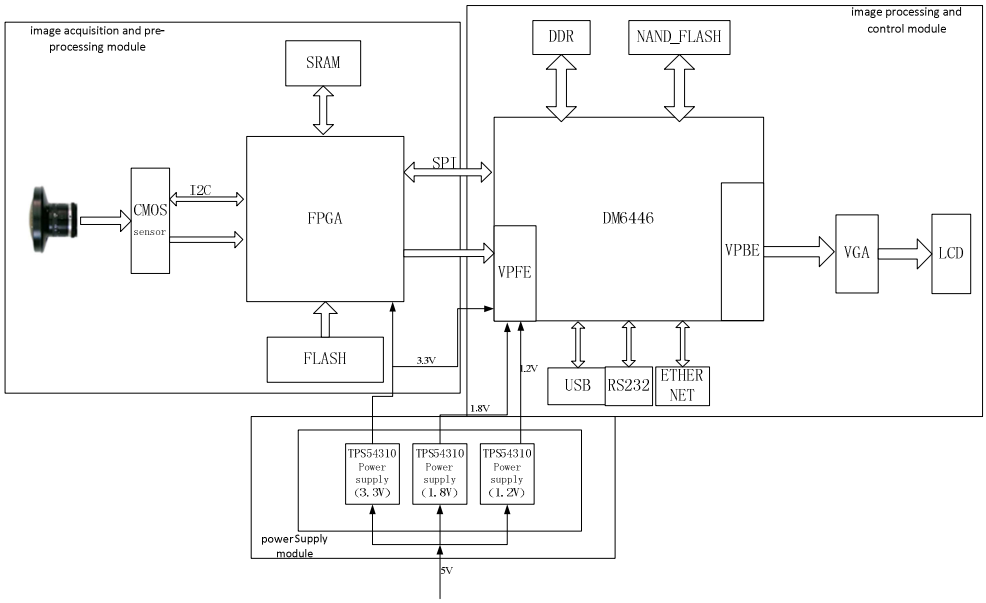

Fig. 1 Functional block diagram of hardware system architecture

On the system power-up initialization, the image data is real-time acquired under the control of the FPGA, and then use its internal hardware resources to achieve the image color space conversion, image enhancement, distortion correction, image pre-processing algorithm; then use the DM6446 high-speed signal processing capabilities to achieve advanced image processing algorithms; Finally, the image processing results are displayed to the LCD through the VGA standard interface.

System Module Unit Design

Image Acquisition and Pre-processing Module. As shown in Fig. 2, the core of image acquisition and pre-processing module is FPGA chip EP2C5Q. The module's function is to control the CMOS image sensor to complete the image data in real-time acquisition, preprocessing, and data exchange functions, under the DM6446 scheduling. CMOS image sensor chip is MT9T001 [8], it through the FPGA built-in I2C interface and image acquisition unit connected to achieve a high precision real-time image data acquisition and control.

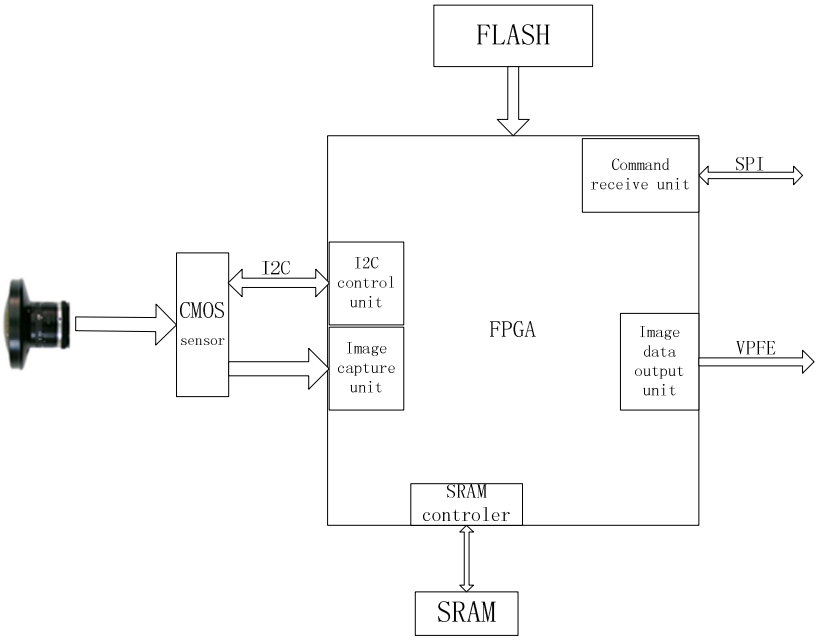

Fig. 2 Functional block diagram of the image acquisition and pre-processing module

The raw image data are preprocessed through FPGA, such as color space conversion and image enhancement. A large number of simple image pre-processing algorithm is achieved through pure hardware, on the one hand alleviate the DM6446 algorithms pressure, on the other hand to improve the efficiency of the system. In addition, after an image pre-processing is completed, the FPGA send a interrupt notification to DM6446 and then enter the handler program. The advanced algorithm is implemented in the DSP program, and then notifies the FPGA to capture the next frame. The method of frame interrupt solves the problem of real-time image signal acquisition in high-speed. DM6446 can handle previous frame image data during the period of image acquisition. This way improve the parallel system processing, and gain more time to implement image processing algorithms.

Image Processing and Control Module. DM6446 chip, program memory and data memory, three chips are the core of the module, as shown in Fig. 3.

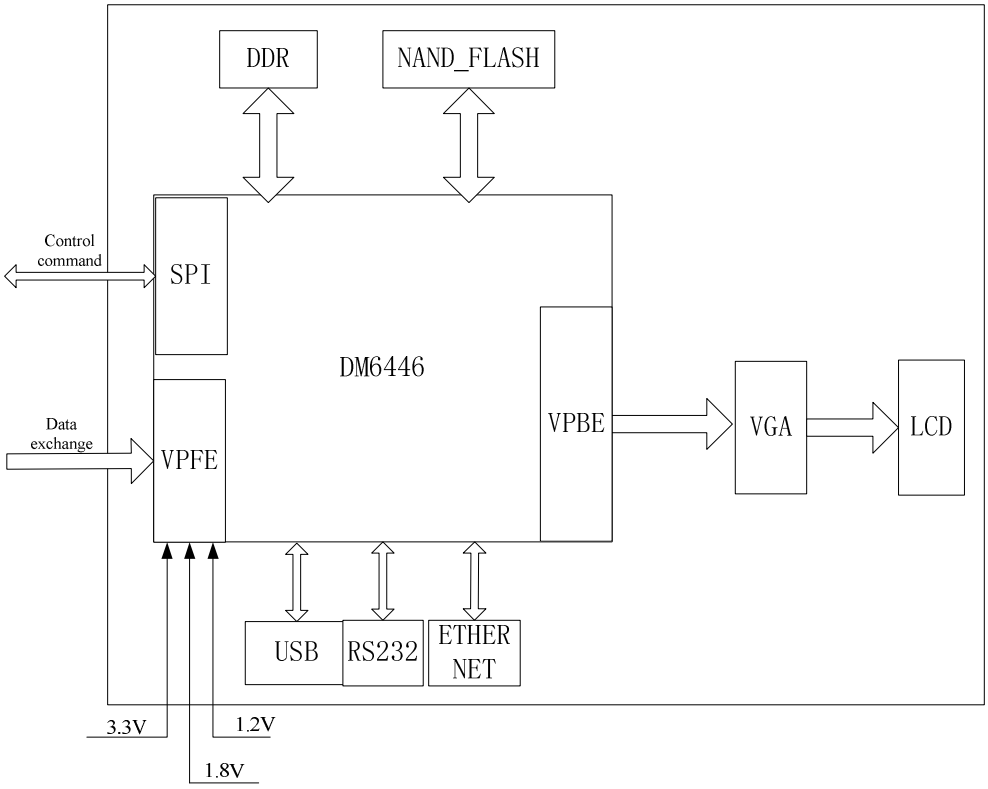

Fig. 3 Functional block diagram of image processing and control module

This module is responsible for advanced image processing algorithm, the system scheduling and output, through the JTAG interface circuit emulator is connected to a computer host, and data communications. DM6446 program is stored in the NAND FLASH. On the system power-up initialization, the module is initialized through the SPI interface under control of DM6446 and completes the configuration of CMOS image sensor. Real-time image data obtained by VPFE (video processing front end) is sent into the DM6446 [9], and then buffered into the DDR memory under the scheduling of the EDMA [10].The image data after post-processing by VPBE (video processing back-end) extended VGA standard interface output.

Memory Unit. The image storage unit, composed of 2 capacities of 64M x 16 bit MT47H64M16HR type DDR2 SDRAM, are used to intermediate data storage areas in image processing. It has a large capacity, small size, speed and low price advantage, the highest clock frequency up to 333MHz, the single - chip capacity of up to 1Gbit. However, the physical storage structure difference of the DDR2 SDRAM and SRAM, DDR2 SDRAM timing control is more complex. The current general general-purpose microprocessor does not have a DDR2 SDRAM

interface, limiting the DDR2 SDRAM widely used [11]. However, the DM6446 chip integrates a 32-bandwidth DDR2 controller, can be seamlessly connected to the DDR2 SDRAM, and become very convenient [6].

Interface Design. The DM6446 need communicate with other devices in system debugging and image processing. The communications module includes RS232 asynchronous communications ports, RJ45 Ethernet interface, and USB interface. Among them, MAX3221 RS232 interface chip, with ± 15kV ESD protection circuitry, the chip meets TIA/EIA-232-F electrical standards, can provide up to 250Kbit/s communication speed. In addition, the MAX3221 can work properly between 3V-5.5V power supply voltages. And the same time, DM6446 integrated EMAC controller, an external Ethernet chip BCM5221KPT [11], can be achieved by RJ45 10/100M Ethernet interface. The same time, the DM6446 chip integrated USB controller, you can easily expand the USB interface, the peripheral extension [12] reserved for the system.

Power Supply Module. The power supply module core is TI's three power chip TPS54310 [4], it provides 3.3V power supply voltage for image acquisition and pre-processing module, and image processing and control, provide a 1.2V core voltage for image processing and control module and 1.8V for chip I/O port [7]. The chip takes into account the DM6446 chip's high power consumption and large current. So it can work with 3A current output continuous and ensure the DM6446 chip and the entire system on the current requirements. To ensure the stability of the output voltage of the power supply module, power chip can automatically detect the voltage output status of the PWRGD pin, monitor the output voltage of the chip, and complete brown-out reset of the system and output voltage monitoring function.

Experiment Results and Analysis

The real-time image processing hardware system platform is shown in Fig. 4. Fisheye lens used in the experiment, the system real-time image acquisition resolution of 720 x 576, 25 frames per second PAL standard fisheye image. Calibrated fish-eye images are real-time output to the LCD display shown in Fig. 5. The experimental results show that the system can capture fisheye image in real time and continuously, and then processing image data and output result in 20 frames per second. The system can be stable in real-time image acquisition and processing.

Fig.4 Hardware platform

Fig.5 Experiment results

Conclusion

In this paper, to solve the traditional image processing system problem such as large in size, high power consumption and poor real-time, an embedded real-time image processing system is designed based on TMS320DM6446+FPGA architecture. The system makes full use of the DM6446 dual-core architecture (ARM+DSP) can be qualified for a complex system administration tasks, and also to meet the characteristics of real-time image processing algorithms; FPGA high-speed and flexibility to ensure the system real-time, simplify the peripheral circuit. The experiment proved that the system for image data acquisition, processing and output to 20 frames per second speed. And the same time, the system laid a foundation for the later complex image algorithms transplantation.

This work was supported by a grant from the National Natural Science Foundation of China （ No. 61172185）and Xinjiang Uygur Autonomous Region Science and Technology Project (The introduction and promotion of the dried fruit color sorting technology and key equipment, No. 201154124).

References

[1] Mohamed Akil, Laurent Perroton: Special issue on parallel computing for real-time image processing. Real-Time Image Proc,2011,(6):1–2.
[2] A. Bensrhair, N. Chafiqui and P. Michel: Implementation of a 3D vision system on DSP4 TMS320C31. Real-Time Imaging,2010,(6) 213-221.
[3] Shiuh-Jer Huang,ian-Cheng Huang: Vision guided dual arms robotic system with DSP and FPGA integrated system structure. Journal of Mechanical Science and Technology. 2011, 25 (8) 2067~2076.
[4] LI Yanbin: On-board embedded landmark tracking system based on Omni-directional vision. Tianjin: Tianjin University，2009.
[5] WANG Zhigang, SHI Yibin: Design of Data Acquisition Module Based on DSP+FPGA Architecture. Chinese Journal of Scientific Instrument,2003,(8):80-81.
[6] DaVinci Technology-Digital Video Innovation Product Bulletin(Rev.D).USA: Texas Instruments Incorporated,2007.
[7] TMS320DM6446 Digital Media System-on-Chip.USA: Texas Instruments Incorporated，2008.
[8] TONG Weifeng: Design of The Embedded Video Acquisition System Based On DSP and FPGA. Xi’an: Xidian University，2009.
[9] TMS320DM644x DMSoC Video Processing Front End (VPFE) User's Guide.USA: Texas Instruments Incorporated，2009.
[10] TMS320DM644x DMSoC Enhanced Direct Memory Access (EDMA) Controller User's Guide .USA: Texas Instruments Incorporated，2009.
[11] FU Xing. Multifunction multimedia processing platform research and development based on DM642 .Tianjin: Tianjin University，2006.
[12] TMS32ODM644xDMSoC ARM Subsystem Reference Guide.USA: Texas instruments Incorporated，2009