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Design and Implementation of the HD Video Signal Converter Based on FPGA

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Abstract. In this paper, based on the FPGA and with a video dedicated A / D converter chip, LVDS coding chip, the design and implementation of a SD(standard-definition) analog video signals to HD(high-definition) digital video signal converter. First, input SD analog video into digital video signals meet the ITU-BT656 standard. Then use the FPGA with the video processing chip and DDR do some corresponding processing to achieve high-definition digital video output. After the actual test, the converter output signal of the image quality is well, meets the design requirements, and to verify the effectiveness of the program.

Introduction

With the increasingly and wide range applications of high-definition video, a large number of high-definition video equipment have emerged, accompanied DVI, HDMI, HD-SDI, LVDS and other emerging high-definition video interface. The market still has a lot of standard definition video capture equipment, such as PAL and NTSC format CCD camera. but new products of the video display devices are more of a digital high-definition input-based,such as LCD and LED monitor. How to make high-definition digital display device to match the analog standard definition video capture equipment and interconnection between a variety of interfaces, has become a problem of the modern video applications. This paper against the problem of not compatible in analog standard definition video capture equipments and digital high-definition video display devices, in industrial detecting field, so that achieve the standard definition analog video in real time and high-quality serial transmission, and display image clearly in digital high-definition monitor.

System Design

According to the needs of practical application, the hardware block diagram design of the digital video signal converter is shown in Figure 1. It can be seen from the figure that the system mainly composed of the system by the video A/D converter module, the video signal processing modules and video serial output modules. The A/D converter module is optional video decoder chip SAA7113H which produced by PHILIPS Corporation, mainly used to input the external CVBS composite video signal decoding into the 8Bit digital YUV video signal which meet the ITU-BT656 standard. Video signal processing module, optional high-performance, low-cost Cyclone series FPGA chip EP1C3T100I7 which produced by Altera Corporation. It's mainly function is to complete the preparation register configuration of SAA7113H and WSC2810, in order to achieve resolution zoom, video frame rate conversion and de-interlacing of video images and other image processing functions. The other function is give output timing to LVDS encoder, so that the video signal can display in monitor via the LVDS to DVI adapter. The video output module is selected NXP LVDS encoder chip DS90C385 which produced by NXP Corporation, it's used to enter the parallel video data into LVDS high-speed serial signal[1].

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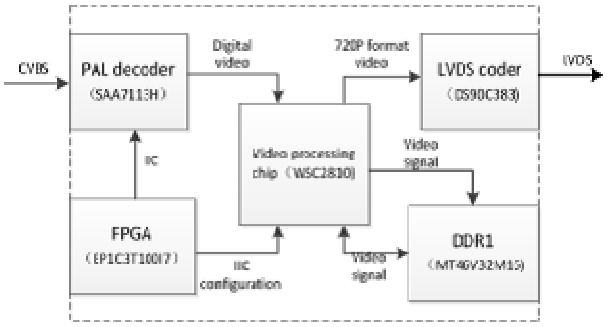


Fig. 1 System block diagram

A/D converter module design. This module‘s core is the chip SAA7113H which produced by PHILIPS Corporation. There are 4 ways of analog video signals input of the SAA7111A which can be 4 ways CVBS or 2 ways S-Video (Y/C). It can be composed one or two in 4 video inputs of different modes of operation, achieved automatic monitoring and signal separation of horizontal and vertical sync. What's more, the start and end position of the horizontal sync signal can be controlled by programming, output is 8 bits VPO bus, supported different output format of different bit-wide data[2]. The main features are as follows:

- Automatic detection of 50Hz/60Hz vertical frequency, convert NTSC and PAL automatically, enable processing the brightness and chromaticity of the input video signals.
- With 4-way composite videos (CVBS) or 2-way S-Video (Y/C) analogy input.
- Brightness, contrast, aperture and saturation control.
- Supports 8 Bit YUV4:2:2 (ITU-BT656), output formats.

Design of the control module. According calculation of RAM resources and I / O pins needed in the design, the system control chip selected Altera Corporation high performance Cyclone II series FPGA chip EP1C3T100I7. This chip has the features of high-speed, small size and and it also be the best choice for low-cost and low-power consumption. The mainly features are as follows:

- 2910 logic elements (LEs);
- 1.5V core voltage , 3.3V port voltage which also compatible with 2.5V;
- One phase-locked loop (PLL), and up to 16 global clock networks;
- Support of AS, PS and JTAG multiple configuration modes which provides users with flexible configuration;
- Support of LVDS, LVPECL, HSTL I/O and other differential signal standards.

Design of video processing module. According to the design requirements, system needs to converts the PAL analog video signal by resolution of 720×576, 25 frames per second (50 fields per second), and interlaced scan into the 720P format signal by resolution of 1280×720, 60 frames per second and progressive scan video, this will require the corresponding video image algorithm processing to complete the conversion of video formats. At the same time, there is different from the normal static image processing, but also to ensure smooth video display output and real-time requirements during the dynamic video image processing. For this, the design uses the Fujitsu WSC2810 dedicated video processing chip with the external DDR to complete the video algorithms processing. The WSC2810 have the following characteristics:

- Automatically detect and switch the input video format;
- Support up to 165M pixel clock input;
- resolution and frame rate transform function;
- Conversion between interlaced and progressive scan mode (based on the improvement of motion compensated de-interlacing algorithm);
- Containing the OSD signal generator.

Design of LVDS coding module. National Semiconductor's LVDS encoder chip DS90C385 is selected as the coding module. This chip is a powerful serialization sending chip, which can made up to 24 bit parallel video data converted to serial differential LVDS interface standard signals output. DS90C385 supports 20MHz-85MHz pixel clock, the transmission amount of data can be up to 2.38 Gbps, which is complied with the TIA/EIA-644 LVDS standard[2]. Because of its strong anti-interference ability and long transmission distance, it's widely used in industrial, communications, military and other fields. It must be noted that, according to VESA standard, the DE stay to high level only when data needs to be transmitted, when there is no data transmission, DE must stays to low level, which can make video signal normally display. DE signal needs to be connected to the FPGA user I / O, according to the needed of video output through the FPGA gives the corresponding DE timing.

Implementation of video Format Transform

I2C bus control[3]. FPGA and SAA7713H or WSC2810 for data transfer on the SDA bus, the SCL bus clock synchronization. Each bit is sampled during the SCL is high level while data transmission, thus the data bus SDA must remain stable during the SCL is high level. The change can only occur during SCL is low, once the shift in high and low status of SDA bus during the SCL is high. means that the master issued start or stop signal.

When the FPGA data transfer request is not sent to the I2C bus, the bus is idle, clock bus SCL and the data bus SDA are high at tis time, if the FPGA start trying to control the I2C bus data transfer, the first to issue a start signal. The start signal is defined as: the data bus SDA changes from high to low, when clock bus SCL is high. Also device by sending a stop signal to abort the data transfer, the stop signal is defined as: clock bus SCL is high, the data bus SDA changes from low to high. As shown in Figure 2.

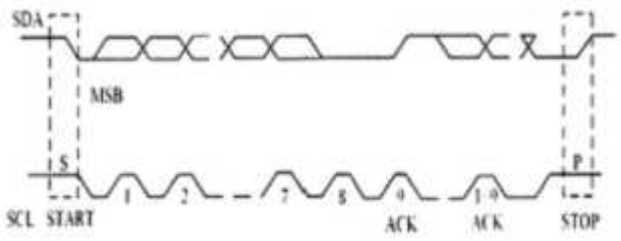


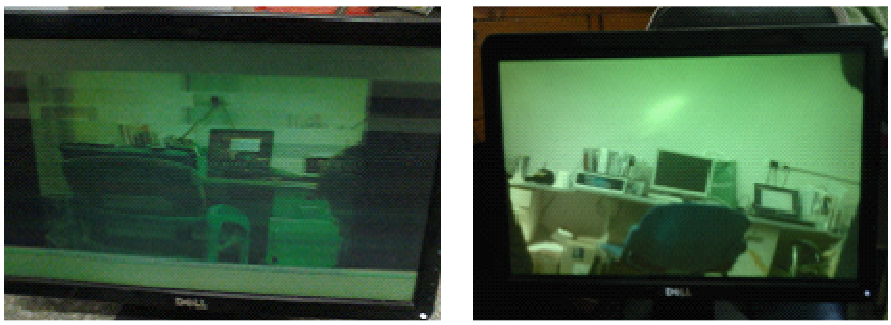
Fig. 2 IIC data transfer timing diagram

A / D Converter. In this design, optional video analog to digital converter and PAL decoding module is a dedicated video decoder chip SAA7113H. SAA7113H also has functions of video decoder and video analog to digital conversion. Convert external input CVBS or YC analog video signal to digital video signal, and output 8Bit YUV digital video signal conformed ITU-BT656 standard, it embedded SAV, EAV, instead of a separate horizontal sync, vertical sync and sampling clock. The chip provides the I2C bus interface, and the FPGA configure the internal register of SAA7113H through the I2C bus[4]. So that initializing the chip's configuration, implement the functions of the analog input, the color space model, the fixed gain, horizontal sync, vertical sync, brightness, contrast, and so on.

Processing of De-interlacing. Scan of the PAL format is interlaced, totally 50 Hz, 25 frames per second. However, some video display terminals are all progressive scan video, such as LCD, plasma display and so on, So it must to be de-interlaced. The traditional method of deinterlace operation as follows: written the odd field of a frame image to the external RAM1, then the even field of this frame also written to RAM1. After such operation in the RAM1, the odd field and the even field interpolation together to a complete frame. Then read out the image line by line from the RAM1, at the same time, written the next frame's odd and even field to another RAM2. So that RAM1 and RAM2 worked in reading and writing state respectively, via this ping-pong operation like this, interlaced to progressive scan conversion can be completed[5].

After the experiment, this method can be interlaced to progressive changes in, but when shooting moving images, the image edge exists jagged, the image quality is poor.

But the WSC2810's deinterlacing device, embedded algorithms for motion estimation compensation, capture motion image very smooth, the image quality is very good. Shaking the camera, the image is shown as Figure 3. The (a) is image with using traditional de-interlacing method, (b) is image with using WSC2810's embedded deinterlacing algorithm for motion picture.



(a) (b)

Fig. 3 The comparison chart of de-interlacing

Frame rate conversion. The PAL input video signal of camera is 25 frames per second after the previous conversion of interlaced scan to progressive scan. This article used the simplest way to duplicate frame to achieve the conversion from 25 frames per second into 60 frames per second. The system uses the most simple way to copy the frames from 25Hz to 60Hz conversion. As mentioned above, while the PAL digital video signal into the FIFO, and then a higher frequency to read out the video frame which stored in the FIFO[6]. The frame rate ratio of 5:12, repeat read out some of the frames, until the equivalent of every deposited 5 should read out 12. That can complete the frame rate conversion.

Resolution conversion. According to requirements of the design, it needs to transform the resolution from 720×576 to 1280×720. It needs for the expansion of the resolution. The resolution to expand of WSC2810 via changing the horizontal frequency, the vertical frequency, and the pixel clock by configuring the appropriate registers so that to change the output video format. Inside the chip, by calculating the horizontal frequency, the vertical frequency and the pixel clock can automatically draw the size of the required resolution. For example, according to the EIA-CEA-861-D[7], it's set to output 720P format video, the horizontal frequency is 45KHz, the vertical frequency is 60Hz, the pixel clock is 74.25MHz. Then:

$$\text{the number of scan lines: } 45000 \div 60 = 750$$

$$\text{The number of pixels of each line: } 74250000 \div 45000 = 1650$$

750 of the above formula is the actual number of scan lines and 1650 is the numbers of pixels per line scan, remove the blanking pixels and so on, the real effective display 720 lines of 1280 pixels per line. Is the standard 720P video resolution.

System testing and analysis

After debugging the hardware circuit and simulating the software modules. In order to observe the display effect, the LVDS-DVI video switch box provided by Hunan Jingjia-micro Company is chosen in this experiment. The video signals from LVDS are transformed into digital video signal and displayed by monitor with DVI interface. After configure the various registers in the SAA7113H, the results shown that each pixel-clock of the digital video signal, horizontal frequency and vertical frequency, which all meet the design requirements. Figure 4 shows the development of the hardware circuit and experimental results. The left figure is the video signal interface hardware board, and the right is the actual display after debugging.

(a) (b)

Fig. 4 Est platform and experimental results

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