Defect and Diffusion Forum
ISSN: 1662-9507, Vol. 425, pp 63-68
doi:10.4028/p-72252k

Submitted: 2022-09-02
Revised: 2022-11-15
Accepted: 2022-11-25
Online: 2023-05-31

Study of Defects in 4H-SiC Epitaxy at Various Buffer Layer Growth Conditions

Tawhid Rana[1,a], Jun Wu[1,b], Gil Chung[1,c], Kevin Moeggenborg[1,d], Matthew Gave[1,e]

[1]SK siltron css, 1311 Straits Drive, Bay City, MI 48706, USA

[a]tawhid.rana@sksiltron.com, [b]jim.wu@sksiltron.com, [c]gil.chung@sksiltron.com, [d]kevin.moeggenborg@sksiltron.com, [e]matthew.gave@sksiltron.com

Keywords: Silicon carbide epitaxy, buffer layer optimization, ramped buffer layer, buffer layer growth rate

Abstract: Buffer layer optimization is a critical technique to mitigate defect propagation from substrate to epilayer, reduce stress, and prevent generation of ingrown defects. In the present study, the impact of dopant transition from substrate to the buffer layer on various epilayer defects was investigated. It was found that a ramped transition of the dopant concentration from substrate to buffer layer is beneficial for reduction of basal plane dislocations in the epilayer compared to an abrupt doping transition. This reduction of defects can be attributed to reduced stress at the substrate-to-buffer layer transition. Tests on buffer layer growth rates also revealed that higher growth rates reduce BPDs (basal plane dislocations) in the epilayers. We believe that BPD conversion in epilayers grown at higher growth rates is energetically more favorable than the conversion at slower growth rates resulting in the observed reduced BPDs at higher growth rates.

Introduction

Buffer layer optimization is a critical technique to mitigate defect propagation from substrate to epilayer and prevent generation of stress induced defects. Various methods have been described to improve the crystal quality of the epilayers. It has been demonstrated that slower growth rates and ramped nitrogen flow during buffer layer growth are beneficial to reduce BPD propagation into the epilayer [1]. BPD reduction was also demonstrated by recombination enhancing buffer layers [2-3]. Reduced temperature was also found to be beneficial for BPD reduction [4]. The doping profile between the substrate-to-buffer layer can impact BPD propagation and conversion in the epilayers [5]. Thicker buffer layers are also beneficial to reduce carrot defects in the epilayer [6]. In the present work, we investigate a ramped transition of substrate to buffer layer doping and its impact on defects in the epilayers.

Prior to buffer layer deposition, surface etching of the substrate was performed. Even though the substrate surface was polished, residual subsurface damage can remain [7] (Fig.1, A-B). Ideally, steps on the surface need to be cleanly delineated prior to epitaxy and surface damage needs to be removed by etching [8-9].

The composition of the buffer layer and its optimization can be dissected into three main parts:

i) Substrate-to-buffer layer doping transition (Fig.1, B-C): The doping concentration of commercially available substrates is ~1e19 cm^{-3} whereas typical buffer layer doping concentrations are ~1e18cm^{-3}. Hence, the delta between the substrate and buffer layer doping is about 9e18 cm^{-3}. The large change in doping concentration results in a misfit between crystal layers and induces high stress per unit length if the transition is too abrupt. This high stress condition can be reduced by introducing a ramped substrate to buffer layer doping transition.

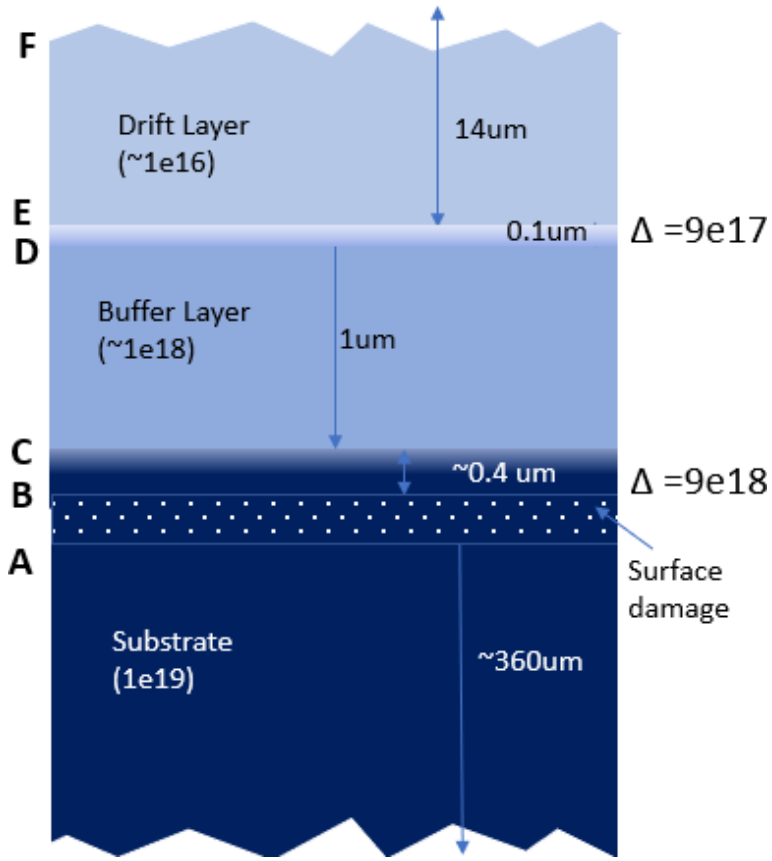

Fig. 1: Cross section diagram of substrate-epilayer. Layer A-B denotes the surface damage layer on the wafer substrate. B-C is the region of steep doping change between the substrate and buffer layer. C-D is the buffer layer. D-E is the doping transition between the buffer and drift layers. E-F is the drift layer.

ii) Buffer layer (Fig.1, C-D): For SiC epitaxy, a buffer layer with a doping target of ~1e18cm^{-3} is typically chosen. Whether defects in the substrate will propagate into the epilayer is dependent on buffer layer thickness, C/Si ratio, growth rate, and other factors.

iii) Buffer layer-to-drift layer doping transition (Fig. 1, D-E): A typical doping concentration of the drift layer (E-F) is ~1e16 cm^{-3} for the commercial applications. Therefore, there will be a ~1e18 cm^{-3} to 1e16 cm^{-3} transition taking place at D-E. The doping concentration difference between these two layers (D-E) is approximately an order of magnitude lower than that of at B-C. Accordingly, the stress impact of the D-E transition is expected to be less severe than the B-C transition

In the present work, studies focused mainly on the substrate to buffer layer doping transition Fig. 1 (B-C) and its impact on epilayer defects. Experiments on buffer layer growth rate and its impact on defect density in the epilayer were also conducted.

Experimental

A commercial epitaxial reactor was used for all tests. Wafers were selected from the same boule to minimize substrate-to-substrate dependency in the results. Growth conditions were similar to those described previously except where noted [10]. Temperature, pressure, and carbon-to-silicon ratio were fixed for all runs. For each test, the substrate was first etched in the reactor in hydrogen ambient at a temperature of 1550 °C prior to buffer layer growth.

Preliminary tests focused on the impact of the layer B-C shown in Fig. 1, which we consider of high importance to mitigate defects in the epilayer. Fig. 2a shows the SIMS doping profile of a buffer layer grown with a sharp increase of nitrogen flow corresponding to the solid line in Fig. 2b. In this case, Experiment 1, nitrogen flow was introduced (AB in Fig. 2b), to achieve a doping target of ~1e18 cm^{-3}. This flow was continued for a time calculated to give a buffer layer thickness of 1 um.

A second test, Experiment 2, used an initial condition with a higher nitrogen flow (A'B' in Fig. 2b) to target a doping of ~7e18 cm^{-3} and this flow was ramped down to achieve a final target of ~1e18cm^{-3} (e.g., dotted line in Fig.2a). The ramp-down time was varied from 1 minute in Experiment 2 to 4 minutes in Experiment 3 by varying B-D in Fig.2b to study the effect.

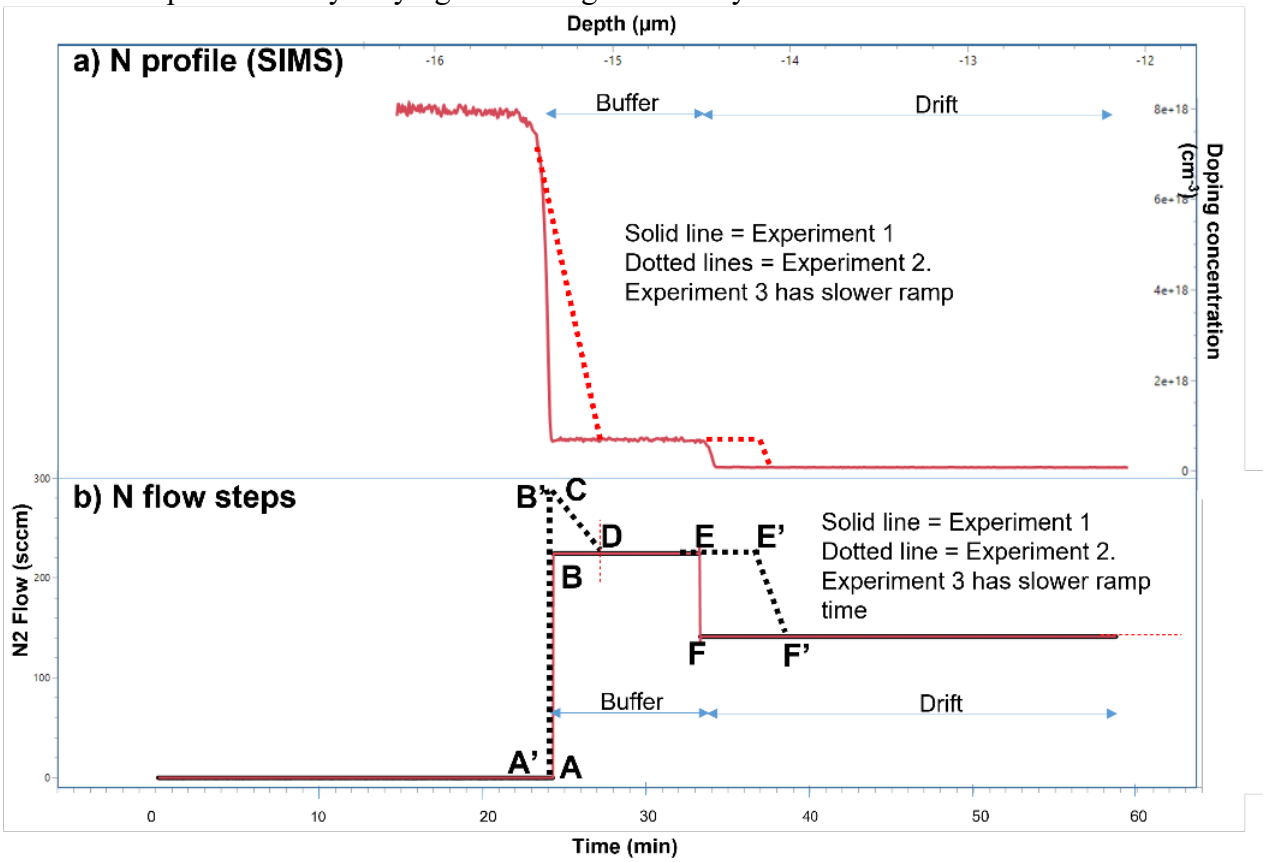

Fig. 2: a) Nitrogen flow steps and corresponding SIMS profile of the buffer layer are shown in solid lines for Experiment 1. Dotted lines show the slower ramp transition concept. b) Nitrogen flow steps are shown for the substrate-to-buffer layer transition. The solid line represents nitrogen flow for the abrupt change of substrate-to-buffer layer doping. Dotted lines show the flow steps for the ramped buffer layer doping transition.

The impacts of the buffer layer growth rate on epilayer defects were also studied. To change the growth rate, the flow of the Si source was varied while keeping the C/Si ratio constant. Finally various defects (Fig. 3) in epilayers were compared for different conditions. Epilayers grown under various substrate-to-buffer layer doping ramp, and growth rate conditions were analyzed using photoluminescence (PL) imaging techniques on a SICA88 by LASERTEC. Kelvin probe microscopy (Semilab, CnCV) was used to study the surface voltage potential and leakage for these epilayers [11].

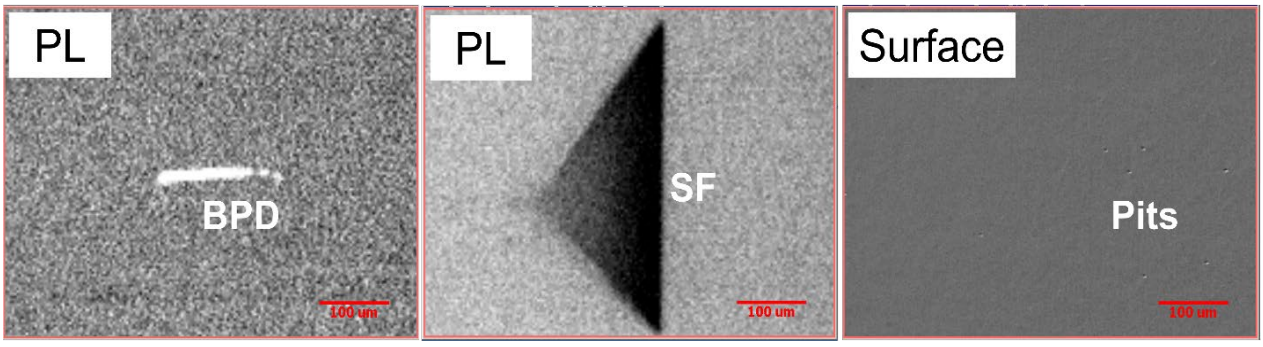

Fig. 3: Basal plane dislocation (BPD), Stacking Faults (SF) and pits in SiC epitaxy

Discussion

Preliminary experiments focused on the impact of the substrate-to-buffer transition step B-C in Fig.1. In Experiment 1, nitrogen flow was initiated instantaneously in the reactor at the beginning of epitaxial growth at a flow rate that gave a buffer layer doping of ~1e18 cm^{-3}. This abrupt change of doping concentration from ~1e19 cm^{-3} in the substrate to 1e18 cm^{-3} in the buffer layer generates high misfit related stress at the substrate-to-buffer layer interface. To mitigate this misfit related stress, Experiment 2 began with nitrogen flow at a higher rate to target ~7e18 cm^{-3} doping and gradually reduced the flow to achieve a final buffer layer doping of 1e18 cm^{-3} in 1 minute. Finally, Experiment 3 duplicated Experiment 2 except that the nitrogen flow was reduced over a 4-minute period. The buffer layer thickness was the same for all 3 experiments.

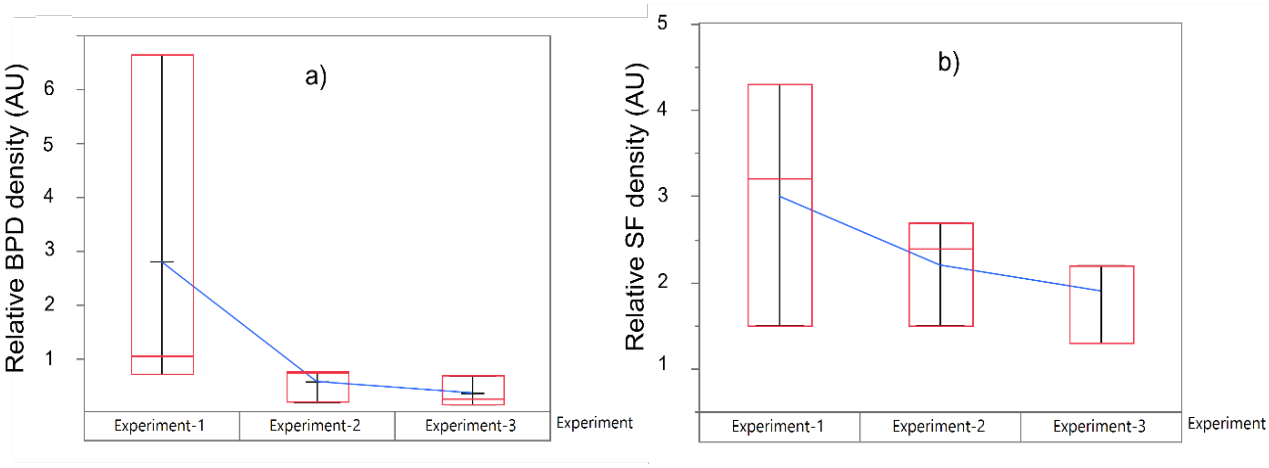

Fig. 4: a) Basal Plane Dislocation (BPD) and b) stacking fault (SF)density at various buffer layer ramp conditions

Results, in Fig.4a, show higher basal plane dislocation (BPD) density for the abrupt transition of doping from substrate-to-buffer layer in Experiment 1. BPD density reduces when substrate-to-buffer layer doping was reduced gradually over 1 minute period. Further BPD reduction was observed when this ramp-down time was increased to 4 minutes. Similarly, in Fig. 4b, reduction of stacking faults at the slower ramp conditions were also observed. While the reason for this improvement requires further detailed study, we attribute the defect reduction to the relaxation of stress due to the graded transition of substrate-to-buffer layer doping. No degradation in defects were seen for the epilayers grown using ramped condition and hence we find this method to be preferable over the abrupt buffer layer condition. However, it needs to be considered that adding ramped condition with longer ramped time impacts overall throughput of production.

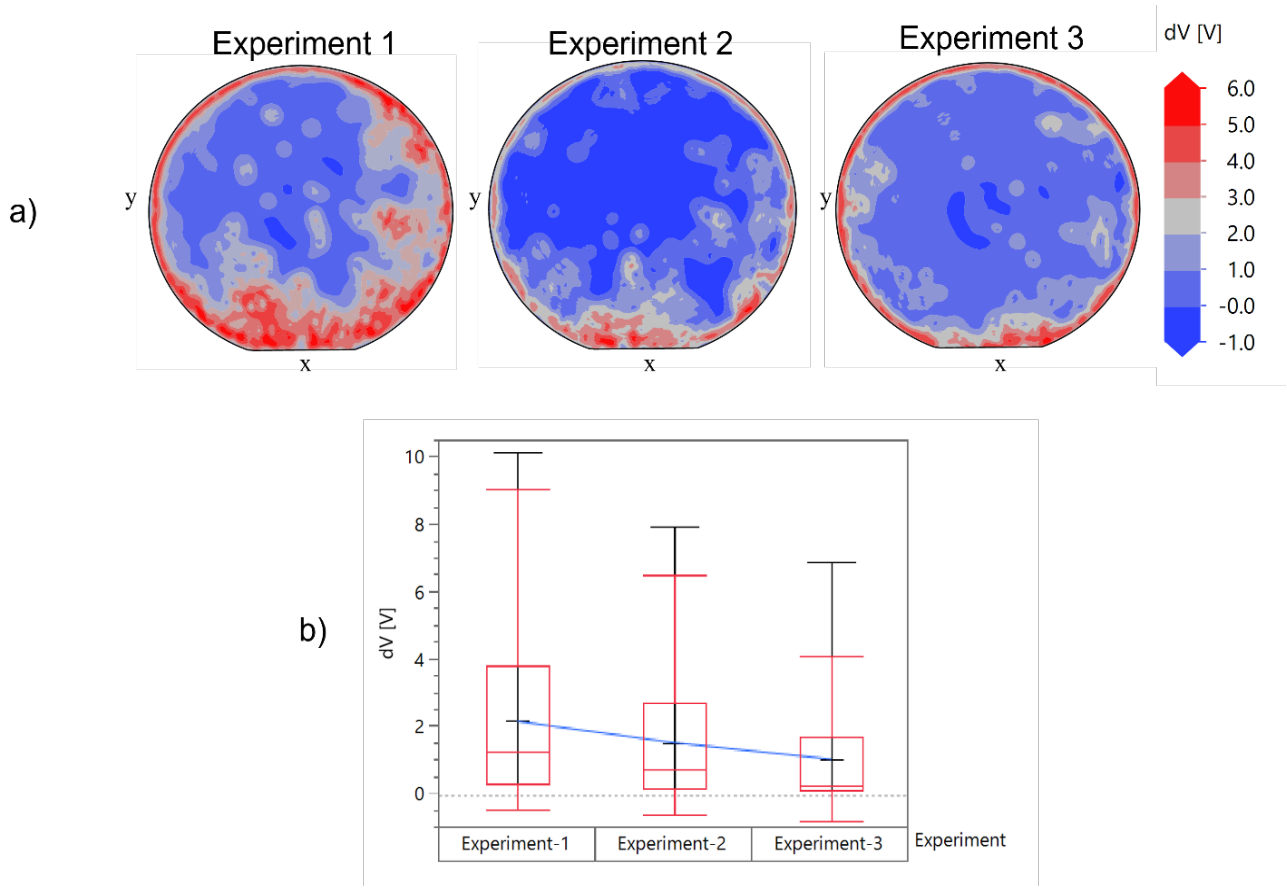

Fig. 5: a) surface leakage contour map of epilayers grown at different buffer layer doping ramp conditions and b) delta potential (dV) plot showing improved leakage condition for ramped buffer layer condition.

Surface potential imaging, by kelvin probe microscopy, was performed on epilayers from Experiments 1-3. Lower surface leakage was observed for Experiment 2 and Experiment 3 compared to Experiment-1 as shown in Fig. 5b. We believe, this reduction in delta potential is due to improved crystal quality of the epilayers using ramped-down substrate-to-buffer layer doping conditions.

The impact of the buffer layer growth rate on epilayer defects was also studied. It was found that higher growth rates reduced basal plane dislocations as shown in Fig. 6a. Further study is needed to explain this improvement in BPDs with higher buffer layer growth rates. Here we are making an effort to explain this reduction in BPDs next.

During the epilayer growth, Si and C adatoms do not only replicate the crystal structure, but they also replicate defects on the surface along the dislocation lines. We believe, when Si and C adatoms reach the surface at a faster rate, replication of BPDs along basal plane gets energetically less favorable and hence they take easier path, perpendicular to the basal plane by forming TEDs.

As a downside, the number of surface pits increased for higher growth rates as shown in Fig. 6b. Further optimization of growth conditions is required to reduce pits on the surface.

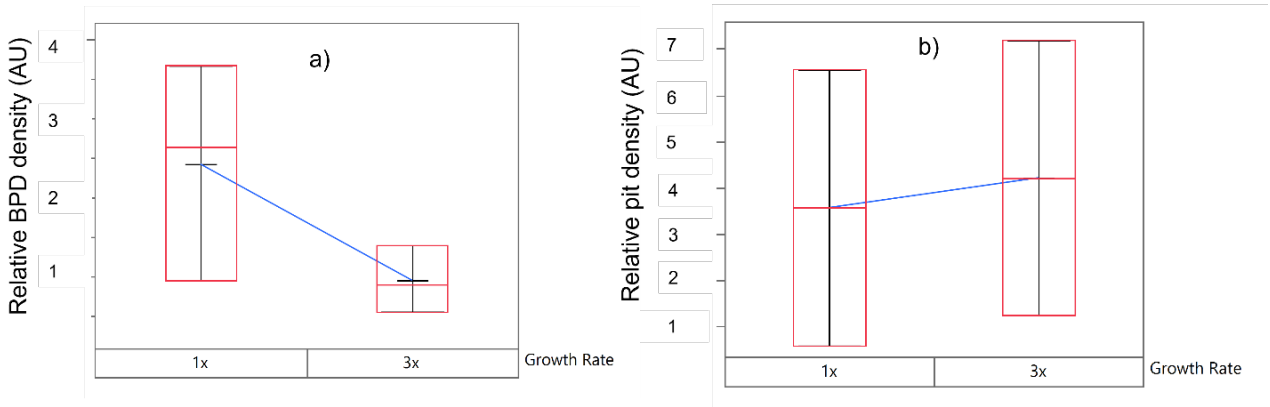

Fig. 6: a) Basal Plane Dislocation (BPD) and b) Pit density at various buffer layer growth rates

Summary

In the present study, the abrupt versus ramped doping change from substrate-to-buffer layer and its effect on defects in epilayers was studied. It was found that a ramped doping transition from substrate-to- buffer layer is beneficial for BPD reduction compared to that of abrupt substrate-to-buffer layer doping transition. We believe this reduction is due to relaxation of misfit related stress at the transition step from substrate-to-buffer layer. The buffer layer growth rate impact on defect densities was also studied. It was found that higher growth rates are beneficial for BPD reduction, but with the disadvantage of increased pit formation. Future studies will investigate the effects of other growth parameters, such as temperature and pressure, during buffer layer growth steps.

References

[1] N. Piluso et al., Materials Science Forum 963, 91 (2019)

[2] Takeshi Tawara et al., Materials Science Forum 897, 419 (2017)

[3] H. Itoh et al., Materials Science Forum 1004, 71 (2020)

[4] L. Yang et al., Journal of Crystal Growth 531, 125360 (2020)

[5] Y. Daigo et al., Materials Science Forum 963, 97 (2019)

[6] Y. Mabuchi et al., Journal of Crystal Growth 531, 125360 (2020)

[7] Gu, Y. et al., Materials 11, 506 (2018)

[8] P, Ramachandran et al., J. Electron. Mater. 27, 308 (1998)

[9] R. Anzalone et al., Materials Science Forum 897, 71 (2017)

[10] T. Rana et al., Materials Science Forum 963, 119 (2019)

[11] V. Pushkarev et al., ICSCRM poster presentation, 2022