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The Development of the Advanced Inspection System to Screen out the BPDs that Extend to Bar Shaped SSFs under Forward Biasing

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Abstract. We are currently developing an inspection system that will provide a low-cost means of screening prior to shipment by fully visualizing latent 1SSF (single Shockley stacking fault) defects originating from basal plane dislocations (BPDs) that cannot be detected by current defect inspection systems. The system will capture not only the defects that expand into right triangles under relatively low-level forward bias, but also the defects that expand into more serious bar-shaped 1SSFs under relatively high-level forward bias, with a particular focus on capturing TED (threading edge dislocation)-converted BPD at or below the buffer layer/substrate interface. Since these defects are known to cause forward voltage degradation during device operation, so-called "burn-in" (accelerated current stress) screening operation is currently utilized in some device manufacturers to avoid the shipping of the defective devices, but it is very time-consuming process which raises a total cost of production. The system we are developing, which can significantly reduce the screening time, has the potential to replace the "burn-in" operation.

Introduction

More than two decades have passed since the reliability issue of the forward voltage degradation of 4H-SiC devices was first reported [1, 2], and since then extensive studies on the issue have been carried out to prove that the degradation is caused by the nucleation and expansion of a 1SSF [3]. The origin of the 1SSF is a BPD which exists in the epilayer or near the epilayer and the substrate (epi/sub) interface. The 1SSFs are expanded by the electron–hole recombination energy when excessive minority carriers are injected into the regions in the vicinity of the BPDs, which is called REDG (recombination-enhanced dislocation glide) mechanism [4].

Subsequent technological insights and process improvements have made it possible to convert more than 99% of BPDs to "benign" TEDs, which do not expand into SSFs, during the epitaxial growth process. However, it was found in recent years that the converted BPDs also expand to 1SSFs from a BPD-to-TED conversion point [5], and then it has been proposed that high impurity concentration buffer layer is inserted between the drift layer and the substrate, in order to prevent minority carriers from reaching the conversion point [5, 6]. Nevertheless, 1SSF expansion is never completely eliminated especially in high current device applications [7].

In addition, there is no commercialized inspection system used in current mass production line that can detect such “malignant” BPDs that are converted to TEDs at or below the epi/sub interface, but expand into 1SSFs, and therefore in some device manufacturers so-called "burn-in" screening is performed, in which the forward voltage degradation is checked, chip by chip, by applying accelerated forward current stress for a certain period. This is a very time-consuming process which raises a total cost of production.

In the following, we propose a new inspection method called the E-V-C (Expansion-Visualization-Contraction) method [8] that captures the “malignant” BPDs. Using the method, we are currently developing a practical screening system to detect these latent defects that have a significant impact on reliability.

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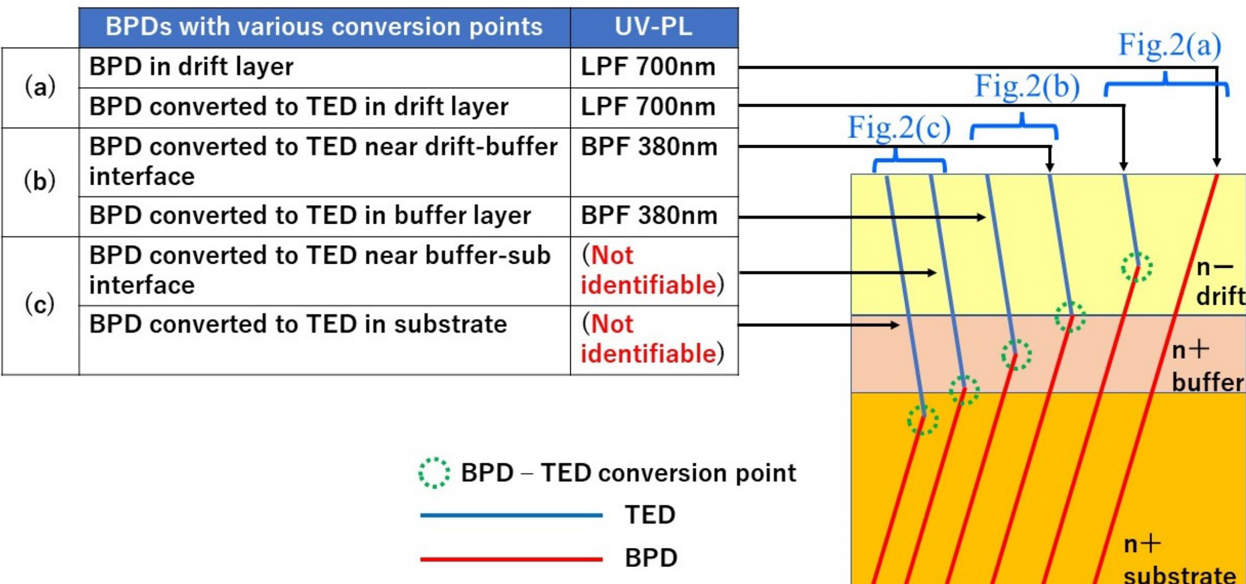
Experimental Results and Discussion

The inspection system under development has the following two main features.

(1) Visualization techniques using UV (ultraviolet) irradiation

BPDs can be classified according to the location of their conversion points to TEDs, as shown in Fig. 1. The sample we have investigated was a commercially available n-type 100 mm Φ 4H-SiC epi-wafer with a 4° off-cut angle, on which heavily nitrogen-doped buffer layer and lightly doped drift layer were epitaxially grown. So far, we can capture the BPD in the drift layer by UVPL (UV photoluminescence) observation technique through a 710 nm LPF (long pass filter) as a bright line [9-11], and also can capture the BPD in the buffer layer through a 380 nm BPF (band pass filter) as a dark line [12], as shown in Fig. 2(a) and Fig. 2(b), respectively. The buffer layer and drift layer profile in Fig. 2(a) are 0.5 μm / 1 x 10^{18} cm^{-3} and 11 μm / 6 x 10^{15} cm^{-3}, respectively, while those in Fig. 2(b) are 10 μm / 1 x 10^{18} cm^{-3} and 10 μm / 1 x 10^{16} cm^{-3}, respectively. However, it has not been possible for us, by UVPL, to reliably capture and visualize the BPD which is converted to TED at or below the buffer layer/substrate interface (Classification (c) in Fig. 1). Instead, by utilizing the property that UV irradiation can induce the same degradation phenomenon as that caused by forward bias, namely, REDG effect [4], we have succeeded in visualizing TED-converted BPD at or below the buffer layer/substrate interface. By irradiating the entire wafer with UV light, we can easily capture the latent defects by targeting the expanded SSFs (plane defects) instead of targeting the BPDs (line defects) at or below the buffer layer/substrate interface. The UV excitation source for expansion of the BPD is a 355 nm, 186 W Nd-YAG laser light, and UVPL observation through a 420nm BPF allows detection of 1SSF (Fig. 2(c)). UVPL observation was performed using a 285-350 nm super-high pressure Hg lamp excitation source with an irradiance of 0.1W/cm^2, a level weak enough not to cause SSF expansion by observation itself. In Fig. 2(c), before UV irradiation, no BPD was observed at the location where the bar shaped SSFs were expanded after UV irradiation, and a bright line BPD was observed only at the location where the right triangle SSF was expanded after UV irradiation. The epi-wafer in Fig. 2(c) is the same as in Fig. 2(a).



	BPDs with various conversion points	UV-PL
(a)	BPD in drift layer	LPF 700nm
	BPD converted to TED in drift layer	LPF 700nm
(b)	BPD converted to TED near drift-buffer interface	BPF 380nm
	BPD converted to TED in buffer layer	BPF 380nm
(c)	BPD converted to TED near buffer-sub interface	(Not identifiable)
	BPD converted to TED in substrate	(Not identifiable)

Fig. 1. Classification by conversion points of BPDs to TEDs

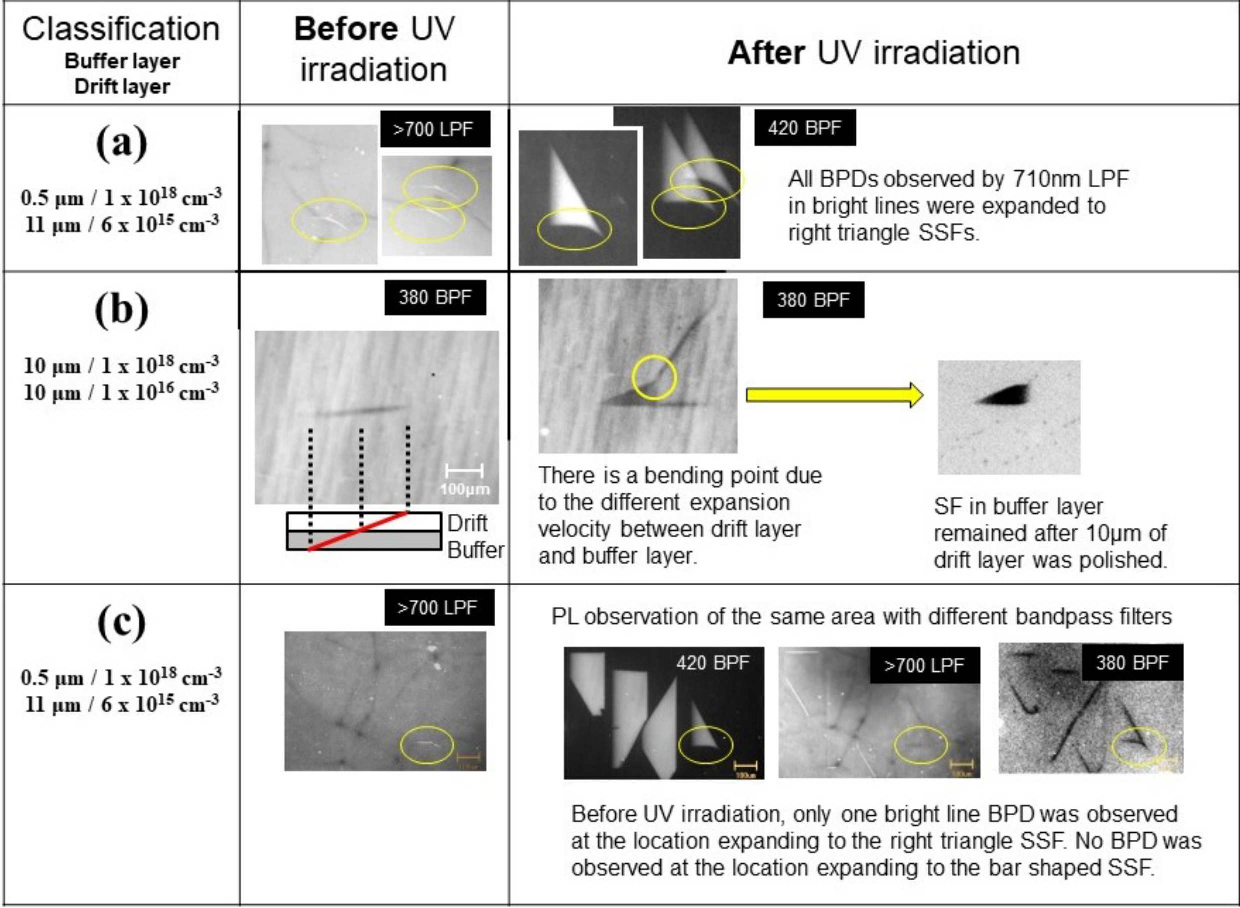


Fig. 2. UVPL observations before and after UV irradiation for each classification

(2) Quantification of the correlation between forward bias and UV irradiation

Under forward bias condition, when the current density exceeds a certain threshold, TED-converted BPDs at the buffer layer/substrate interface start to expand, and as the current density increases further, the BPDs with deeper conversion points also expand [9] and this means that the total number of expanding BPDs increases. The same can be said about the intensity of irradiance in case of the expansion by UV irradiation. If the defect screening is done by unnecessarily intense UV irradiation, that will cause even devices that show no forward bias degradation in a relatively low current application environment to be screened out. This means "overkill", namely a "don't wake sleeping dogs lie" situation.

Thus, it is necessary to adjust the intensity of UV irradiation according to the application (Absolute maximum current rating) of the SiC device, and quantification of the correlation is essential. We quantified the correlation by comparing the expansion glide velocity of 1SSFs between UV intensity and forward bias (current density), using PiN diode devices on the same wafer. The structure of the PiN diode used in our experiment was formed by doping aluminum (1 x 10^{20} cm^{-3}) on the Si face of the epi wafer (buffer layer (0.5 µm, 1 x 10^{18} cm^{-3}), drift layer (5.4 µm, 5 x 10^{15} cm^{-3})). A nickel electrode was then formed on the entire backside of the wafer as Ohmic contacts. Finally, an aluminum electrode array of comb pattern was formed in half the area of the Si face surface wafer for forward bias stress, and the other half of the wafer has no electrode pattern for UV irradiation stress, as shown in Fig. 3.

The PiN diodes were subjected to accelerated pulsed current at three levels of 300 A/cm^3, 350 A/cm^3, and 400 A/cm^3, as depicted in Fig.4. , and the length of the 1SSF was measured by the UVPL method from the position of the Si(g) core partial dislocation visible through the gap between the comb line patterns, which aligned with the step flow direction [1 1 $\bar{2}$ 0] of the wafer, as shown in Fig. 5.

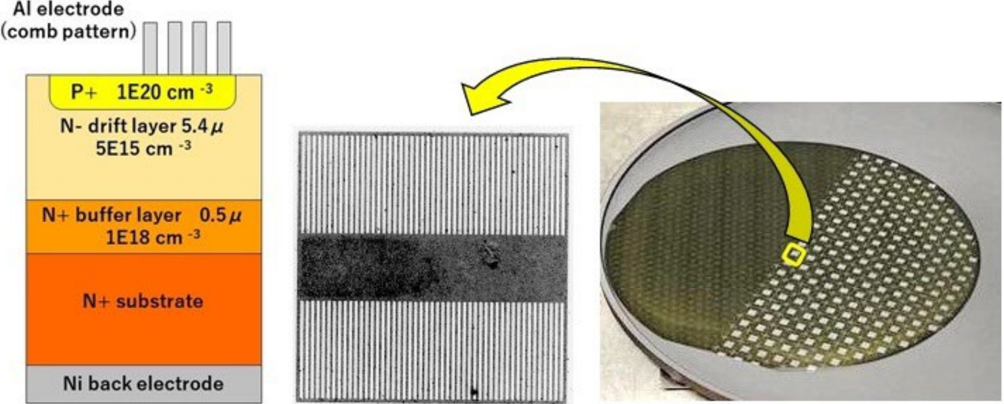


Fig. 3. Schematic diagram of the PiN diode and photos of aluminum electrode pattern on SiC Epi-wafer

The number of measured bar shaped SSFs has been 39 for 300 A/cm^3, 32 for 350 A/cm^3, and 15 for 400 A/cm^3, so far. The measured glide velocities varied considerably even at the same current density, possibly due to various factors that inhibit dislocation glide, such as random defects, etc. Therefore, the median of the measured values at each current density was used as the glide velocity. In addition, since most of the bar shaped SSFs extend from the contact area of the probe to the electrode, they seem to extend downward from the chip surface due to the stress concentration caused by the contact.

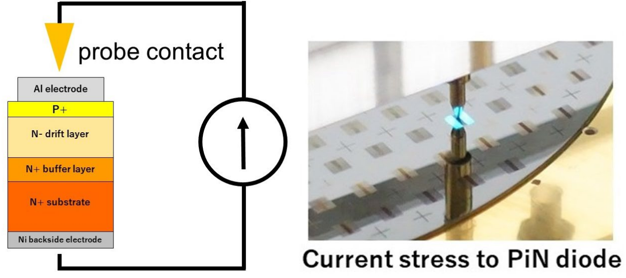


Fig. 4. Accelerated pulsed current stress

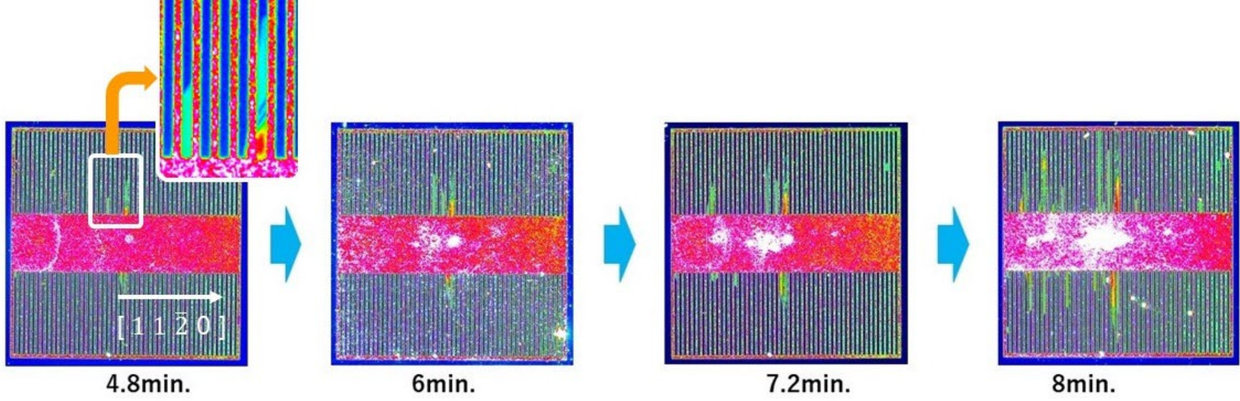


Fig. 5. Forward bias (acclerated current pulse) stress test

While non-electrode patterned area of the same wafer was UV irradiated at four levels of intensity, 18.6 W/cm^2, 46.5 W/cm^2, 93 W/cm^2 and 186 W/cm^2, and the length of the expanded SSFs was measured, as shown in Fig. 6. Bar shaped SSFs are randomly generated on the chip , and most of them extend from the epi/sub interface.

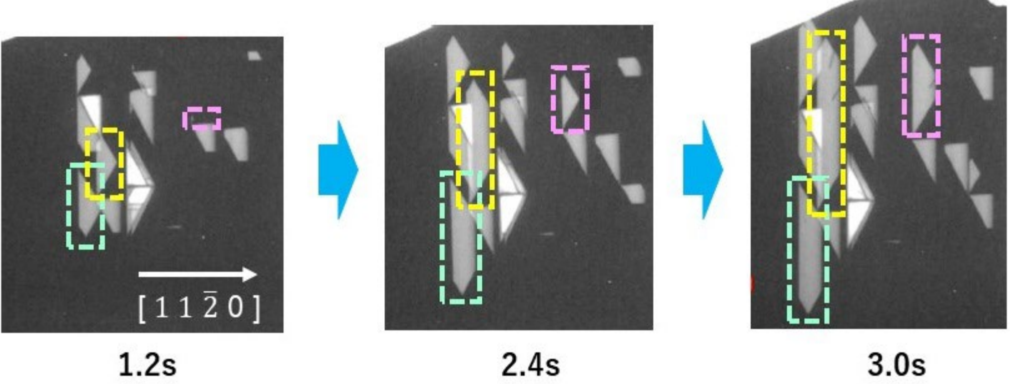


Fig. 6. UV irradiation test

As described above, most of the SSFs observed in the forward bias test originated from the epi layer surface scratches probably caused by probe contacts, expanded downward from the surface, and extended in the ± [1 $\bar{1}$ 0 0] direction after they reached the epi/sub interface. On the other hand, in the case of UV irradiation test, BPDs which converted to TEDs near the epi/sub interface expanded upward from the conversion point and extended in the ± [1 $\bar{1}$ 0 0] direction when it reached the epi surface. Both can be distinguished by whether the apex of the 30° Si core of the extending SSF is on the right or left side of the bar shape. In the case that the [1 1 $\bar{2}$ 0] direction faces to the right, as shown in Fig.5 and Fig.6, the apex of the 30° Si core on the left side of the bar indicates that the SSF would have expanded from the epi/sub interface.

In both cases, when the SSF is UV irradiated or forward biased, the Si core partial dislocation at the leading edge of the SSF glides and the SSF expands. Initially, it forms an isosceles triangle, which expands until the Si core penetrates through the drift layer between the epi/sub interface and the epi surface, and then it elongates in the ± [1 $\bar{1}$ 0 0] direction to form the bar shaped SSF, as shown in Fig.7.

However, in the initial stage of expansion of the isosceles triangle before the bar formation, the depth position of the Si core is different between the two (Fig. 7 a-a'), and therefore, the Si core glide velocity of the two cases might be different because the carrier density of excess holes near the Si core is also different generated by UV irradiation or forward bias. On the other hand, after the Si core penetrates through the drift layer and starts to form a bar shape, the two can be regarded as the same (Fig. 7 b-b'). Therefore, the correlation was quantified by comparing the glide velocity of the Si core in the ± [1 $\bar{1}$ 0 0] direction after the bar formation. We have obtained the result that 400 A/cm^2 of current density, for example, corresponds to 28 W/cm^2 of UV irradiation. Fig. 8(a) and Fig. 8(b) show the dislocation glide velocity against current density and against UV irradiation power, respectively.

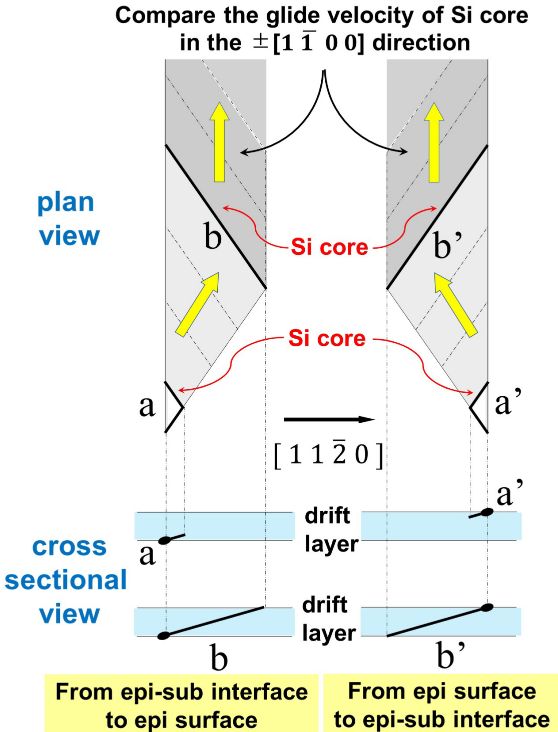


Fig.7. Schematic diagram of the two types of the bar shaped SSF formation

Since it has been reported that the dislocation glide velocity is strongly dependent on the concentration of the injected excess holes [14] either by forward bias or by UV irradiation, numerical simulations of hole concentration at the epi/sub interface are currently in progress to validate the relationship between forward bias and UV irradiation derived from experimental results.

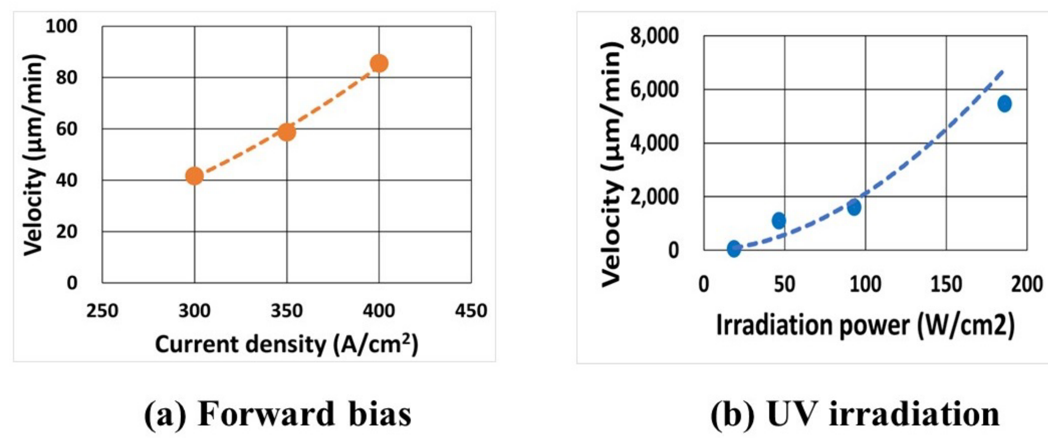


Fig. 8. Degradation by UV irradiation and that by forward bias can be correlated via dislocation glide velocity

Proposal for a New Screening Process

In the right side of Fig. 9, our proposed screening process is shown. In the "Expand" step, the intensity and time of UV irradiation is adjusted according to the application (Absolute maximum current rating) of the device. In the "Visualize" step, expanded defects are visualized with a 420nm BPF to obtain the defect map. Since it is known that right triangle SSFs are formed at a lower level of current injection than bar shaped SSFs [15], the right triangle SSF map can be obtained at the same time as the bar shaped SSF map. At the end of the screening, the expanded defects are contracted to their original or near-original size by low temperature annealing [16,17]. We call this detection and screening method the E-V-C (Expansion-Visualization-Contraction) method.

In some device manufacturers so-called "burn-in" screening is performed, in which the forward bias degradation is checked, chip by chip, by applying accelerated current stress for a certain period. We believe that the chip or product burn-in process can be replaced with our proposed E-V-C screening process, which will significantly shorten the time for screening required and lead to significant cost reductions.

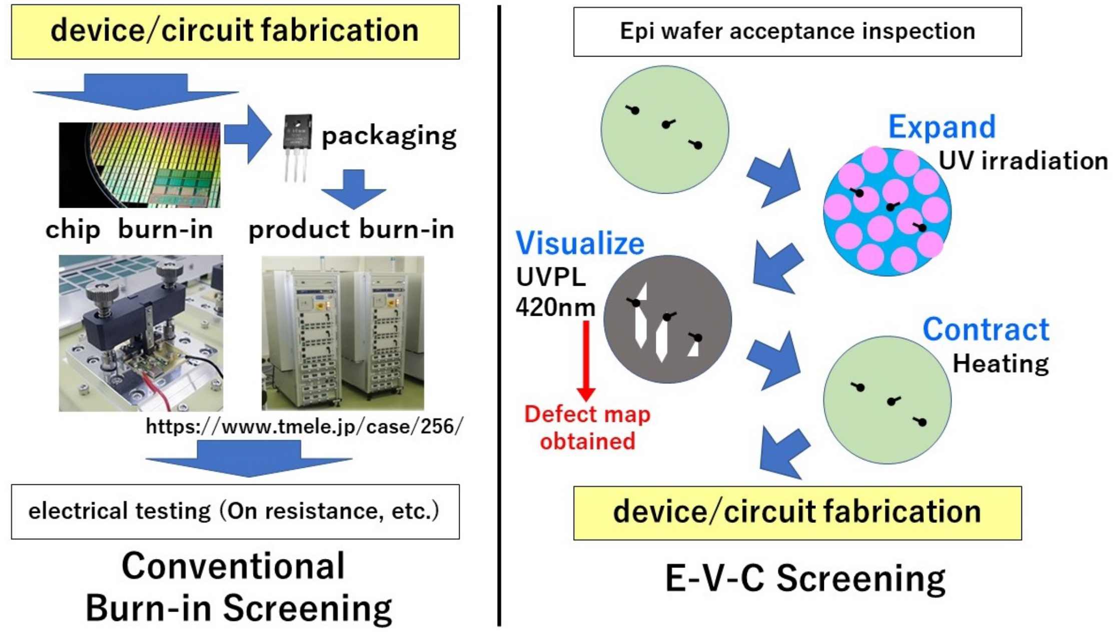


Fig. 9. E-V-C screening VS. conventional burn-in screening

Summary

In this study, we have paved the way for the commercialization of a practical and effective inspection system that can visualize and screen defects that cause forward voltage degradation in the market, which cannot be detected by currently available inspection systems for mass production. To achieve this, the property that UV irradiation can reproduce phenomena equivalent to forward voltage degradation has been utilized. Moreover, the system allows UV irradiation conditions for screening to be optimized for the device application (Absolute maximum current rating) through the quantification of the correlation between UV irradiation and forward bias.

Currently, some device manufacturers perform so-called "burn-in" operation, which is very time-consuming process, but by introducing the proposed screening process, the time for screening can significantly be shortened. Furthermore, in the "burn-in" process, every product is shipped under accelerated current stress, which might cause a certain degree of degradation to progress even for good products, shortening the product life. In contrast, the "Contraction" step in the proposed screening process acts to undo expanded defects and restores the degradation, giving it an advantage over "burn-in" screening. Thus, the system we are developing has the potential to replace the current "burn-in" operation.

References

[1] H. Lendenmann, F. Dahlquist, N. Johansson, R. Soä derholm, P.A. Nilsson, J. P. Bergman and P. Skytt, Mater. Sci. Forum, 353-356, 727 (2001).

[2] J. P. Bergman, H. Lendenmann, P. A. Nilsson, U. Lindefelt, and P. Skytt, Mater. Sci. Forum 353-356, 299 (2001)

[3] M. Skowronski and S. Ha, J. Appl. Phys. 99, 011101 (2006).

[4] K. Maeda and S. Takeuchi, in *Dislocations in Solids*, ed. F. R. N. Nabarro and M. S. Duesbery, (Elsevier, Amsterdam, 1996), pp. 443.

[5] N. A. Mahadik, R. E. Stahlbush, M. G. Ancona, E. A. Imhoff, K. D. Hobart, R. L. Myers-Ward, C. R. Eddy, Jr., D. K. Gaskill, and F. J. Kub, Appl. Phys. Lett. 100, 042102 (2012).

[6] T. Tawara, T. Miyazawa, M. Ryo, M. Miyazato, T. Fujimoto, K. Takenaka, S. Matsunaga, M. Miyajima, A. Otsuki, Y. Yonezawa, T. Kato, H. Okumura, T. Kimoto, and H. Tsuchida,, J. Appl. Phys. 120, 115101 (2016).

[7] S. Hayashi, T. Yamashita, J. Senzaki, T. Kato, Y. Yonezawa, K. Kojima, and H. Okumura, Appl. Phys. Express 12, 051007 (2019)

[8] Japan patent application number (2020) 03567

[9] R. E. Stahlbush, K. X. Liu, Q. Zhang, and J. J. Sumakeris, Mater. Sci. Forum 556–557, 295 (2007).

[10] A. Galeckas, J. Linnros, and P. Pirouz, Appl. Phys. Lett. 81 883 (2002).

[11] K. X. Liu, R. E. Stahlbush, S. I. Maximenko, and J. D. Caldwell, Appl. Phys. Lett. 90, 153503 (2007).

[12] H. Itoh, T. Enokizono, T. Miyase, T. Hori, K. Wada, H. Doi, and M. Furumai, Mater. Sci. Forum, 71-77, 1004 (2020).

[13] K. Konishi, R. Fujita, K. Kobayashi, A. Yoneyama, K. Ishiji, H. Okino, A. Shima, T. Ujihara, AIP Advances 12, 035310 (2022).

[14] T. Tawara, S. Matsunaga, T. Fujimoto, M. Ryo, M. Miyazato, T. Miyazawa, K. Takenaka, M. Miyajima, A. Otsuki, Y. Yonezawa, T. Kato, H. Okumura, T. Kimoto, and H. Tsuchida, J. Appl. Phys. 123, 025707 (2018).

[15] S. Hayashi, T. Yamashita, J. Senzaki, M. Miyazato, M. Ryo, M. Miyajima, T. Kato, Y. Yonezawa, K. Kojima, and H. Okumura, Jpn. J. Appl. Phys. 57, 04FR07 (2018).

[16] T. Miyanagi, H. Tsuchida, I. Kamata, T. Nakamura, K. Nakayama, R. Ishii, and Y. Sugawara, Appl. Phys. Lett. 89, 062104 (2006).

[17] J.D. Caldwell, R.E. Stahlbush, K.D. Hobart, O.J. Glembocki, and K.X. Liu, Appl. Phys. Lett. 90, 143519 (2007).