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Correlation of Extended Defects with Electrical Yield of SiC MOSFET Devices

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Abstract. The quality of the silicon carbide (SiC) epitaxial layer, i.e., layer homogeneities and extended defect densities, is of highest importance for high power 4H-SiC trench metal-oxide-semiconductor field effect transistors (Trench-MOSFET) devices. Especially, yield for devices with a large chip area is severely impacted by extended defects. Previously, devices had to be fully manufactured to effectively gauge the impact of a reduction in extended defect densities in the epitaxial layers on device yield. The production of devices such as Trench-MOSFETs is an extensive procedure. Therefore, a correlation between extended defects in the epitaxial layer and electrical device failure would allow to reliably estimate the impact of process changes during epitaxial layer deposition on electrical device yield.

For this reason, n-type epitaxial layers were grown on around 1,000 commercially available 150 mm 4H-SiC Si-face substrates, which received a chemical wet cleaning prior to the epitaxy deposition. Substrates with lowest micro-pipe density from two different suppliers were used. The wafers were characterized with the corresponding device layout for defects utilizing surface microscopy as well as ultraviolet photoluminescence techniques. Subsequently, these wafers were used to produce more than 500,000 Trench-MOSFET devices. All devices have been tested on wafer level for their initial electrical integrity.

With these methods a precise correlation between extended defects in the epitaxial layer and electrical failures on wafer level could be found. The influence of different substrates on the defect-based yield prediction regarding the electrical yield on wafer level is discussed. Additionally, a calculated kill-ratio is presented and the severity of defect classes on initial device failure, e.g., stacking faults, and their key failures modes are discussed.

Introduction

Silicon carbide (SiC), especially the 4H poly-type, possesses superior physical, electrical and thermal properties compared to silicon. These properties result in an increasing commercial interest of SiC as a material for high-power and high-voltage semiconductor devices. Thus, small and efficient SiC devices, e.g., trench metal-oxide-semiconductor field effect transistors (Trench-MOSFETs) in high-power inverter modules, are steadily replacing established silicon technologies [2–4].

High quality homo-epitaxial layers on mono-crystalline substrates with low defect densities are a key feature concerning the functionality and reliability of such devices. The absolute thickness and doping concentration of the deposited layers, including their respective homogeneities, is important for the quality of the epitaxial layers. The densities of extended surface and crystallographic defects impact the quality of the epitaxial layers as well [4–6]. Most defects in the epitaxial layer are caused by existing imperfections in the substrates. Not all extended defects are critical for device operation or reliability. Therefore, a further classification between device critical and non-critical defects has to be made [4–7].

This paper presents a method to correlate extended defect data of homo-epitaxial layers with the corresponding electrical yield of Trench-MOSFETs. In this study classes of extended defects could be defined to be critical for initial electrical performance and reliability of the investigated devices. Therefore, a statistically significant number of defect measurements were correlated with electrical tests on wafer level.

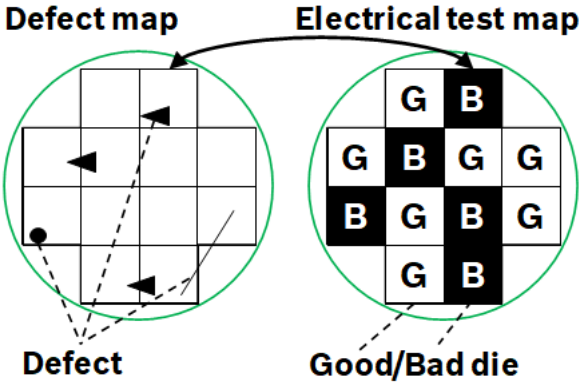
Experimental Procedure

Commercially available 150 mm 4H-SiC substrates with off-cut angle of 4° towards the [11$\bar{2}$0] direction were used for this investigation. Homo-epitaxial layers were grown using a multi-wafer warm-wall chemical vapor deposition epitaxy reactor. All n-type layers were grown on "epitaxy-ready" polished and wet chemical cleaned Si-face substrates with low micro-pipe density.

The devices were manufactured following the same manufacturing process flow for Trench-MOSFETs. A general overview of this process flow for Trench-MOSFETs can be found elsewhere [8]. Lasertec's SICA88 was used for surface and crystallographic defect analysis. This tool was utilizing confocal differential interference contrast optics for surface inspection and ultra-violet photoluminescence (UV-PL) imaging. Wafer level tests for all processed devices were carried out on standard semiconductor manufacturing testing equipment. All components were tested under the same conditions as far as possible.

A total of approx. 1,000 wafers were manufactured, characterized, and electrically tested for this investigation. The manufacturing process for these wafers was kept as constant as possible within the margins of semiconductor production. With these wafers more than 500,000 Trench-MOSFET devices were produced and electrically tested.

A defect-based yield prediction was calculated using the device layout, i.e., excluding the scribe lines and test structures. The defect characterization on structured wafers allowed for a local precision of up to 5 µm, which was crucial to correlate this data to electrical tests. The device critical defect classes considered for the defect-based yield prediction included scratches and polytype inclusions originated in the substrate, basal plane dislocations, various types of stacking faults excluding UV-PL only types, as well as downfalls and downfall related defects [6,7].



Electrical integrity	At least one defect	No defects
Good	G_D	G_{ND}
Bad	B_D	B_{ND}

Fig. 1. Four possible die categories and their visualization used in the calculation of the "Kill-Ratio" after Ono et al. [1].

A "Kill-Ratio" (KR) for the chosen device critical defects was calculated using the definite device layout [1]:

$$KR = 1 - \frac{\frac{G_D}{(G_D+B_D)}}{\frac{G_{ND}}{(G_{ND}+B_{ND})}}. \quad (1)$$

G_D/B_D refers to electrically good/bad devices with at least one critical defect and G_{ND}/B_{ND} refers to devices without any extended device critical defects.

In Fig. 1 the four possible categories of a die (**G**ood/**B**ad, **D**efective/**N**on-**D**efective) are shown. This means, that the KR corresponds to the number of false positives and true negatives for the device critical defects. Therefore, the number between 0 and 1 assesses the quality of the critical defect-based yield prediction regarding electrical device failures. A value of 0 refers to "no impact" of a certain defect on the electrical yield, whereas a value of 1 means "definitive" device failure during wafer level tests.

Results

In Fig. 2 the exemplary normalized defect-based yield prediction and the normalized real electrical yield on wafer level tests of 23 wafers is shown. The average yield prediction was set to 1 and all other values were adjusted accordingly. The Trench-MOSFET devices were manufactured on substrates of two different suppliers (A and B). Fig. 2 shows that the accuracy of the defect-based yield prediction varies between different substrates. For substrates A the defect-based yield prediction is on average 1.048. For substrates B the average yield prediction is 0.947. The normalized electrical yield for substrates A is on average 0.759 and 0.758 for B. Furthermore, the average difference between defect-based and electrical device yield for substrates A is 0.289 and 0.189 for B.

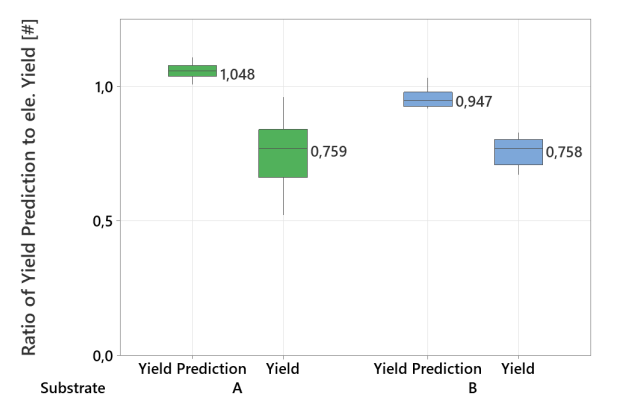


Fig. 2. Normalized defect-based yield prediction vs. normalized electrical yield on wafer level tests of two substrate suppliers. For the defect-based yield prediction a device layout and only device critical defects were considered.

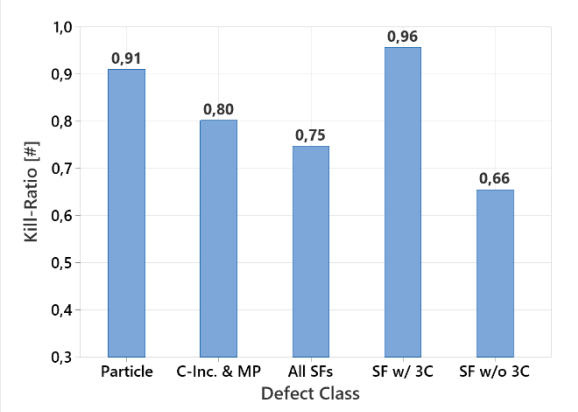


Fig. 3. Calculated "Kill-Ratio" of most important critical defects on more than 500,000 electrically analysed Trench-MOSFET devices on supplier B substrates.

Fig. 3 shows the calculated KR for chosen critical defect classes of more than 500,000 Trench-MOSFETs on substrates B. The KR for particles and related defects is 0.91 and for C-inclusions and micro-pipes (MPs) 0.8. Considering all types of stacking faults (SFs) with a surface topology the KR is 0.75. Dividing all SFs into SFs with 3C-inclusions and into (partial) SFs without 3C-inclusions the KR is 0.96 and 0.66, respectively.

Fig. 4 shows the ratio of different initial electrical device failures on wafer level of Trench-MOSFETs for each considered critical extended defect class. Here only good/bad devices with extended defects (G_D/B_D) are taken into account. Devices without any extended defects (G_{ND}/B_{ND}) are not part of this evaluation. Different electrical failures regarding leakage currents, i.e., the drain-source (I_{DSS}), the gate-source (I_{GSS}) at different gate voltages (20/40 V), as well as the breakdown voltage ($V_{(BR)DSS}$) are shown separately. 12 additional electrically tested parameters are shown as the "Sum of other Failures". Devices with extended defects but without any failed electrical parameter limits are grouped "No Failure". For particle related defects around 72% of failures are due to different leakage currents. Considering all stacking faults around 66% of affected devices fail with increased leakage currents. Whereas 80% of SFs with 3C-inclusions and 60% without 3C-inclusions fail due to leakage currents. C-inclusions and MPs result in 54%, BPDs in 38% and scratches in 31% of leakage related failures.

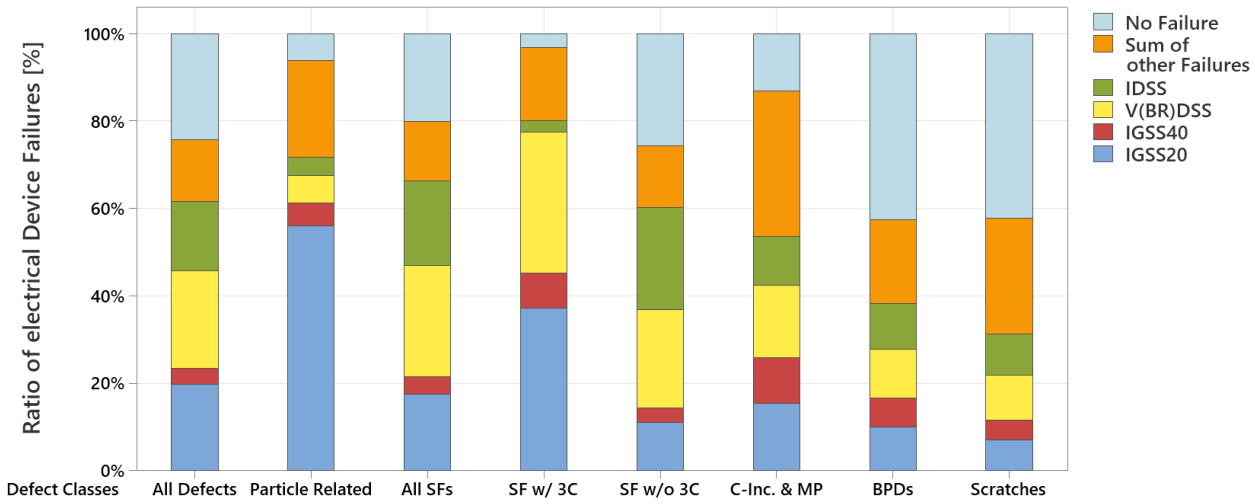


Fig. 4. Normalized ratio of different initial electrical device failures on wafer level of Trench-MOSFETs for each considered critical defect class. Only (electrically good/bad) devices with defects are considered.

Discussion

Comparing the normalized defect based predicted yield with the (wafer level) electrical yield of 23 different substrates (Fig. 2) shows a significant difference in prediction accuracy. For substrates of supplier A, a difference between normalized predicted and electrical yield of 0.289 and 0.189 for epitaxial layers on supplier B substrates is measured. Therefore, on supplier B substrates the yield prediction is more accurate by 0.1. All wafers have been processed with the same tools as well as under the same conditions as far as possible. Thus, an influence due to process variation during device production has been reduced as much as possible. It is possible that this difference is due to a reduced detection of device critical defects or because of substrate intrinsic variation, e.g., doping level and homogeneity or substrate defects. An improvement to the defect detection algorithm could increase the yield prediction accuracy on supplier A substrates because some extended defects, e.g., stacking faults, can differ slightly in their occurrence between A and B.

When looking at the most important extended critical defect classes (Fig. 3) a KR of more than 0.66 is calculated. This corresponds to a high accuracy in the defect-based prediction of electrical failures. An electrical failure of a device affected by particle related defects is very likely. Taking all stacking faults into account, a significant difference in the KR (0.3) between those with and without 3C-inclusions shows, though the KR is high for an optical inspection method. SFs with 3C-inclusions are of very similar appearance, whereas SFs without 3C-inclusions can significantly differ in their detected shape. Therefore, a lower impact on electrical yield can be expected due to a larger variation in different occurrences. Additionally, further defect properties, e.g., position within the die or other defects as well as their number, are not considered. Larger defects, i.e., particle related and SFs with 3C-inclusions, affect a larger area within the die. Considering that not all parts of a device are electrically active, a larger affected area results in a higher probability of device failure. Conversely, the probability of device failure is lower if less device area is affected by smaller defects.

Evaluating electrical wafer level tests of defect-affected Trench-MOSFETs (Fig. 4) it is depicted that different leakage currents are the predominant failure modes. This aligns with known literature, where different types of stacking faults or particle related extended defects can cause leakage currents for SiC devices [4,6,7]. It is shown that most of these defects, excluding BPDs and scratches, are very likely to cause leakage currents in Trench-MOSFET devices. The failure rate of devices affected by BPDs, and scratches is significantly lower. This is due to the nature of the shown wafer level tests. Basal plane dislocations are known for causing bipolar degradation of the body diode in Trench-MOSFETs rather than initial device failure. Since BPDs can occur beside other defects within one device their KR and ratio of electrical device failures is not zero although they are not the cause

of the failure. Not all detected scratches are detrimental for the electrical device performance. The used algorithm could not distinguish between “shallow” or “deep” scratches. Deep scratches can cause additional defects, e.g., stacking faults, and therefore device failure. Shallow scratches may not cause additional defects.

It is therefore necessary for the defect-affected electrically good devices to undergo additional more exhaustive electrical (stress) testing, e.g., burn-in or high-current stress tests. Discarding affected devices based on the defect analysis can also reduce the chance of electrical failure and therefore improve quality.

Conclusion

This paper shows the high accuracy of defect-based yield prediction that can be achieved for Trench-MOSFET devices regarding electrical yield on wafer level. Additionally, the “Kill-Ratio” of the most important device critical extended defect classes as well as the main failure mode of affected devices during electrical testing are discussed. Therefore, a total of around 1,000 substrates (supplier A and B) were characterized for their defects with the definite device layout. With those wafers more than 500,000 similar Trench-MOSFET devices have been manufactured using a typical process flow. Comparing the defect-based yield prediction with electrical yield for 23 wafers a clear difference in prediction accuracy was identified. The yield prediction is significantly more accurate on substrates of supplier B. The root cause for the difference between substrate suppliers (A and B) is still under investigation. Calculating the KR for devices on substrates B a correlation between the most important critical defect classes and device failure during wafer level tests was verified. Large defects, i.e., particle related defects, 3C-inclusions and MPs, and SFs with 3C-inclusions, resulted in an accurate defect-based prediction of electrical device failure. The KR of SFs without 3C-inclusions was lower due to the more varying occurrences of this type of defects. We were able to show that different leakage currents, i.e., I_{DSS}, I_{GSS} and $V_{(BR)DSS}$, were the main electrical failure modes during wafer level tests for the most important extended defects. Most failure modes for devices affected by BPDs and scratches were identified to not correlate to leakage currents. BPDs are not known to affect the initial electrical device performance. Scratches need to be further differentiated into “shallow/deep” types for a more accurate defect-based yield prediction.

Improving and verifying the defect-based yield prediction with higher statistics of electrical device data on wafer level as well as further refined defect classes will be the subject of future investigations.

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