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Investigation of BPD Faulting under Extreme Carrier Injection in Room vs High Temperature Implanted 3.3kV SiC MOSFETs

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Abstract. Implantation process for high Al dose p+ contact layers in SiC MOSFETs can generate new basal plane dislocations (BPDs). Such BPD faulting under high carrier injection was investigated in SiC MOSFET layers designed for 3.3kV operation with either room temperature (RT) or high temperature (HT) implantations performed for their high dose p+ contact layer. For excess carrier injection levels of ~1x10^{18} cm^{-3} implant induced BPDs faulted from the termination regions of the MOSFETs in the case of RT samples, while the HT samples show no BPD faulting because there were no implant-induced BPDs. However, in the active region of the device no BPDs faulted for both the RT as well as HT samples even at a higher carrier injection of ~1x10^{19} cm^{-3}. Technology computer-aided design (TCAD) simulations show that the lower doped p-well region below the p+ contact in the active area of the device prevents the minority electron density in the p+ contact layer to below 10x the hole density, which limits BPD faulting even when they are present in that layer as in the case of RT implanted samples.

Introduction

Silicon Carbide (SiC) based metal-oxide-semiconductor field effect transistors (MOSFETs) in the voltage class 900 V-3300 V have successfully been commercialized due to significant improvement in as-grown material defects that influence device performance and reliability [1, 2]. Previously, it was reported that room temperature (RT) implantation with high p-type Al dose can generate basal plane dislocations (BPDs) in SiC devices [3]. These BPDs can cause stacking fault (SF) expansion during MOSFET switching when the body diode is turned on, and result in degradation of on-state resistance and higher reverse leakage currents [4]. Several of these newly generated BPDs have been mitigated either by high temperature (HT) ion implantation or by other processing techniques such as post implant oxidation [5]. However, it is desirable to perform RT ion implantation to reduce high temperature fabrication steps that causes unnecessary thermal stress, and may reduce device yield. It is also unclear how the differently doped regions of the device structure influences faulting of SFs. Also for pulsed-power application it is critical to investigate the impact of the process induced BPDs with extreme current injection conditions. In this work, we investigate BPD faulting generated by either RT or HT ion implantation for the high Al dose p+ implants, and evaluate the ruggedness and reliability of the devices under very high carrier injection conditions.

Experimental Procedure

For this work, SiC MOSFETs with 30 μm drift layers were fabricated on four 150 mm diameter SiC wafers at a commercial foundry. These MOSFETs were designed for standoff voltage of 3.3 kV. Two of the wafers had a room temperature implant for the high Al dose p-type contact layer, while the other two wafers had a high temperature implant performed at ~ 600 ºC. The p+ Al implants in

the termination region was also performed at the same time along with the p+ contact region. More than 100 device dies were removed from each of the four wafers, and their metal layers were removed to observe generation of fabrication process induced extended defects. UV photoluminescence (UVPL) imaging using a 355 nm laser and a custom microscope was performed before device fabrication on full wafer, and after the complete device fabrication following the metal removal. The UVPL imaging was performed with low excitation power (~65 Wcm^{-2}) on the 4 samples for more than 400 SiC MOSFETs. This was followed by UV excitation of >1500 Wcm^{-2} and >13000 Wcm^{-2} on several MOSFET device dies. Sequence of UVPL images were collected to study progression of any new implant-induced SF expansion. Simulation of current injection in typical MOSFET structures was performed using TCAD and correlated with the UV carrier injection conditions.

Results and Discussion

Upon UV exposure and imaging of hundreds of MOSFET dies at 65 Wcm^{-2} excitation for several hours for either RT or HT implanted samples, no new BPDs were observed to fault. This carrier injection is similar to typical device operating conditions of ~100 Acm^{-2}. The excess carrier density was numerically simulated and estimated to be ~$5x10^{16}$ cm^{-3} in the p+ layer with this excitation, which is ~2-3 orders below background doping. At 65 Wcm^{-2} UV excitation, the injection in the drift layer was ~$1x10^{17}$ cm^{-3}, which would cause any SF expansion from growth related BPDs existing in the wafers. However, due to the high quality of the wafers used in this study almost no growth-related BPDs existed previously in the MOSFET dies that were examined. Subsequently upon UV excitation at higher power of 1500+ Wcm^{-2}, SF expansion from BPDs were observed in the RT implanted samples from the termination regions, but not from the active region, as shown in Figs. 1(a) and 1(b). The SFs expanded from the epitaxial layer surface towards the substrate-epitaxial layer interface, which is from right to left in the image, and opposite to the step-flow direction. This indicates that these BPDs were in fact generated during the RT implantation process near the epitaxial layer surface. A cross-sectional schematic of this is shown in Fig. 1(c) where a BPD that is created near the surface due to implantation expands upon carrier injection and propagates towards the surface. The estimated carrier injection in the p+ layer at this power is ~$1x10^{18}$ cm^{-3}. Such SF expansion, however, was not observed from the active regions of the device. The reason for this will be discussed later.

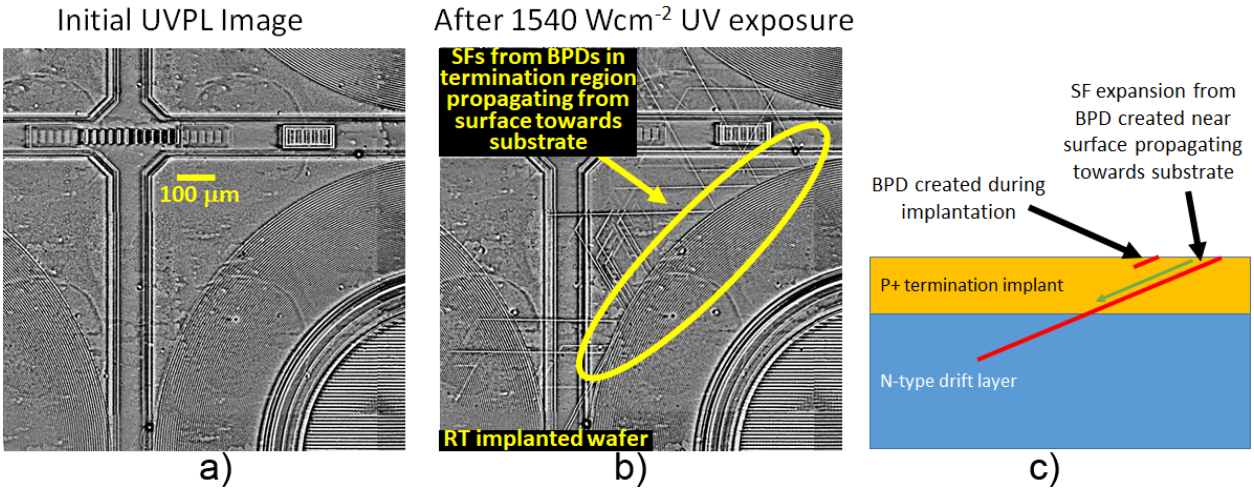

Fig. 1. UVPL images of room temperature (RT) implanted SiC MOSFET (a) before and (b) after carrier injection with >1500 W/cm^2 UV carrier injection showing BPD faulting and SF expansion in the termination region. c) shows cross-sectional schematic where implantation induced BPDs generated near the surface cause SF expansion and propagate towards the substrate interface.

The HT implanted samples were also subjected to same UV excitation at >1500 Wcm^{-2}. Fig. 2(a) and 2(b) show before and after UV exposure images, where no new SF expansion is observed from any region of the device. This was consistent with all the devices measured, which indicates that the

HT implantation process prevents the initial formation of new BPD segments in the p+ layer and, therefore, causes no SF expansion. Fig. 2(c) shows the simulation of estimated carrier injection from the UV excitation, where the p+ contact, p-well and n-type drift layers were included with arbitrary thicknesses. The carrier injection at this UV power level is within ~10x the typical doping of the high dose p+ layer. If BPDs were present, SF expansion is likely to occur and be observed in UVPL images as in the case of the RT implanted conditions. This indicates the HT implantation process does not generate new BPDs.

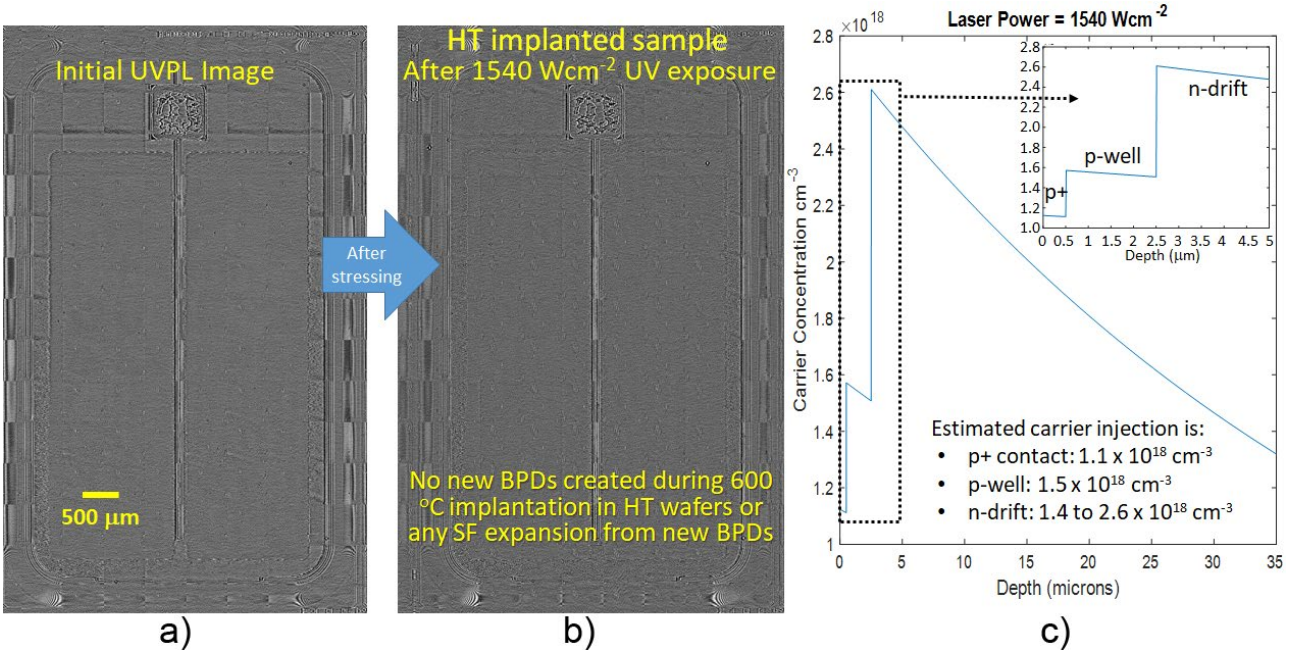

Fig. 2. UVPL images of HT implanted SiC MOSFET (a) before and (b) after carrier injection with >1500 W/cm^2 UV carrier injection showing no BPD faulting from any region of the device die. c) Estimated carrier injection profiles simulated from a p+ contact layer, a p-well and n-drift layers with arbitrary thicknesses emulating a typical 3.3kV SiC MOSFET.

Following this, the RT implanted samples were subjected to higher UV laser stressing with power density of over 13,000 Wcm^{-2}. Under this condition, the SFs from the termination region expanded more rapidly due to higher carrier injection, and spanned throughout the epitaxial layer. They also expanded spatially into the active region of the device after they initially faulted/originated from the termination region. However, upon analyzing the SF expansion behavior, no BPDs were found to fault that initiated from the active region of the device as shown in Fig. 3(b). Fig. 3(a) shows the UVPL image of the full MOSFET die, from which a central region of the active area is magnified in Fig. 3(b), where no new SFs are observed. The estimated carrier concentration from the top 5 µm of the MOSFET layer structure is shown in Fig. 3(c), which shows ~1x10^{19} cm^{-3} excess carriers generated in the high dose p+ layer. BPD faulting appears to be prevented in the active device region even at such high injection conditions. The UV carrier injection profile depends primarily on an exponential penetration depth and carrier lifetime of the layer. Doping level does not play a direct role. For a similar carrier injection level at the top of this device structure, electrical injection would fall off more rapidly than UV carrier injection due to its dependence on layer doping. Hence UV carrier injection, used in this study with >13kWcm^{-2} power, has higher carrier generation compared to similar electric current injection. This demonstrates the robustness of the active area of the MOSFET to potential high current stress. During device operation, carrier densities should not approach such high levels in the termination region with proper design, even at high pulsed conditions.

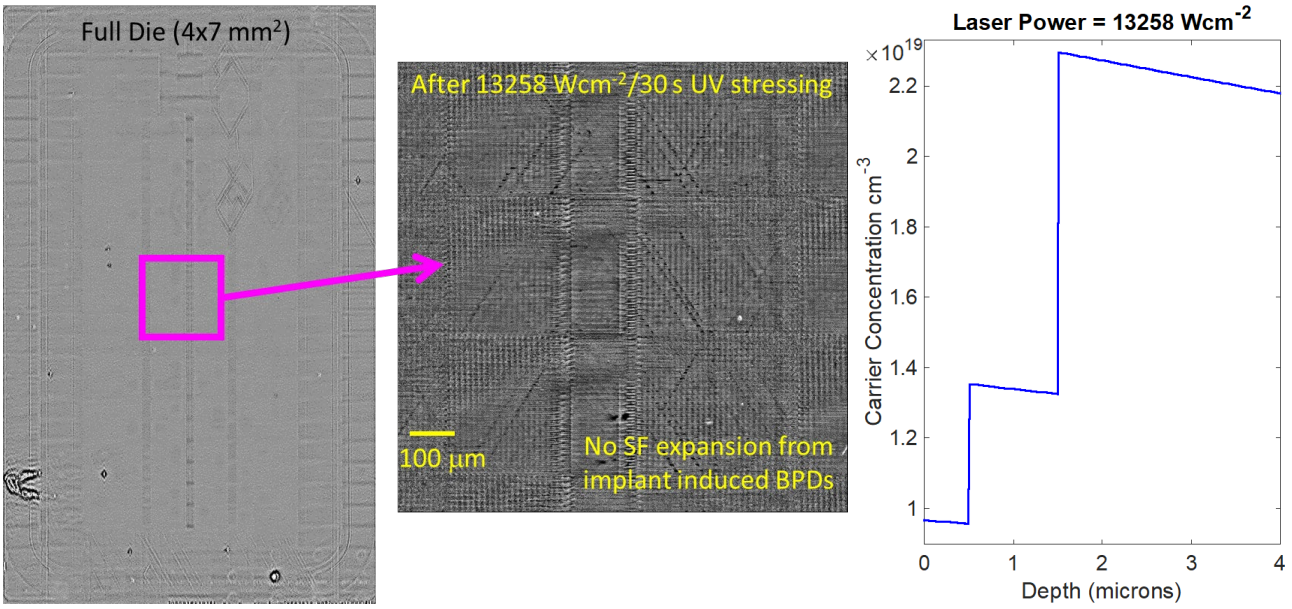

Fig. 3. UVPL images of (a) full MOSFET die and (b) magnified view from center of active region after carrier injection with >13 kWcm^{-2} UV carrier injection showing no BPD faulting. c) Estimated carrier injection profiles of top 5 µm showing high injection of ~1x10^{19} cm^{-3} excess carriers in the p+ implanted region.

However if the carrier density reaches high levels, BPDs can fault and SFs can expand from the termination region into the active region and cause device failure. Hence BPD faulting in the termination region should also be mitigated under high carrier injection. Furthermore, the reason why BPDs faulted in the termination region and did not fault in the active region needs to be investigated.

To understand this, TCAD simulations were carried out in the MOSFET layers from the termination region vs the active device region, where the primary difference was the absence of the lower doped p-well in the termination region. Figure 4 shows the 2D carrier density profiles as well as a 1D profile with an electrical current injection of 5000 Acm^{-2}. It was found that the lower doped p-well in the active region below the p+ contact region causes the minority electron density in the p+ contact region to be significantly lower than background doping in the p+ contact layer. This is likely due to an injection of holes from the p-well to enhance recombination with the injected electrons in the p+ contact layer. Since the RT implantation generates BPDs in the p+ contact region, there are fewer minority electrons in that region to recombine at the BPDs, which would prevent their faulting and SF expansion even at very high carrier injection conditions. Carrier recombination at the BPDs is the primary mechanism for BPD faulting [6]. TCAD simulations were also carried out with 20,000 Acm^{-2} injection level, which shows the electron and hole concentrations getting closer in the p-well, but still had ~5X lower electron density in this layer. The absence of this p-well in the termination region allows the minority electrons to reach higher and similar concentrations as the holes. Even through the carrier lifetime would be low in the p+ layer, at high enough carrier injection, the implant-induced BPDs can fault and result in SF expansion, as observed in the UVPL images from this study. To mitigate this, the termination region can be designed with modifications to alter doping profiles so that carrier densities do not reach ambipolar conditions near the p+ implanted contact layer, or HT implantation can be carried out. However to avoid the disadvantages of HT implantation, design modifications can be used to enhance the robustness of SiC MOSFETs for high current applications

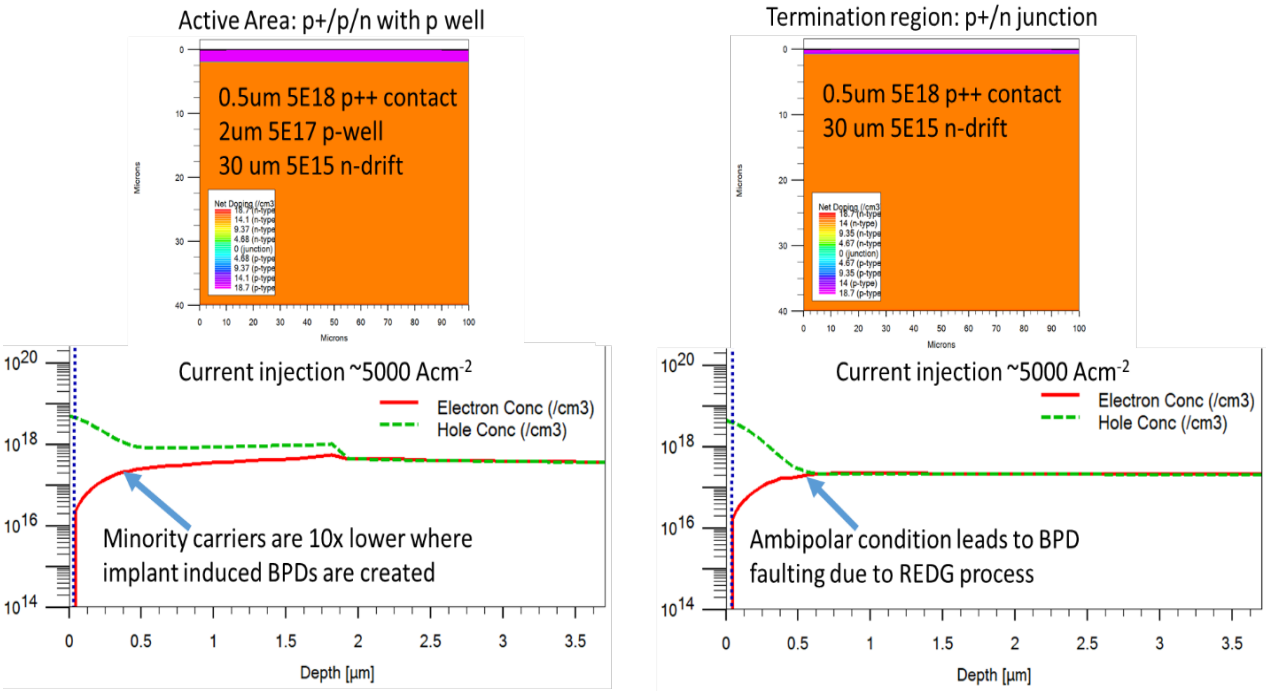

Fig. 4. TCAD simulation of electrical injection in the MOSFET structure (left) in active device region with p-well and the p++ contact, and (right) without the p-well region for the condition in the termination region of the device. The carrier concentration curves under 5,000 Acm^{-2} injection are plotted for both the epitaxial layer conditions below.

Summary

In this paper, we demonstrated the ruggedness of SiC MOSFETs layers designed for blocking voltage of 3.3kV to faulting of implant-induced BPDs for both RT as well as HT implanted high dose p+ layer under high carrier injection up to $1x10^{19}$ cm^{-3}, which is similar to greater than $10kAcm^{-2}$ in the active device area. Carrier injection was carried out using high intensity UV excitation at >1500 Wcm^{-2} and >13 $kWcm^{-2}$. HT implanted samples showed no BPD faulting from any region of the device. However, BPD faulting was observed in the RT devices from near the termination region, which also had the same high dose p+ implants. Hundreds of MOSFET dies were measured with consistent results for both the RT and HT samples. TCAD modeling indicated that the p-well, which is below the p+ contact layer in the active area, prevents the faulting of implant-induced BPD due to enhanced recombination of the minority electrons in the p+ contact layer. This inhibits the recombination at the BPDs and prevents their faulting. Due to the absence of the p-well in the termination region, electron density quickly approaches the hole density causing BPDs to fault and SF expansion that can propagate throughout the epitaxial layer and also spatially into the active area, causing device failure. Even though high carrier injection generally does not occur in termination region, this can be a serious reliability issue and can be mitigated by proper design of the doping profiles in the termination region.

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