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Epitaxial Defectivity Characterization Combining Surface Voltage and Photoluminescence Mapping on 200mm 4H-SiC Wafers

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Abstract. Charge biased non-Contact Voltage imaging, QUAD (Quality Uniformity And Defects) is measured on epitaxial layers grown on 25 wafers of 200 [mm] 4H-SiC. Electrical data is analyzed and deviations in the ΔV signal are compared with defectivity observed by the optical surface detection system with UV-PL capability. Reliable statistical data of the relationship between decreasing voltage and defect classification show good detection of triangles and several other defects in the epitaxial layers. The QUAD mapping gives a good first indication of the electrical active defectivity of an epitaxial layer.

Introduction

The Silicon Carbide (SiC) semiconductor industry is paving the way for next generation power devices, outperforming the equivalent silicon-based devices. But there is still a long way to go as SiC suffers from a high manufacturing costs and low device-yield due to the presence of significant, device-killing, crystal related defectivity [1,2]. Today, several methods are used for defect inspection. For substrates, X-ray topography and destructive methods like KOH are used for defect inspection [3]. Epitaxial grown layers are typically too thin to use X-ray KOH and in addition KOH is not compatible with further device processing. Today there are several surface analyzers available on the market which can detect and classify defects in grown epitaxial layers.

In our work we expand the understanding of defects and their classification, by combining optical surface detection systems, focusing on UV-photoluminescence (UV-PL), with surface voltage mapping. For the UV-PL we used a KLA Candela 8520 and for surface voltage mapping we use a SemiLab FAaST210 tool that utilizes whole wafer biasing to depletion of the surfaces and is completely reversible by capturing the photogenerated minority carriers through illumination [4, 5]. The data is collected on 25 wafers of 200 [mm] 4H-SiC with n-type SiC epitaxial layers. All substates were grown with a layer thickness of 6 [µm] and a doping concentration of $1x10^{16}$ [cm^{-3}], on top of a 0.5 [µm] thick buffer-layer with a doping concentration of $1x10^{18}$ [cm^{-3}].

Experimental Details

In series with optically identified defects, primarily using UV-photoluminescence (UV-PL) imaging, we identify electrical effective defects by using charge based non-contact C-V (CnCV) metrology incorporating the “QUAD” (Quality, Uniformity and Defect) method for whole wafer surface voltage mapping [2,5]. The QUAD technique uses whole wafer corona charging of SiC to deep depletion followed by measurement of the surface voltage using a vibrating Kelvin Probe, see schematic of setup in Fig. 1.

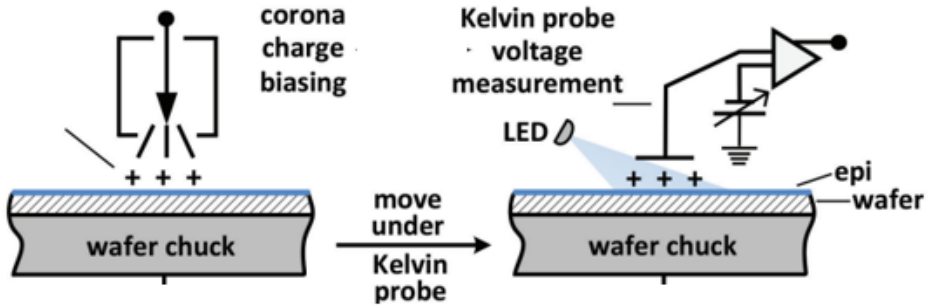

Fig. 1. QUAD part of CnCV210 contained from whole wafer corona station used for biasing and vibrating Kelvin Probe measured surface voltage. Wafer illumination by LED is used for neutralization and removing of deposited charge by capturing of photogenerated minority carriers after measurement leaving SiC epi surface non-invasive. Image adopted from Ref. [6].

Uniform voltage distribution that does not decay after charging is proof of good quality SiC. However, if the wafer contains defects, see UP-PL imaging, Fig. 2 c), these areas can show reduced voltage, see corresponding surface voltage reduction map, Fig. 2 a-b), using QUAD. For instance, the 4th quadrant in Fig. 2 c) shows an increase density of Triangles and MicroPits that overlaps well with a surface voltage reduction up to 4.8 ΔV as seen in Fig. 2 a-b). The depletion leakage current caused by carrier emission from deep levels can result in the neutralization of corona deposited surface charge, leading to a lowering of depletion barrier and the surface voltage.

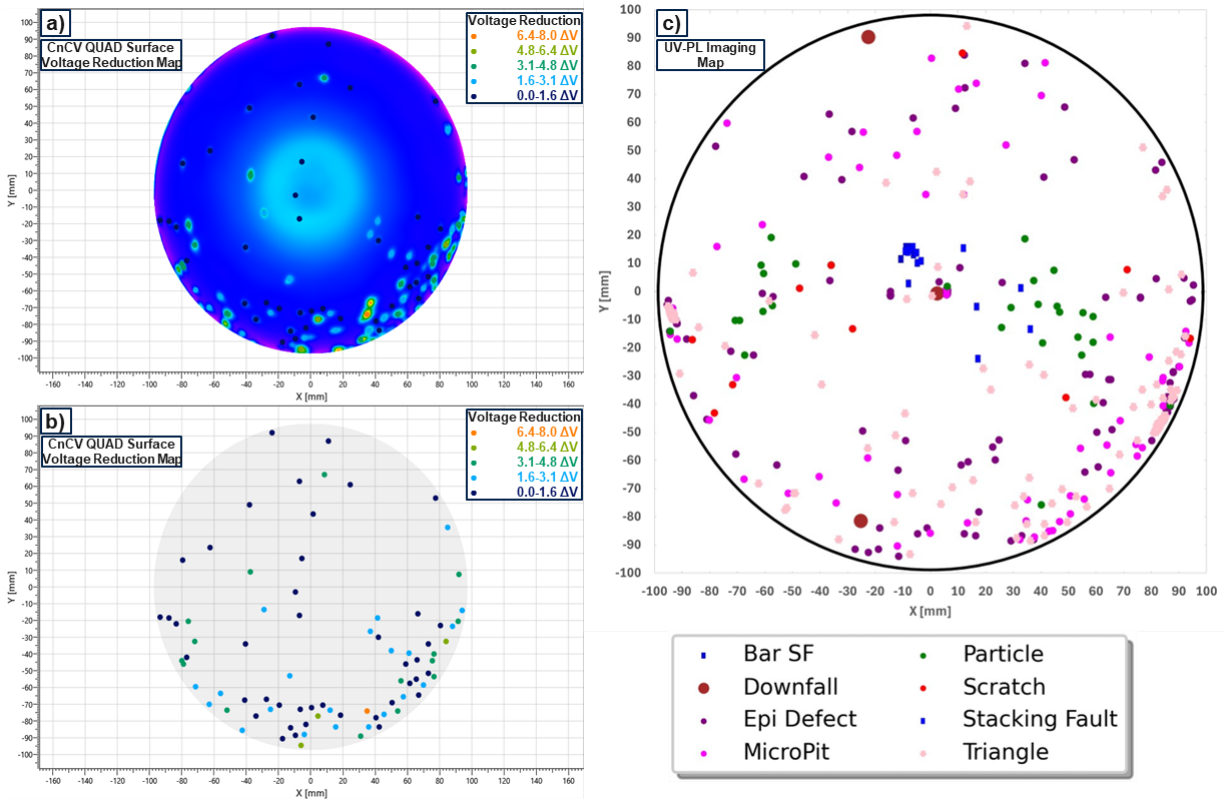

Fig. 2. Example of surface voltage mapping and optical surface inspection of epitaxially grown SiC-layers on a 200 [mm] SiC substrate highlighting a) regions of reduced voltage with corresponding b) clearer view of said voltage map and c) the corresponding optical surface inspection.

Results from the acquisition on the respective tool are parsed and processed to a matching coordinate system, then spatially correlated, in-order to see overlapping of reduced voltage sites and optically captured defectivity. The sweep-radius of the algorithms used for superpositioning is limited to 3 [mm], in-order to compensate for the probe-size in QUAD. Consequently, one reduced depletion voltage site can easily overlap with several UV-PL active defects, as the limitation of resolution is in the probe-size of the QUAD measurement.

Experimental Results and Discussion

The defects in the epitaxial layer of the 25 wafers, that were analyzed with UV-PL and QUAD mapping, are presented in Tab. 1. With a total of 13 390 UV-PL active defects, 5 121 (31.5%) overlap with electrical active sites with respect to QUAD, suggesting that more than half of the defects cause no measurable surface voltage reduction. Most prominent is the Epi Defect, a collection of various unclassified defects found in the epitaxial layer, and Triangles, both comprising more than half of the total defects of which half is electrical active. While a significant number of Particles are found on the surface, most remain electrical dormant. For Scratches, the total number is low but they have the highest electrical activity. It is important to note that there might be several defects overlapping with one QUAD site, resulting in a defect coincidentally appearing electrical active. A Particle on the surface is unlikely to be electrical active but might overlap with a Triangle or Stacking Fault thus, appearing active. All wafers inspected have larger areas without defects and typically have a total usable area (TUA) >95% after epitaxy.

Table 1. Defects and their corresponding classification from UV-PL mapping as well as which overlap with surface voltage reduction sites as seen in QUAD.

Classification	Total	QUAD Overlap	No Overlap	Electrical Active (%)	Electrical Dormant (%)
Bar Stacking Fault	164	54	110	33	67
Carrot	4	0	4	0	100
Downfall	11	2	9	18	82
Epi Defect	4172	1915	2257	46	54
MicroPit	715	257	458	36	64
Particle	1012	205	807	20	80
Scratch	159	101	58	64	36
Stacking Fault	3986	919	3067	23	77
Triangle	3167	1668	1499	53	47
Total & Average	**13390**	**5121**	**8269**	**32**	**68**

The defect detection criteria, ΔV used in QUAD, corresponds to the voltage difference between the reduced voltage points to the uniform surface voltage distribution and can be varied from lowest, 0.05%, to highest (34%). The magnitude of ΔV variation on the QUAD signal in relation to electrical active defects are presented in a Tab. 2 and plotted in logarithmic scale in Fig. 3. The response in QUAD signal is normalized and divided into 5 groups ranging from smallest, green bar, to largest ΔV, red bar, with a total count shown as the black bar. Bar Stacking Faults (SF) is present in more electrical sites than the actual total defect count, suggesting presence of several BSF in one surface voltage reduction site. It is also clear that Stacking Faults, if electrically active, have a significant effect on voltage retention. Micropit, Particle and Scratch give a relatively clear signal from medium to largest even if rather few of these defects are present on the 25 wafers inspected. The triangles are clearly detected with quite an even ΔV distribution. For the Epi Defects most of the defectivity detected have large or largest ΔV signal, but a significant group are also detected with the smallest signal. Even if the same issue with mapping position versus defect position as for triangles are present, we attribute the difference to be related to different defects all classified in the Epi Defect category. Areas without electrically active defects show no depletion leakage, no surface voltage reduction in QUAD signal.

Table 2. Defect overlapping with reduced surface voltage sites and respective ΔV classification.

Classification	Total Defects	Smallest [ΔV]	Small [ΔV]	Medium [ΔV]	Large [ΔV]	Largest [ΔV]
Bar Stacking Fault	54	28	39	39	60	452
Downfall	2	1	0	0	0	1
Epi Defect	1915	156	293	247	687	913
MicroPit	257	18	35	42	98	98
Particle	205	4	20	15	71	144
Scratch	101	11	16	27	33	25
Stacking Fault	919	45	70	84	216	744
Triangle	1668	214	304	338	437	619
Grand Total	**5121**	**477**	**777**	**792**	**1602**	**2996**

Presented in Fig. 4 a) we see the total number of UV-PL active defects that show no electrical activity with the corresponding ratio of electrical active defects in Fig. 4 c). Similarly in Fig. 4 b) the electrically active sites seen in QUAD that do not show an overlap with UP-PL active defects are presented. The most interesting take-away from this is Fig. 4 d), suggesting that nearly all the electrical active sites found by QUAD can correspond with an UV-PL active defect. The implication of this is that QUAD can reliably be used to localize real defectivity that is also seen in UV-PL.

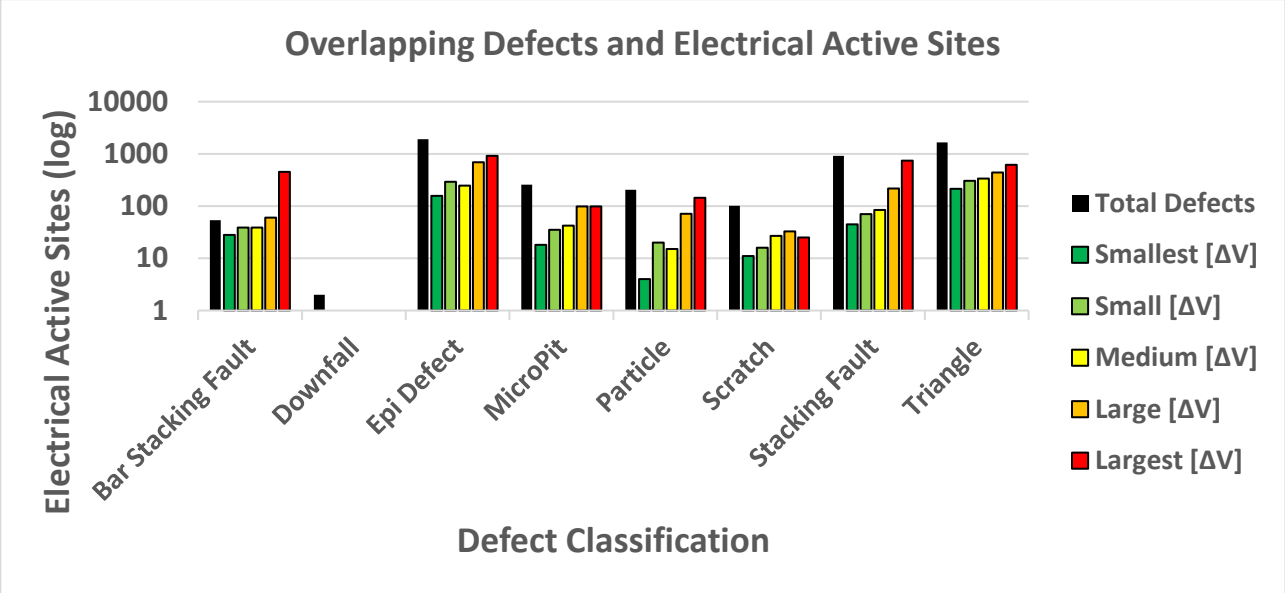

Fig. 3. Logarithmic distribution of defectivity with overlapping voltage leakage sites, see Tab. 1 for corresponding data.

With the data available we conclude the QUAD mapping is the first fast feedback on the epitaxial quality and supports decisions related to the epitaxial growth, like the need for maintenance or possible issues in process or with substrates. The data from QUAD and UV-PL do not correspond one to one and UV-PL gives more detections. This is partly due to the resolution and, generally, maps from the two methods give the same picture. The example shown in Fig. 2, functions as a representation for all 25 wafers, showing dense, and less dense, defective area in top left corner and bottom half, respectively. Next step is to make more detailed studies on the Epi Defect category to see if a further classification can explain the wide electrically active presence, from smallest and Largest Δ V, in QUAD. Another investigation is the QUAD sensor position versus distance from and area/size of the defect. This will help to understand if some defects need a denser mapping pattern or if the current 3 by 3 [mm] grid is sufficient. The QUAD maps will also be compared to device yield when the electrical device results are ready as these 25 wafers will undergo electrical wafer sorting (EWS) to determine the final yield of power devices. These results can be used to see if the electrically active sites seen in QUAD are a good representation of device failure. If EWS results are more in-

line with QUAD, rather than UV-PL activity, then QUAD is fully viable, non-destructive, method to approximate the final device yield.

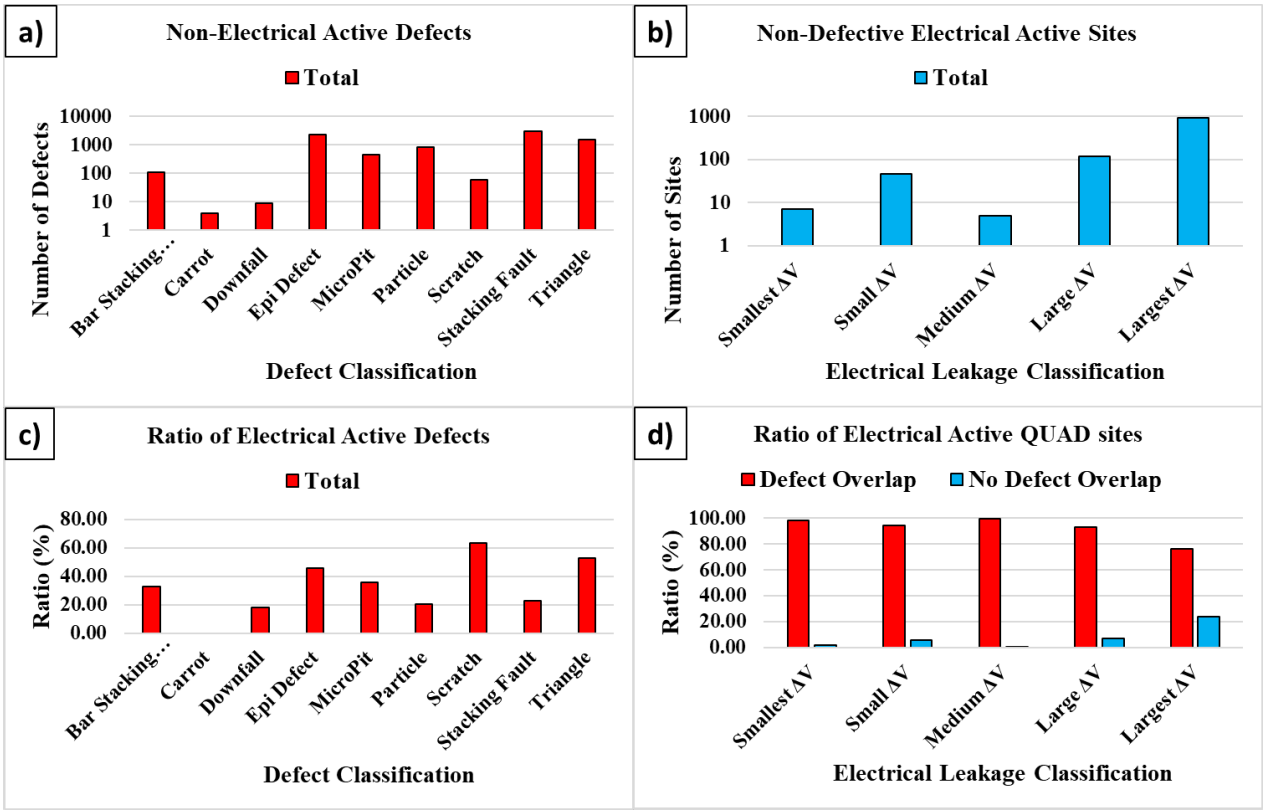

Fig. 4. Logarithmic distribution of a) defectivity and b) electrical active sites without an overlapping defect. Total ratio of c) defects that convert to active sites and d) ratio of active sites that overlap with defects.

Conlusion

The QUAD Voltage map is related to defects detectable with UV-PL and the map can be used as first reliable feedback of electrically active one on the grown epitaxial layer. The QUAD gives clear detection on roughly half of the total UV-PL detected defects and accurately finds defects most found in 4H-SiC epitaxy. A follow-up study using EWS results will be conducted to verify the reliability of QUAD and to determine if it can replace more time-consuming and expensive process steps.

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