Defect and Diffusion Forum
ISSN: 1662-9507, Vol. 434, pp 123-127
doi:10.4028/p-1LgGLQ

Submitted: 2023-09-07
Revised: 2024-03-28
Accepted: 2024-04-05
Online: 2024-08-22

A Study of Process Interruptions during Pre- and Post-Buffer Layer Epitaxial Growth for Defect Reduction in 4H SiC

Tawhid Rana[1,a*], Jun Wu[1,b], Vladimir Pushkarav[1,c] and Ian Manning[1,d]

[1]SK siltron css, 1311 Straits Drive, Bay City, MI 48706, USA

E-mail: [a*]tawhid.rana@sksiltron.com, [b]jim.wu@sksiltron.com, [c]vladimir.pushkarev@sksiltron.com, [d]ian.manning@sksiltron.com

Keywords: Silicon carbide epitaxy, buffer layer optimization, process interruption, basal plane dislocation reduction

Abstract. We perform epilayer growth where the process is interrupted (in situ) during post and pre buffer layer growth at a reduced temperature. Process interrupted during post buffer layer growth demonstrates significant reduction in basal plane dislocation (BPD) at a lower temperature. SIMS study demonstrates that etching takes place during the interruption time. We believe surface treatment of the buffer layer at different etching conditions during the interruption plays a major role in BPD reduction. However, the in-situ interruption, taking place prior to the buffer layer (i.e., on the substrate), does not contribute to the reduction in BPD in epilayer. We believe that the surface effect of interruption related etching on substrate during pre-buffer layer interruption, is not efficient enough to reduce BPD due to the higher doping and higher BPD associated with the substrate. Furthermore, we demonstrate that post buffer layer growth interruption contributes to the reduction in stacking faults in the epilayers. We also attribute this reduction of SF due to the surface etching prior to the drift layer growth.

Introduction

Silicon carbide is a material of choice for applications in electric vehicles due to its high power and high temperature operation capabilities. During SiC epitaxy, substrate defects, such as basal plane dislocation (BPDs) propagate, convert into threading edge dislocations (TEDs), or even annihilate. Ideally, the process is optimized so that a maximum number of BPDs are converted into TEDs [1, 2]. Increasing the BPD conversion efficiency is a subject of high interest since BPDs can adversely impact device performance, especially reliability [3]. Various methods have been used to reduce defect propagation from substrate to epilayers, as described in reference [4].

It is well known that BPD propagation from substrate to epilayer for lower off cut substrates is not energetically favorable during the epilayer growth. Hence, naturally, most of the BPDs are converted into TEDs during epitaxy on lower off cut wafers. The conversion efficiency of the BPDs can be increased further by engineering the surface by various surface treatment methods. The goal of treatments, usually, to disturb the BPD defect point or intersection at the surface to make the BPD propagation even less favorable in the epilayer [5].

A growth interruption technique was reported earlier and demonstrated to reduce BPD in the epilayers [6]. In this technique, the epilayer growth is performed introducing in-situ and ex-situ growth interruption. Here, we further investigate growth interruption at different process steps during the epitaxial process.

Experimental

Epitaxial layers were grown using a commercially available hot wall CVD reactor. 150 mm wafers were selected from the same boules, and experiments were designed to eliminate boule related effects. Wafers were grown in consecutive runs to minimize reactor related process variation with a fixed temperature, pressure, and C to Si ratio. We perform two groups of experiments. Firstly, for our experiments, interruption (Fig. 1, CD) was introduced after the buffer layer step (Fig. 1, AB) and before starting the drift layer step (Fig. 1 EF). Secondly, we interrupt the process prior to starting the

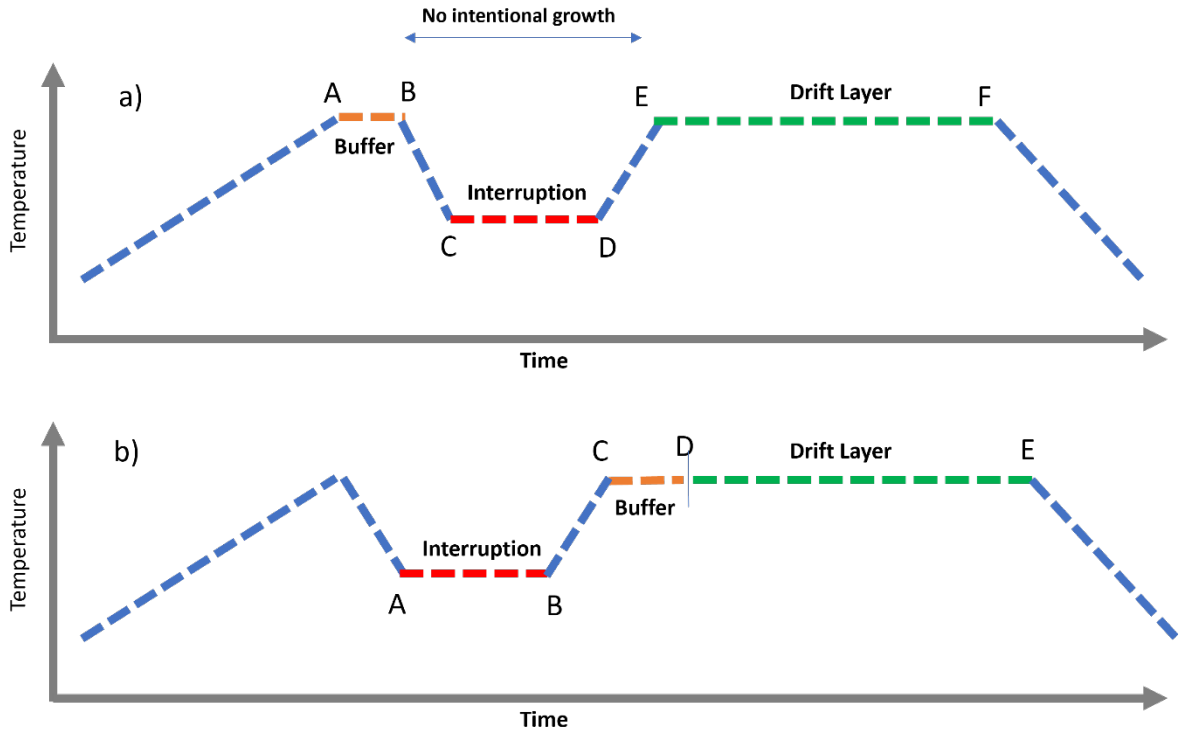

Fig. 1. Growth steps for process interruption experiments. a) Here, buffer layer (AB) and drift layer (EF) are at fixed temperatures, while the growth process is interrupted (CD) after the buffer layer growth is done. b) in this case, the process is interrupted by reducing the temperature (AB) before starting the buffer layer growth.

buffer layer growth (Fig. 1b AB). The flows of source and dopant gases (carbon, silicon, and nitrogen sources) were stopped in the reactor chamber during the interruption. In these experiments, we varied temperature as following: i) epi growth temperature, ii) temperature close to Si melting point and iii) temperature lower than the Si melting point. We keep the duration of the interruption. We use PL ima- ging tool (Lasertec, Sica) for defect comparison. We perform SIMS for the epi layers grown using post

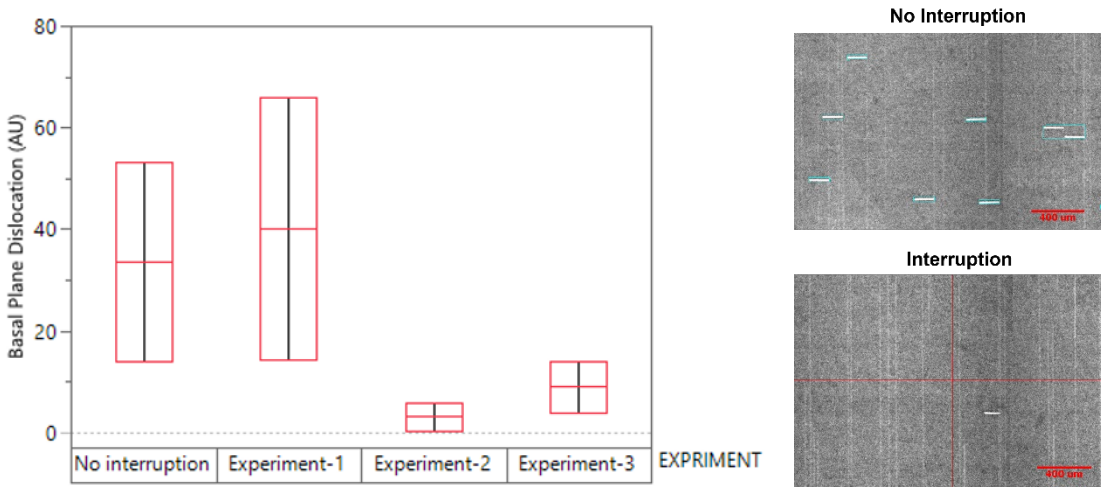

Fig. 2. Basal plane dislocation reduction is observed with a reduction in the interruption temperature (left). BPD density with and without interruption are shown on the right.

buffer layer interruption to investigate the impact of the growth interruption in the epilayer comparatively.

Discussion

Significant decrease in BPDs and Stacking faults (SF) are seen when the process is interrupted after the buffer layer and before drift layer growth (Fig. 2 and Fig. 3). SIMS data indicates etching takes place during the interruption step (Fig. 4). It can be concluded that etching during the interruption is responsible for higher BPD conversion and SF reduction in the epilayer. Interruption at a higher temperature (Experiment-1 in Fig. 2), did not show significant reduction in BPD. However, when the temperature was lowered further (Experiment-2, Fig.2), a significant reduction in BPD was observed. It indicates that temperature plays a significant role in etching during the interruption. Lowering the temperature lowers the etching. We believe that the lower etch rate at lower temperature during the interruption is helpful for BPD conversion rather than higher etch rates at higher temperatures.

Fig. 3. Stacking fault counts are reduced with lowering the interruption temperature (left). A typical PL image of a stacking fault is shown (right).

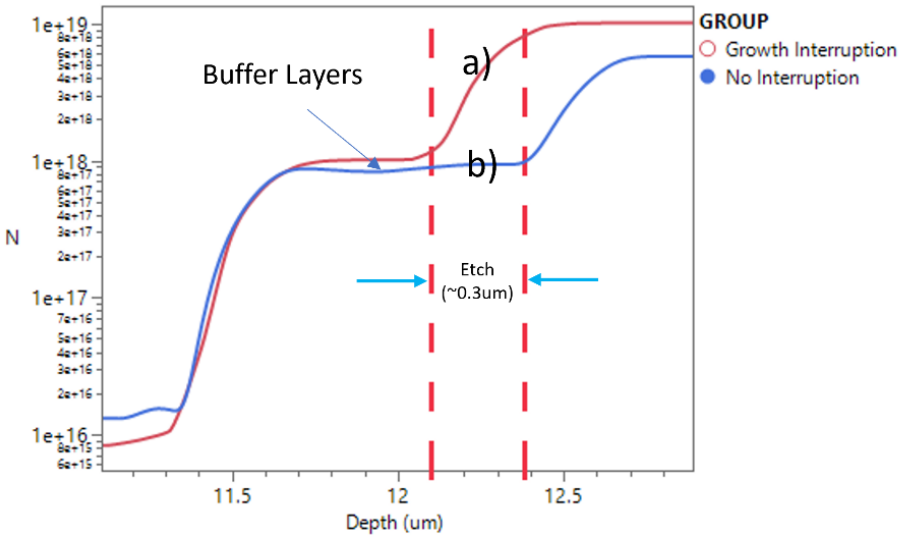

Fig. 4. Depth profile comparison at buffer layer transitions using SIMS for a) epi with post buffer growth interruption, b) no interruption. Buffer layer thickness was found to be ~0.3um thinner for buffer layer growth interruption than the buffer layer thickness without any interruption. This clearly indicates etching takes place during the interruption.

No significant change in basal plane dislocation or stacking fault is seen for the process interruption taking place prior to the buffer layer growth (Fig. 5). This result may be related to the surface condition of the substrates, which is expected to be different than that of the buffer layer. We know that, in general, BPD number in substrates are much higher than the BPD number in the epilayer (e.g. buffer layer). Hence, we believe that the effect of the interruption related etching taking place on the substrate is not efficient enough to passivate higher density of BPD intersections on the substrate. Also, doping concentration in substrate may play a role to change surface etching condition since substrate has significantly higher doping concentrations compared to the buffer layer doping concentration (substrate ~1e19 vs buffer ~1e18 cm^{-3}). Similar result was reported [7] where lower doping rendered higher efficiency in BPD conversion. The conversion mechanism is expected to be similar to enhanced BPD conversion by KOH etching [8]. However, there is no report yet describing H_2 etching contributing to selective etching of BPD [9,10]. We plan to perform more detailed study for the surface comparison for pre and post buffer layer interruptions in future experiments.

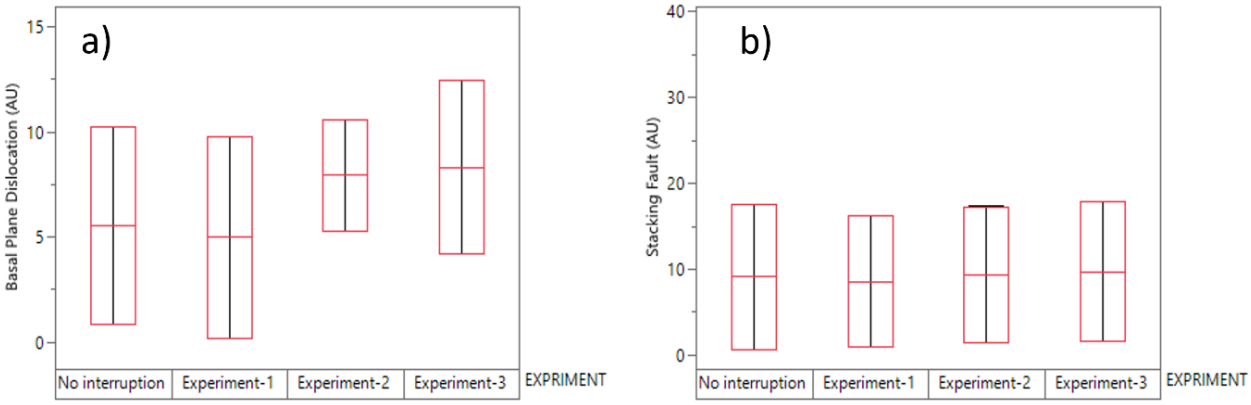

Fig. 5. a) Basal plane dislocation and b) stacking faults are shown for various temperature conditions with interruptions taking place prior to the buffer layer growth.

Summary

We find that post buffer layer interruption by temperature reduction plays a major role in reducing BPD and stacking faults. SIMS analysis shows that, in fact, unintentional etching takes place during the interruption and is the key reason for the reduction BPD and SF. The conversion here is dependent on the temperature of the interruption. We believe lowering temperature changes the surface etching condition, which increases BPD conversion rate in epilayers. However, the exact mechanism of this conversion is not known yet and needs further investigation.

On the other hand, no significant difference is seen for the epilayers grown using interruption prior to buffer layer growth. Here the etching takes place on the higher doped substrate with higher density of BPD compared to the BPD number on the buffer layer surface, where interruption does not play any significant role for BPD reduction in epilayer. Further study will be performed for the surface conditions using various surface characterization methods for both pre and post buffer interruptions, without any drift layer to understand their differences in BPD conversion in epilayers.

References

[1] Z. Zhang and T. S. Sudarshan, Applied Physics. Letters. 87, 161917 (2005)

[2] Z. Zhang and T. S. Sudarshan, Applied Physics Letters. 87, 151913 (2005)

[3] R. E. Stahlbush, K. N. A. Mahadik, A. J. Lelis and R. Green, IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 19.4.1-19.4.4 (2018)

[4] L. Yang, L.X. Zhao, H.W. Wu, Journal of Crystal Growth, 531, 125360 (2020)

[5] Haizheng Song, Tawhid Rana, Tangali S. Sudarshan,, Journal of Crystal Growth, 320, 95 (2011)

[6] R. E. Stahlbush, B. L. VanMil, R. L. Myers-Ward, et al., Applied Physics Letters 94, 041916 (2009)

[7] V.D. Wheeler, B.L. VanMil, R.L. Myers-Ward, S. Chung, Y.N. Picard, M. Skowronski, R.E. Stahlbush, N.A. Mahadik, C.R. Eddy Jr., and D.K. Gaskill, Materials Science Forum, 679-680, 63 (2011)

[8] Haizheng Song, Tawhid Rana, Tangali Sudarshan, Journal of Crystal Growth, 320, 95 (2011)

[9] V. Ramachandrana , M. F. Bradya , A. R. Smitha , R. M. Feenstraa and D. W. Greve, Journal of Electronic Materials 27, 308 (1998)

[10] Tawhid Rana, MVS Chandrashekhar, Tangali Sudarshan, Journal of Crystal Growth, 380, 61 (2013)