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High-Volume SiC Epitaxial Layer Manufacturing - Maintaining High Materials Quality of Lab Results in Production

B. Thomas[1,a*], D. Baierhofer[1,b], F. Staiger[1,c] and C. Bierhoff[1,d]

[1]Robert Bosch GmbH, Tübinger Str. 123, 72762 Reutlingen, Germany

[a]bernd.thomas@de.bosch.com, [b]daniel.baierhofer@de.bosch.com,
[c]frank.staiger@de.bosch.com, [d]christian.bierhoff@de.bosch.com

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Abstract. Typically, research and development (R&D) results of epitaxial layer growth show superior properties of the grown layers compared to high volume results. Layer uniformities are excellent and achieved defect densities are low compared to typical results. In particular, the conversion of basal plane dislocations (BPD) from the silicon carbide (SiC) substrate is in focus to reduce bipolar degradation of p-n-junctions. It is a great challenge to maintain those excellent results in high-volume manufacturing considering all the factors that impact the properties of the epilayer. Thus, quality of the layers, high throughput and low cost have to be assessed to find a compromise between these key factors. In this paper we present results on the growth of epitaxial layers on 150 mm and 200 mm 4° off-oriented 4H-SiC substrates using warm-wall multi-wafer chemical vapor deposition (CVD) systems. Single wafer data of the key epitaxial layer parameters, thickness, doping and defect densities, are compared to batch and lot results, as well as to statistical data of several hundreds of wafers produced. Improvements in wafer-to-wafer (w-t-w) doping uniformity could be achieved for instance by implementation of an on-wafer temperature measurement. Substrate impact on defect levels is shown comparing X-ray topography (XRT) results of bare substrate wafers and defect analysis of epilayers on sister wafers from the same crystal. Statistical defect data and resulting predicted yield loss also show a dependence on substrate suppliers. For the first time we show w-t-w and run-to-run (r-t-r) results of doping and thickness measurements on 200 mm substrates. Also, defect results of epilayers on 200 mm wafers are compared to results on 150 mm.

Introduction

Over the past decade the demand for silicon carbide (SiC) devices has increased dramatically. The transition from a niche market to a steadily growing market especially for automotive SiC based products is in progress. From 2020 to 2026 Yole Group projected a compound annual growth rate (CAGR) of 35% for electric and hybrid electric vehicles [1]. Within this market segment SiC discrete devices and modules are predicted to grow with a CAGR of 73% and 34.6%, respectively, until 2026. Thus, small and efficient SiC devices, e. g. trench metal-oxide-semiconductor field-effect transistors (trench-MOSFETs) in high-power inverter modules, are steadily replacing established silicon technologies [2-3]. The SiC materials business had to catch up in parallel to serve the demand of device manufacturers. The increasing demand for substrates and epitaxial layers led to a fast transition from 100 mm to 150 mm in diameter, which is the most common wafer size today in production. Early adopters have already started with 200 mm in research and development (R&D) and manufacturing.

High quality epitaxial layers with low defect densities are a key factor to ensure the functionality and reliability of SiC devices. Important layer properties like thickness and doping concentration as well as their respective homogeneities, are important for the quality of the epitaxial layers and the final yield of devices. The quality of the epitaxial layers is also strongly dependent on extended surface defects as well as buried crystallographic defects [4-5].

Experimental Procedure

Commercially available 150 mm and 200 mm 4H-SiC [0001]-oriented Si-face substrates with an off-cut angle of 4° towards the <11$\bar{2}$0> direction were used for this investigation. Homo-epitaxial layers were grown on these substrates using multi-wafer warm-wall chemical vapor deposition epitaxy reactors which can run 8×150 mm, 9×150 mm or 6×200 mm wafers per batch. The epitaxial layers were grown at temperatures between 1500 °C and 1600 °C using silicon and carbon containing precursors, hydrogen as carrier gas, and argon for the Gas Foil Rotation (GFR) of the wafer carrier. Nitrogen served as the n-type dopant. All layers were grown on "epi-ready" polished and wet chemical cleaned substrates with low micropipe density.

Wafer-to-wafer (w-t-w) as well as run-to-run (r-t-r) data collection of the epilayer properties as well as statistical data analysis are essential to implement a stable process control. This includes thickness, doping and defect measurements. Thickness was measured by Fourier-transform infrared spectroscopy, doping by non-contact capacitance-voltage and defects were measured by confocal differential interference contrast microscopy and ultra-violet photoluminescence imaging. Device critical defects were extracted from the huge number of all detected defects which still exists in SiC wafers today. Device yield prediction and impact of individual defects was determined by using a so-called "kill ratio" approach overlaying our real device layout with defect maps [6].

Results and Discussion

Key parameters which impact the process are equipment, base material, and human. Equipment parameter logging is the basis for a statistical process control. If equipment parameters are out of control warnings or alarms are triggered. The system can then be put on hold and further processing is prohibited until the warnings/alarms are cleared. If epilayer parameters like thickness, doping or defects are out of their control limits, the manufacturing execution system (MES) is set up to give automated feedback. Problem solving is not always clear in some cases and well-trained personnel must do a root cause analysis (RCA).

Fig. 1 shows a thickness profile of a single wafer with a uniformity of 1.3% for (max-min)/(2×mean). In comparison Fig. 2 shows thickness profiles of a full loaded batch of 8 wafers. The value for (max-min)/(2×mean) of all measured sites increases to 2.5%.

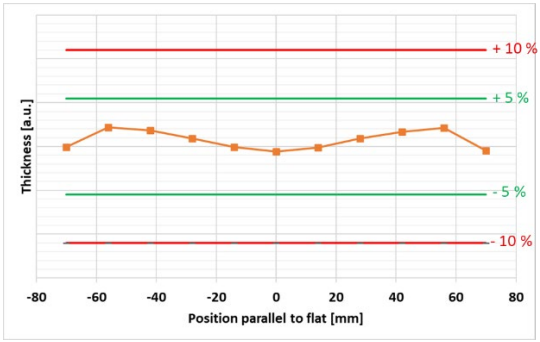


Fig. 1. Normalized thickness profile of a single 150 mm epiwafer across the diameter parallel to the flat ((max-min)/(2×mean) = 1.3%, all sites, 5 mm EE).

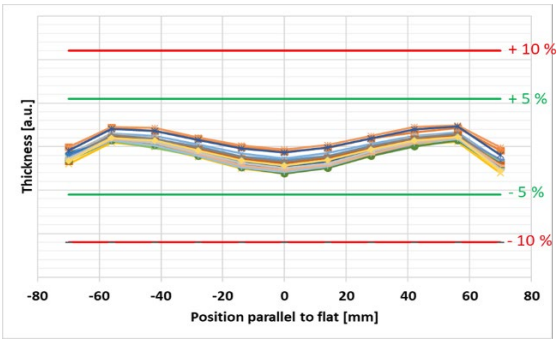


Fig. 2. Typical normalized thickness profiles across the diameter parallel to the flat of an 8 × 150 mm run ((max-min)/(2×mean) = 2.5%, all sites, 5 mm EE).

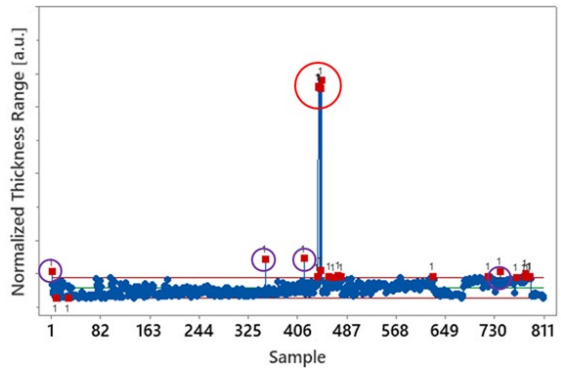


Fig. 3. Thickness range (normalized) with excursions due to outliers (purple circle) and non-rotating wafers (red circle).

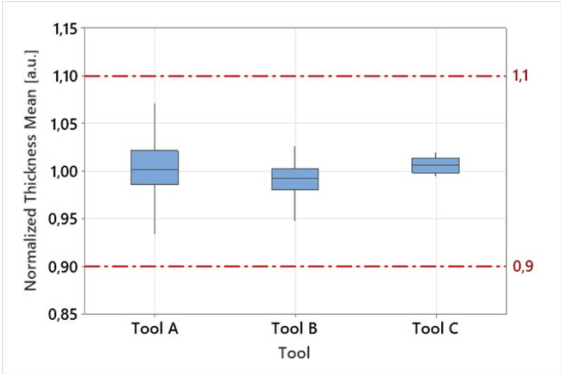


Fig. 4. Example of thickness means for a selection of epi tools (normalized).

For instance, r-t-r and w-t-w data can be controlled by tracking the range. Normalized thickness range data of more than 800 samples are shown in Fig. 3. Cases of thickness excursions are visible and marked by circles. Reasons could be problems of the thickness metrology tool (outlier points measured, marked with purple circles) or the epi equipment, which e. g. had a wafer rotation problem (marked with a red circle). Based on the RCA a decision is needed to avoid scrap wafers in following runs. Furthermore, it is important to achieve similar results in all production tools. For example, thickness matching of a selection of epi tools is depicted in Fig. 4. Deviations of layer thickness are less pronounced in newer tools with optimized hardware configurations which is represented by tool C.

Most important for maintaining a good w-t-w doping uniformity in a batch reactor is the temperature control of each individual wafer during epitaxial growth. The temperature in our reactors is measured on every wafer. This surface temperature is controlled by the system software which then controls the rotation gas flow for each wafer in that way that all wafers in a batch have a similar surface temperature (AutoSat function).

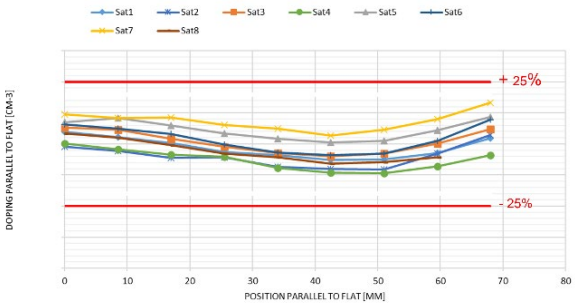


Fig. 5. Doping profiles from center to edge on a batch of 8×150 mm wafers without AutoSat function.

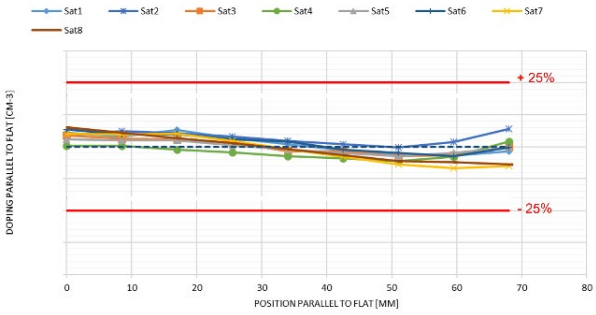


Fig. 6. Doping profiles from center to edge on a batch of 8×150 mm wafers with AutoSat function.

Doping profiles from the center to the edge for an 8-wafer batch is shown without (Fig. 5) and with (Fig. 6) AutoSat functionality. Applying this functionality good doping results for epi lots of 24 wafers (Fig. 7) can be achieved.

Parasitic depositions of polycrystalline SiC in the epi reactor are known to have an impact on r-t-r data. Dependent on the type of reactor, corrections of process parameters are necessary after a certain amount of total deposition accumulated. This can be done either by manual input or by automatic feedback using r-t-r data analysis. As an example, the matching of doping concentration of epilayers grown in reactors with the same configuration within a three-month period is shown in Fig. 8.

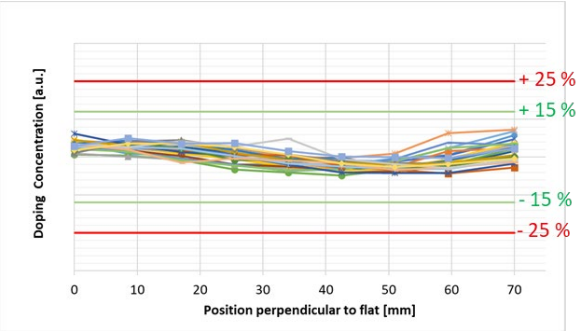


Fig. 7. Typical doping profiles (normalized) from center to edge of a lot of 24 150 mm wafers ((max-min)/(2×mean) =7.5%, all sites, 5 mm EE).

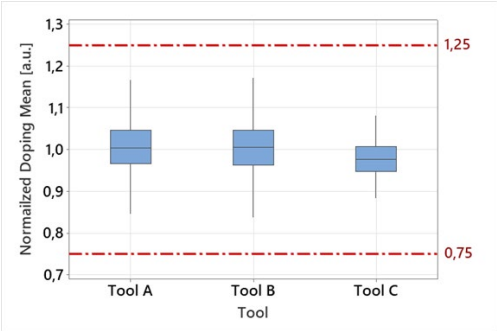


Fig. 8. Tool matching example of doping means (normalized) of selected epi tools of the same configuration for a random three-month period.

Deviations in defect density are most challenging for an RCA. Substrate quality, quality of epi reactor maintenance and process deviations can lead to increased defect levels. Fig. 9 shows a trend of BPD counts with excursions caused by formation of interfacial dislocations (ID) in the center of the wafer (Fig. 9a). This ID formation is found to be related to the substrate quality - mostly stress related due to high concentration of dislocations in the wafer center [7]. Excursions which are caused by the formation of a BPD ring near the wafer periphery are mostly related to epi reactor conditions (Fig. 9b). In this case adjustments to the epi process conditions can be made to avoid the circular BPD formation.

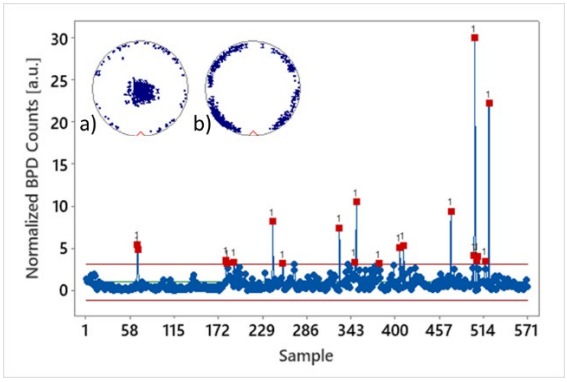


Fig. 9. Example of BPD counts (normalized) and excursions (red squares) caused by a) interfacial dislocations (substrate related) and b) reactor related issues.

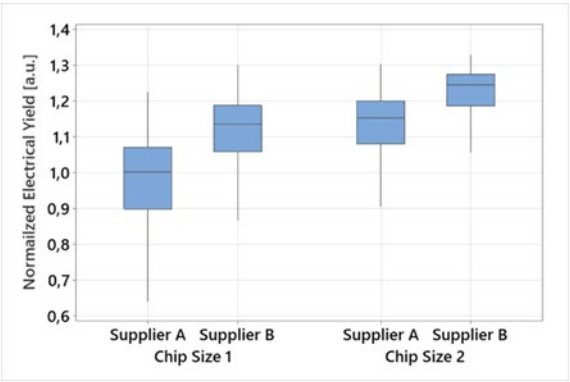


Fig. 10. Normalized electrical yield on wafers from two different suppliers and on different chip sizes (chip size 1 > chip size 2).

Fig. 10 shows a comparison of electrical yield data on substrates of two different suppliers for two different chip sizes. It is obvious that epilayers on wafers from supplier A are yielding lower than on substrates from supplier B. We detected not only a higher density of epi defects on supplier A, but also compared the dislocation densities in the substrates by X-ray topography (XRT). As an example, the BPD density of two typical substrates from both suppliers are shown in Fig. 11. The BPD density is randomly distributed in wafers of supplier A (Fig. 11 a). Substrates from supplier B show a circular distribution with a very low BPD density in the center of the wafer. This could be an indication that the crystal quality and in particular the dislocation density still affects the electrical yield.

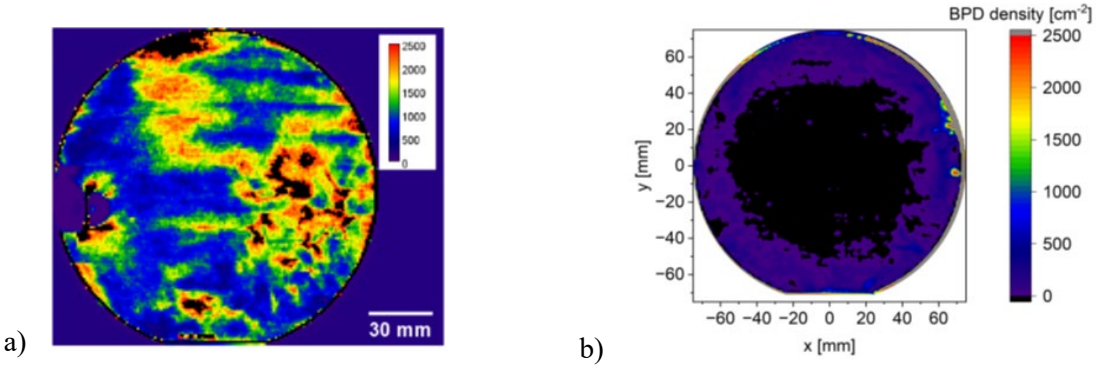


Fig. 11. Typical X-ray topography maps of basal plane dislocation density in substrates of supplier A (a) and supplier B (b).

First Results on 200 mm Substrates

Thickness profiles across the diameter of a 6-wafer batch on 200 mm wafer is illustrated in Fig. 12. The thickness uniformity is 3.9% for (max-min)/(2×mean) and thus by a factor of 1.5 larger than on 150 mm. Fig. 13 shows doping profiles of the same batch as in Fig. 12. A doping uniformity of 9.0% for (max-min)/(2×mean) was achieved. Compared to an 8-wafer batch of 150 mm wafers the uniformity on 200 mm wafers is by a factor of 1.4 larger. Taking these results as start point r-t-r data were investigated as well. Fig. 14 shows the w-t-w and r-t-r data of 15 consecutive runs. It is seen that all data points are within ±10% limits, most of the thickness values are well between ±5%. W-t-w and r-t-r data of the same 15 runs are illustrated in Fig. 15. All data points are within a ±15% range, most of the doping values are even well between ±10%. These results are very promising and would allow to start with manufacturing of devices on 200 mm substrates.

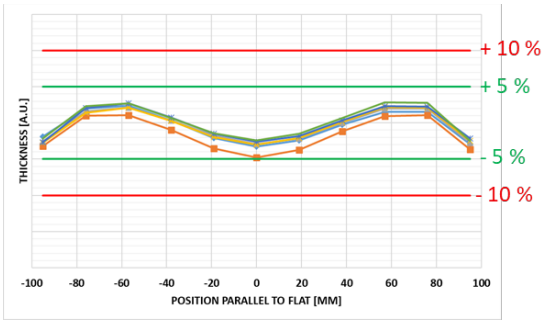


Fig. 12: Typical thickness profiles across the diameter parallel to the notch of a 6 × 200 mm run ((max-min)/(2×mean) = 3.9%, all sites, 5 mm EE).

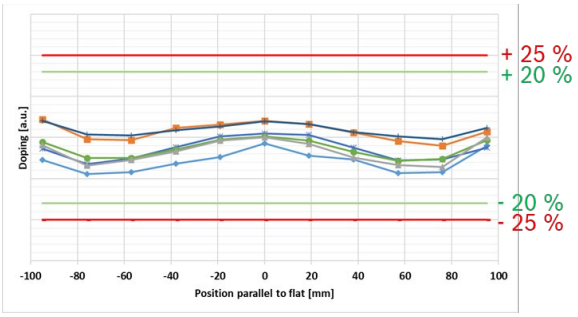


Fig. 13: Typical doping profiles across the diameter parallel to the notch of a 6 × 200 mm run ((max-min)/(2×mean) = 9.0%, all sites, 5 mm EE).

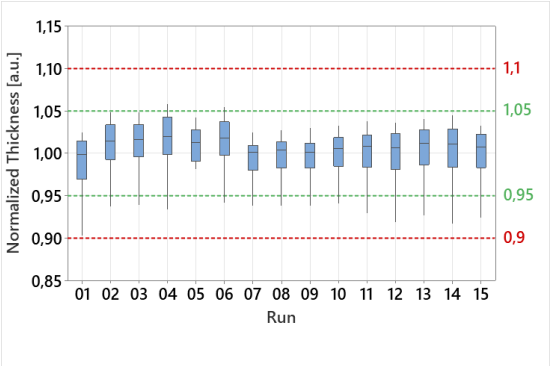


Fig. 14: Boxplot of r-t-r and w-t-w uniformity of epilayer thickness (6 × 200 mm setup, all measured sites included).

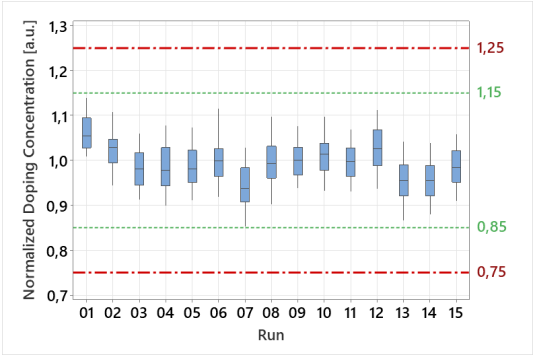
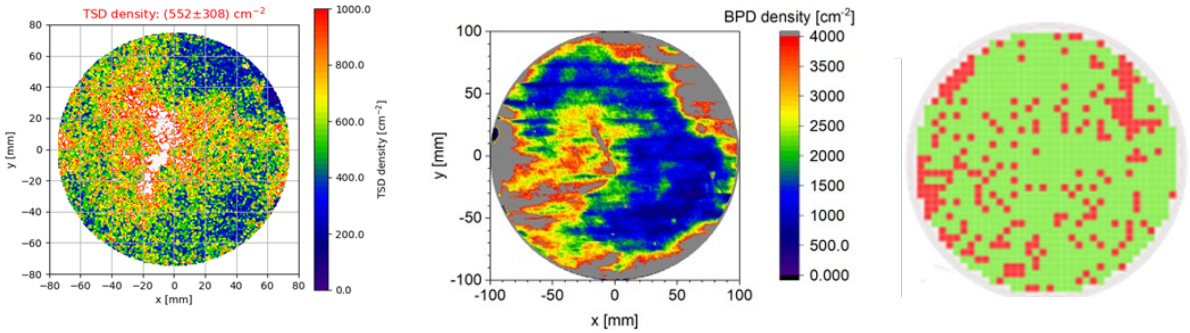


Fig. 15: Boxplot of r-t-r and w-t-w uniformity of epilayer doping (6 × 200 mm setup, all measured sites included).

Defect levels on 200 mm substrates were also improved over the past years by the suppliers. As an example, typical TSD and BPD densities in a substrate of supplier A are shown in Figs. 16 a) and 16 b), respectively. In Fig. 16 c) one can see the resulting epi defect map for a randomly chosen 5×5 mm^2 die size on an adjacent wafer from the same crystal.



a) b) c)

Fig. 16. Typical X-ray topography maps with TSD density (a) and BPD density (b) in a 200 mm substrate of supplier A and predicted yield map (c) (dies with critical defects in red, 5×5 mm^2 die size) on an adjacent wafer of the same crystal as used in a) and b).

Considering all critical defects for our trench-MOSFETs, a predicted usable area or vice versa a predicted yield loss was calculated based on our real device layout (see also [6]). Results of the comparison of epilayers on 200 mm and 150 mm substrates are displayed in Fig. 17. In this graph epilayers on substrates of all suppliers which provided 150 mm and 200 mm wafers are included. One can see that the predicted yield loss is by a factor of 1.4 higher on 200 mm substrates. While statistics is high for 150 mm wafers, 200 mm wafer availability is still limiting the amount of statistical data. But even with the 200 mm data set of at least 100 wafer one can see that substrate quality of 200 mm wafers has improved and will reach 150 mm quality in the near future.

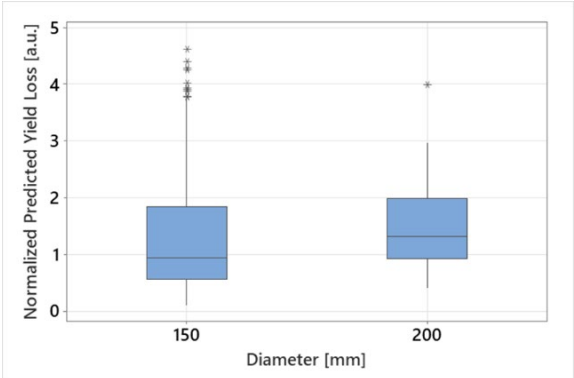


Fig. 17. Normalized predicted yield loss of epilayers on 150 mm and 200 mm wafers (same die size, same suppliers).

Conclusion

This paper compared epi results of single wafer runs with epi batch results and epi lot results. To maintain best in class single wafer results of thickness, doping and defects in epi batches or epi lots various efforts are needed. The comparison of single-wafer runs with batch results and lot results for thickness and doping showed that w-t-w and r-t-r uniformities can be optimized and controlled within the limits of the specification for device manufacturing. Data for thickness, doping and defects are tracked for each single wafer and excursions of these parameters can be detected and tackled. Defect density in epilayers and electrical yield were shown to be still dependent on the substrate quality. A clear supplier dependence was observed for results on electrical yield.

First results on 200 mm substrates were shown. Uniformity data for a batch of 150 mm and 200 mm epilayers were compared and show a slightly worse uniformity on 200 mm wafers by factors of 1.5 and 1.4 for thickness and doping, respectively. Defect density has improved on 200 mm wafers. Considering all critical defects, the yield prediction is still not comparable with state-of-the-art 150 mm quality, but the quality is now usable for pilot manufacturing on such wafers.

Funding

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