

# Non-Destructive Quantification of In-Plane Depth Distribution of Sub-Surface Damage on 4H-SiC Wafers Using Laser Light Scattering

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**Abstract.** The development of non-destructive quantitative evaluation techniques for the in-plane depth distribution of sub-surface damage (SSD) layer induced by mechanical processing of chemical mechanical polishing (CMP) finished SiC wafers is essential to reduce the occurrence of crystal defects during epitaxial growth. Until now, no wafer inspection method has been able to nondestructively and quantitatively assess the in-plane depth distribution of the SSD. This study investigates the correlation between the scattered light intensity measured nondestructively by the Laser light scattering (LLS) method and the SSD depth estimated by destructive inspection using the Dynamic AGE-ing<sup>®</sup> method, a sublimation-controlled etching and growth process, to develop a novel non-destructive SSD inspection method. As a result, it was found that there is an exponential relationship between the scattered light intensity by the LLS method on the bare wafer surface and the depth of the SSD layer that contributes to the formation of in-grown stacking faults (IGSF) during subsequent epitaxial growth. The results show that SiC wafer inspection using the novel LLS method, which introduces this relational equation, enables non-destructive and quantitative evaluation of SSD depth and in-plane distribution.

## Introduction

A quantitative method to evaluate the depth of sub-surface damage (SSD) caused by the machining process that remains on chemical mechanical polishing (CMP) finished 4H-SiC (0001) wafers is essential to reduce the defect density in the epitaxial growth layer. It has been indicated that the SSD is the most significant near the top surface of the wafer and decreases exponentially [1]. The SSD consists of amorphization, microcrack formation, defect formation, and elastic strain, in that order, starting with the most damaged layer. The concept of SSD removal by machining processes originally established in the Si process is that the SSD removal proceeds as the flatness improves through a multi-step grinding and polishing sequence [2]. Since this concept applies to SiC as well, the final SiC wafer finishing quality is guaranteed to achieve a flatness (Ra) of 0.1nm or less, as specified in the wafer specification sheet. However, SiC is a hard and brittle compound material that is difficult to machine, and it has been reported that defect formation layers of less than 100 nm with elastic strain layers of several  $\mu\text{m}$  remain even on CMP-finished surfaces with the sufficient flatness for an epi-ready condition [3, 4]. It is widely recognized that defect-forming layers must be removed because they form defects such as in-growth stacking faults (IGSFs) during epitaxial growth at the epi/substrate interface [5]. Conversely, removal of the elastic strain layer, unlike the defect-forming layer, is generally not considered necessary. Therefore, in the following chemical vapor deposition (CVD) process, it is expected that the adverse effects of the residual SSD can be sufficiently eliminated by removing less than 100 nm by using hydrogen etching in advance.

In our recent study, we demonstrated that a residual elastic strain layer increases the formation of IGFSs and the propagation of basal plane dislocations (BPDs) during the epitaxial growth process on CMP-finished SiC wafers using a sublimation process called Dynamic AGE-ing<sup>®</sup> (DA). The DA

process is a non-contact etching and growth process that utilizes sublimation control and maintains surface flatness independent of etching depth [6]. Substrates with different etching depths ranging from 0.0 to 6.6  $\mu\text{m}$  were prepared by DA etching, and epitaxial growth was performed on them. The results show that the formation density of IGSF and the propagation probability of BPD in the epitaxially grown layer decrease with etching depth. This result provides direct evidence of a previously unanticipated effect of the elastic strain layer negatively affecting the quality of the epitaxial growth layer. Furthermore, our findings indicate that the necessary etch depth to prevent the formation and propagation of defects differs among wafer vendors. Therefore, this finding introduces a critical challenge for the quality control of SiC wafers, underscoring that surface flatness alone is insufficient as a metric of finishing quality, thereby emphasizing the necessity for a non-destructive and quantitative inspection method capable of evaluating SSD depth.

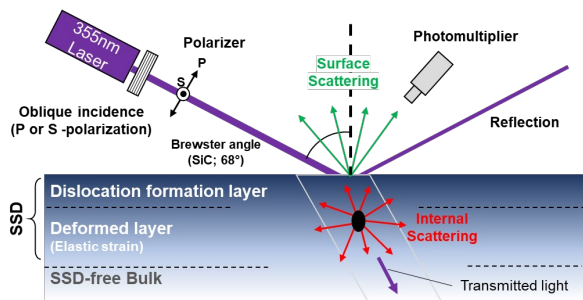
We have recently developed the Laser Light Scattering (LLS) method as a non-destructive technique to qualitatively detect the in-plane distribution of Sub-Surface Damage (SSD) on SiC wafers. This rapid assessment tool, capable of inspecting 6-inch wafers in under 5 minutes and 8-inch wafers in under 7 minutes, utilizes polarized laser light at oblique incidence to measure scattering light intensity. Initial observations revealed variations in scattering intensity across wafers post-CMP, likely reflecting the mechanical processing, including using vacuum jigs during polishing. Notably, a wide variance in scattering intensity among wafers from different vendors and even within batches from the same vendor highlighted the limitations of current manufacturing quality assurance practices in accurately assessing SSD.

However, a direct correlation between the measured scattering intensity on bare SiC wafers and the SSD depth contributing to defect formation during epitaxial growth has yet to be established. To address this gap, our study employs the DA sublimation-controlled process to quantitatively assess SSD depth in wafers inspected via the LLS method. By elucidating the relationship between scattering intensity and the etching depth required to mitigate defect formation and propagation, we have developed a novel, non-destructive, quantitative evaluation method for the in-plane depth distribution of residual SSD in SiC wafers.

## Experiments

A 6-inch 4H-SiC(0001)  $4^\circ$  off-cut wafer after the CMP process purchased from several manufacturers in FY2021 was used as a sample. First, scattering light intensity was measured for these wafers using the LLS method. A schematic of the LLS inspection is shown in Fig. 1. The oblique incidence laser source for measuring scattering light intensity by the LLS method is incident at a near Brewster's angle ( $68^\circ$ ), with a wavelength of 355 nm and polarizations of S- and P-polarization. The

depth of transmission of  $68^\circ$  oblique incidence light through 4H-SiC for 355 nm incident light at room temperature is about 50  $\mu\text{m}$  [8]. In LLS inspection, only scattering light is observed, so the photomultiplier tube, which is the detector, is positioned at an angle where reflection does not directly enter the detector. The scanning method involves moving the optical arrangement in a radial direction while rotating the wafer at high speed. Scattering light intensity values were calibrated to the amplification factor of the photomultiplier tube to evaluate data measured at different photomultiplier tube applied voltages. When using an oblique incidence laser near the Brewster angle of the SiC, the P-polarized laser has more transmitted light components than the S-polarized laser light. Therefore, if the incident laser light is S-polarized, it is expected to provide information near the surface, and if it is P-polarized, it is expected to provide more internal information. The details are the same conditions as in reference [6].



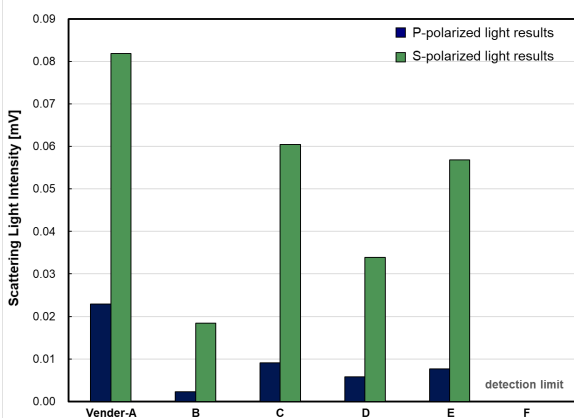
**Fig. 1.** Schematic diagram of 4H-SiC wafer measurement arrangement by laser light scattering (LLS) method

A small sample piece of  $10\text{ mm} \times 25\text{ mm}$  was cut from the portion of the wafer where the scattering light intensity was close to the median value of the wafer as the SSD depth quantitative measurement sample for each vendor. Small pieces cut out for BPD density measurement of purchased substrates were molten KOH etched, and laser microscope images were taken to count BPD etch pits. The Dynamic AGE-ing<sup>®</sup> (DA) method [5], which allows control of surface morphology independent of etching depth, was used for the quantitative SSD depth measurement method for small specimens by sublimation etching and epitaxial growth. Thermal sublimation etching was performed at  $1700\text{--}1800\text{ }^{\circ}\text{C}$ , and the etching depth was controlled to  $0.1\text{--}6.6\text{ }\mu\text{m}$ . Sublimation growth at  $1800\text{ }^{\circ}\text{C}$  was then used to grow epitaxial layers with approximately  $1.0\text{--}3.0 \times 10^{17}\text{ cm}^{-3}$  carrier concentrations. The IGSF density of the epitaxial layer was evaluated by PL imaging using  $313\text{ nm}$  as the excitation light wavelength and a high-pass filter at  $750\text{ nm}$  on the detector side. BPD density was measured by the etch-pit method using molten KOH etching at  $500\text{ }^{\circ}\text{C}$  for 6 minutes. An IGSF density of  $\leq 0.1\text{ cm}^{-2}$  and a BPD conversion ratio of  $\geq 99.9\%$  were selected as the required etching depth to suppress the formation and propagation of these defects. This density and conversion ratio can be chosen arbitrarily. This study chose the above densities and conversion ratio because small pieces of  $10\text{ mm} \times 25\text{ mm}$  in area were used.

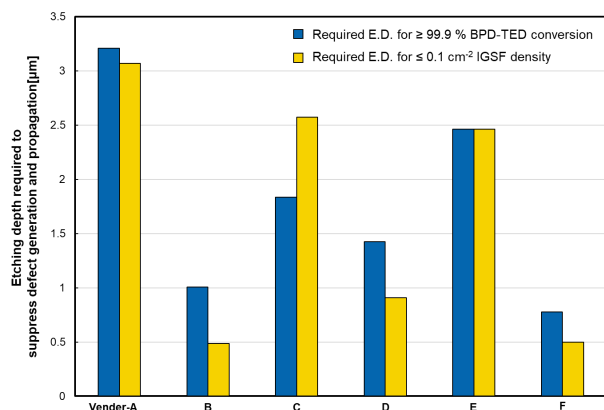
## Results and Discussions

The scattering light intensity of 6-inch wafers purchased from several vendors was measured by the LLS method. Small pieces were then cut from the wafers and sublimation-etched at different temperatures and times to produce samples with different etching depths ranging from  $0.1$  to  $6.6\text{ }\mu\text{m}$ . Sublimation epitaxial growth was performed on these samples, and the defect density of IGSF and BPD was measured using PL and KOH defect detection techniques.

Figs. 2 and 3 show the median scattering light intensity for each vendor and the etching depth required to suppress BPD propagation and IGSF formation, respectively. Fig. 2 shows that the scattering light intensity difference, measured by the photomultiplier tube using the LLS method for each vendor, ranges from 0 (detection limit) to  $0.08\text{ mV}$ . Fig. 3 indicates that the necessary etching depth to suppress defect formation and propagation varies from  $0.5$  to  $3.2\text{ }\mu\text{m}$ , a variation attributed to the processing quality of the machining process.



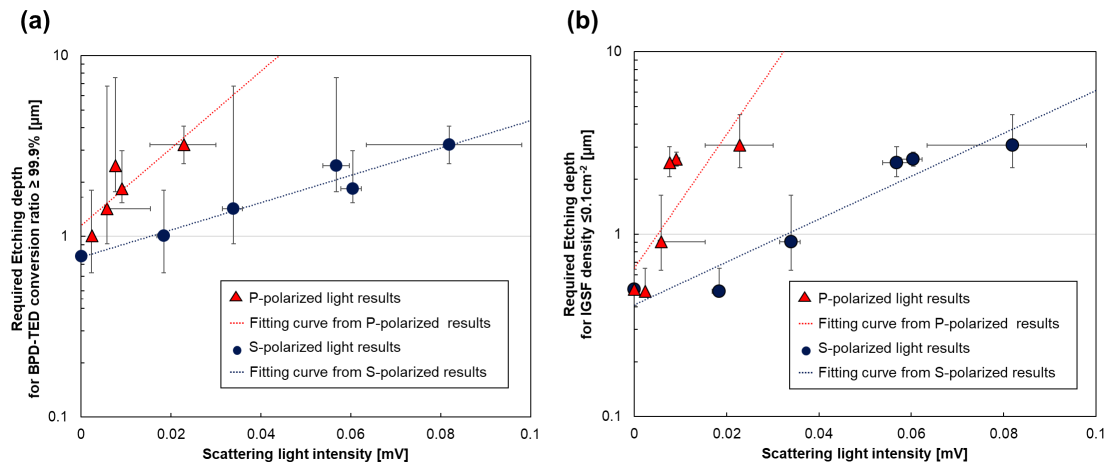
**Fig. 2.** Scattering light intensity results from P-polarization and S-polarization measurements for each CMP-finished wafer from vendors A- F.



**Fig. 3.** Required etching depth to achieve a BPD-TED conversion ratio of  $99.9\%$  or greater and IGSF formation density of less than  $0.1\text{ cm}^{-2}$  during DA sublimation growth on CMP-finished substrates from vendors A -F.

Fig. 4 plots the relationship between the required etching depth for (a) BPD-TED conversion ratio greater than  $99.9\%$  and (b) IGSF density less than  $0.1\text{ cm}^{-2}$  and the median scattering light intensity for P and S polarization measured by LLS after the CMP process. The vertical error bars represent errors derived from the required etching depth fitting curve to suppress defect generation and propagation. In contrast, the horizontal error bars show the first through third quartiles of scattering

intensity across the wafer plane. The etching amount required to achieve a BPD-TED conversion rate of over 99% has a significant positive error. This is because, in this experiment, it is necessary to cut multiple samples from areas where the LLS intensity is close to the median, and there are limitations in terms of area and number. The data suggests that the required etching depth to suppress defect formation and propagation for each wafer can be modeled by a curve that increases exponentially with the median scattering light intensity. Even though, this observation implies an exponential decrease in SSD, as described earlier, and underscores that the LLS measurement evaluates SSD[1]. The vertical error bars also highlight a margin error in the required etching depth to suppress BPD propagation, likely due to the limited measurement points used to determine the necessary etching depth. Some wafers exhibit a scattering light intensity variation of 0.04 mV within the same wafer, indicating processing uniformity within the wafer plane.



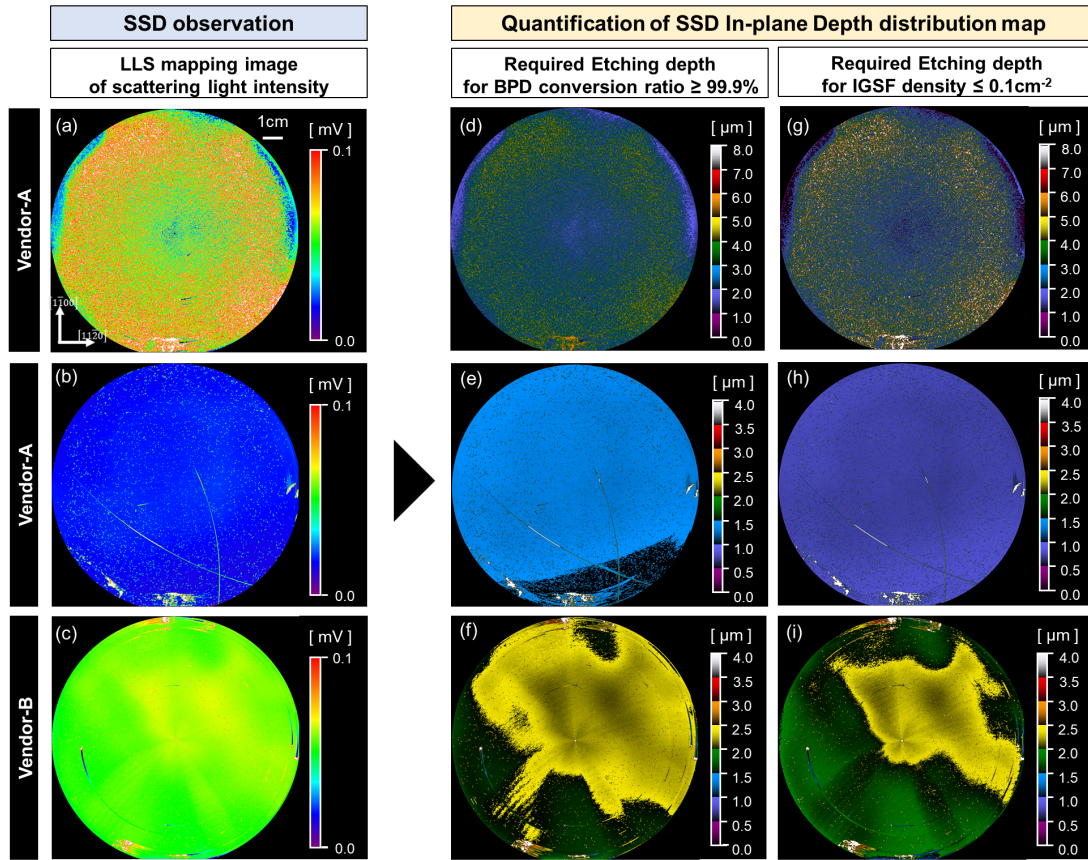
**Fig. 4.** Graph of the required etching depth to achieve (a) BPD-TED conversion ratio  $\geq 99.9\%$  and (b) IGSF density  $\leq 0.1 \text{ cm}^{-2}$  versus the median scattered light intensity in LLS measurements with P and S polarization.

Fig. 5 presents scattering light intensity mapping images of wafers from vendors A and B with S-polarization selection and their conversion to the quantitatively required etching depth in-plane distribution for defect suppression estimated from the fitting curves. Figs. 5 (a), (b), and (c) display S-polarized LLS images of a 6-inch SiC wafer from vendors A and B. The wafer from vendor A in (b) showcases a uniform scattering light intensity in-plane distribution with a median value of approximately 0.02 mV. Conversely, the wafer from vendor A in (a) exhibits a scattering light intensity roughly 3.5 times greater than that in (b) despite both wafers being of the same grade. The wafer from vendor B in (c) has a median value of around 0.06 mV, with an in-plane scattering light intensity deviation of about 40 % from the median. For wafers with these LLS measurements, the required etching depth to suppress defect formation and propagation was estimated from the fitting curves, and its in-plane wafer distribution map was created.

Figs. 5 (d), (e), and (f) show the in-plane distribution mapping images of the required etching depths to achieve a BPD-TED conversion ratio of 99.9 % or higher for the wafers made by vendors A and vendor B. For the vendor A wafer in (e), an etching depth of 0.5 to 1  $\mu\text{m}$  is sufficient for almost all areas, but an etching depth of 4  $\mu\text{m}$  or more is required for the etching depth of the scratches. For the vendor A wafer in (d), an etch depth of 1.5 - 2.0  $\mu\text{m}$  is required near the center, while many areas require an etch depth of 4.0  $\mu\text{m}$  or greater. Vendor B in (f) has a wide area requiring 2.5 - 3.5  $\mu\text{m}$  etching depth. For vendor B wafer, there are certain regions where the required etching depth of 1.5 - 2.0  $\mu\text{m}$  is sufficient and a certain number of regions where 3  $\mu\text{m}$  or more is required, respectively. This result indicates that local SSD depth measurement methods such as transmission electron microscopy and electron backscattered diffraction have difficulty adequately estimating the required etching depth to suppress defect formation and propagation. Figs. 5 (g), (h), and (r) are mapping images of required etching depths to achieve IGSF density  $\leq 0.1 \text{ cm}^{-2}$  for wafers made by vendor A



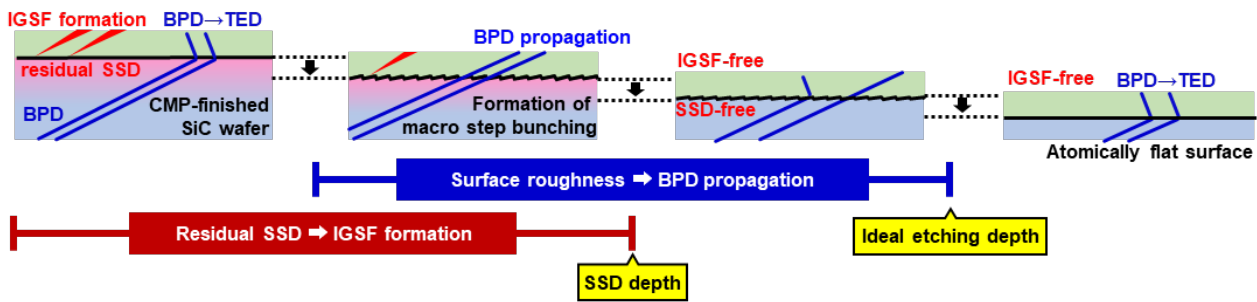
and vendor B. The in-plane distribution of required etching depth per vendor and plane was also confirmed here.



**Fig. 5.** LLS measurement mapping images of scattering light intensity obtained from (a), (b) vendor A, and (c) vendor B, respectively (median values: (a) 0.07 mV, (b) 0.02 mV and (c) 0.06 mV). (d)-(f) In-plane distribution maps of required etching depths to achieve BPD-TED conversion ratios  $\geq 99.9\%$  for vendor A and vendor B wafers, respectively. (g)-(i) In-plane distribution maps of required etching depth to achieve IGSF density  $\leq 0.1 \text{ cm}^{-2}$  for vendor A and vendor B wafers, respectively.

Based on these variations in required etching depths to suppress BPD propagation and IGSF formation, we hypothesized that the SSD intrinsically influences certain defects. Fig. 6 presents a model for defect formation and propagation during epitaxial growth as a function of the etching depth of the SiC substrate. Initially, defects that form after DA growth following the CMP finish maintain surface flatness, facilitating efficient BPD conversion. However, IGSF forms due to the lingering SSD. In DA growth after the initial DA etching phase (etch depth  $\leq 400 \text{ nm}$ ), the SSD remains, leading to IGSF formation and macrostep bunching caused by the SSD, which hinders BPD conversion. After SSD removal, IGSF formation is suppressed, but BPD conversion is obstructed by the residual macrostep bunching caused by the SSD. Further etching is necessary after SSD removal to enhance BPD conversion efficiency. Therefore, the quantitative SSD depth value is the value of the required etching depth to suppress the formation of IGSF.

Eliminating SSD on the scale of a few micrometers poses a significant challenge for pre-epitaxial growth etching techniques. This is because hydrogen etching, widely used in commercial settings, is restricted to an etching depth of less than 100 nm to maintain planarity[5]. BPD-TED conversion is efficient during epitaxial growth after hydrogen etching, but IGSF formation remains unsuppressed. Therefore, the Dynamic AGE-ing<sup>®</sup> method, capable of preserving surface flatness irrespective of etching depth, is crucial for achieving high-efficiency BPD-TED conversion and suppressing IGSF formation.



**Fig. 6.** Model for in-grown stacking fault formation and BPD propagation during epitaxial growth as a function of the thermal sublimation etching depth of the CMP-finished SiC substrate.

## Summary

In this research, a pioneering non-destructive and wafer-level quantitative measurement method for SSD depth in SiC wafers using scattering light intensity is established, showcasing an innovative way to preset the required etching depth pre-epitaxial growth. The study measured SiC wafers of varying LLS intensities and utilized the DA process on SiC substrates derived from these wafers for quantitative SSD depth estimation. An exponential relationship between median scattering light intensity and SSD depth was discerned, enabling the creation of an SSD in-plane depth distribution map of the wafer using only the non-destructive LLS method.

This technological advance transcends the limitations of conventional methods like transmission electron microscopy, offering a more comprehensive evaluation of SSD across the wafer surface and ensuring superior quality and reliability of SiC wafers in semiconductor manufacturing processes. It allows for identifying and managing regions with notable damage that could affect the epitaxial growth, establishing a significant leap towards achieving higher yields of SiC wafer devices. This research underscores the essential role of this novel method in enhancing the accuracy, reliability, and integration of LLS measurements in the manufacturing process, attributing substantially to the production of high-quality SiC wafers.

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