Macro Step Bunching/Debunching Engineering on 4° off 4H-SiC (0001) to Control the BPD-TED Conversion Ratio by Dynamic AGE-ing®

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Abstract. This paper presents an investigation into the surface morphology control of 4H-SiC (0001) wafers cut to 4º off during thermal processing, aiming to suppress the propagation of basal plane dislocations (BPD) into the epitaxial growth layer. Developing methods for debunching rough surfaces with macro step bunching (MSB) using thermal processes removes many of the limitations of the conventional epitaxial growth process. This study presents a surface morphology control method that includes debunching of steps by thermal sublimation etching/growth using the Dynamic AGE-ing® (DA) method. By controlling the surface morphology before and after growth using this method, the dependence of the BPD-threading edge dislocation (TED) conversion ratio on surface morphology was systematically revealed. By selecting the optimal pre- and post-growth surface morphology, a 100 % BPD-TED conversion ratio was obtained for the 10 mm × 25 mm area. It was indicated that an innovative and stable surface morphology control technique using the DA sublimation process could solve numerous technological challenges in various fields.

Introduction

Surface morphology control during thermal processing of 4º off-axis 4H-SiC (0001) wafers is essential to suppress the propagation of basal plane dislocations (BPD) into the epitaxial growth layer. BPD in the epitaxial growth layer on the SiC substrates causes an increase in on-resistance due to bipolar degradation, which is an issue as a factor in device yield reduction [1]. It is known that more than 99 % of BPDs are converted during the epitaxial growth process into harmless threading edge dislocations (TED) with the same Burgers vector and a propagation direction parallel to <0001> [2]. In general, dislocations have strain energy per length and thus have the property of propagating toward surfaces, interfaces, and other crystal defects in the vicinity of the dislocation due to image forces, which are the driving forces that minimize the dislocation length [2]. Therefore, it is suggested that surface morphology control before and during growth that maximizes the image force in the [0001] direction determines the BPD-TED conversion ratio.

Typically, the SiC wafer surface is tilted at an angle of 4° from the (0001) plane to the [11-20] direction to prevent the inclusion of hetero-polymorphs by using step-controlled epitaxy [3]. Therefore, the SiC wafer surface has a step-terrace structure, in which terraces and steps consisting of a basal plane (0001) and {11-2n} facets, respectively, are exposed, reflecting the crystal structure. The minimum step height of SiC is 0.25 nm, which is the height of a single molecular layer. On the other hand, on the 4° off-axis 4H-SiC wafer surface after thermal processing, the smallest step is 1 nm height, which is the height of a full unit cell that is energetically stable [4]. Thus, the smooth surface of a SiC wafer after thermal treatment consists of equally spaced 1 nm height steps. One phenomenon that degrades the surface flatness of SiC wafers is the formation of macrostep bunching (MSB). MSB is a step with a height of several nm or more, and multiple steps are bunched together
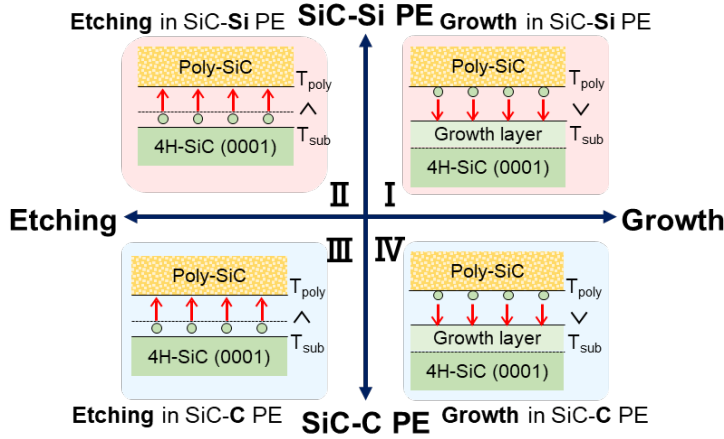
Fig. 1. Schematic quadrant diagram of Dynamic AGE-ing® (DA). The vertical axis indicates the phase equilibrium environment (PE) of SiC-Si or SiC-C, and the horizontal axis indicates the direction of molecular transport.
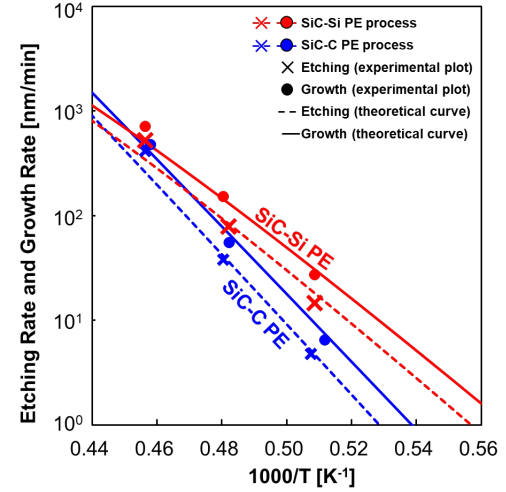
Fig. 2. Arrhenius plots of etching and growth rates. Experimental values for the DA process with and without a Si vapor supply source are plotted. Theoretical curves derived from vapor pressure curves of SiC-Si PE and SiC-C PE are plotted.

to form a single step. Surface roughening due to MSBs during growth increases the density of epitaxial defects [5], and rough surfaces with MSBs of several nm step height adversely affect the uniformity of the oxide layer on the epitaxially grown layer [6].

Researchers have reported several methods to improve the BPD-TED conversion ratio by controlling the image force, which determines the direction of dislocation propagation through surface morphology. Examples include the method of conversion by MSB of 4° off-substrates during epitaxial growth [7] and CMP substrates with flat surfaces of $Ra \leq 0.1$ nm for wafers prior to epitaxial growth [8]. However, there is no systematic examination of the surface morphology before and after growth and the BPD-TED conversion ratio.

The surface morphology before and after growth can be classified as a smooth surface covered by full unit cell height steps and a rough surface formed by MSBs. Therefore, to systematically examine the BPD-TED conversion ratio as a function of surface morphology, it is necessary to control for four patterns of surface morphology before and after growth: rough to smooth, rough to rough, smooth to smooth, and smooth to rough, respectively. However, one of the issues with this approach is the difficulty in surface control of the hydrogen etching and CVD methods, which are the most common vapor phase processes in this SiC device fabrication process. Especially in hydrogen etching, the MSB tends to increase with etching depth [9]. No reports exist of successful decomposing, i.e., debunching, of MSBs once formed in the CVD method or hydrogen etching. Therefore, the formation of MSBs and the ability to maintain a smooth surface during the thermal process while suppressing MSBs and debunching MSBs will solve the problem.

We have developed the Dynamic AGE-ing® (DA) method as a new process to address these challenges. In this method, single-crystal SiC wafers are placed in a closed environment made of polycrystalline SiC and annealed at 1200 - 2100 °C (Fig. 1). The reaction equations for etching and growth in the DA sublimation process are as follows

$$SiC\ (s) \leftrightarrows Si\ (v) + C\ (s). \tag{1}$$
$$C\ (s) + 2Si\ (v) \leftrightarrows Si_2C\ (v). \tag{2}$$
$$Si_2C\ (v) \leftrightarrows SiC\ (s) + Si\ (v). \tag{3}$$

In the DA method, thermal sublimation etching and epitaxial growth can be switched by the direction of the temperature gradient. The C/Si ratio of the polycrystalline SiC closed system can be controlled

by the arrangement of the Si vapor supply source, and the C/Si ratio is stable over a wide temperature range [10]. The solid line in Fig. 2 shows the DA-etching/growth rate calculated from the vapor pressure curve calculated by Toda et al. using thermodynamic calculations based on JANAF thermochemical tables. The blue and red lines are theoretical growth/etching rate curves obtained from thermodynamic calculations of the partial pressure of vapor-phase molecules, including C in the SiC-Si and SiC-C phase equilibrium environments (PE), respectively, and the temperature difference between the source and substrate. The theoretical curve of SiC-Si PE and the experimental values of the DA process with the Si vapor supply source introduced are similar, and the theoretical curve of SiC-C PE and the experimental values of the DA process without the Si vapor supply source introduced are similar. Based on this, the DA process environment was defined as SiC-Si PE with a Si vapor source and SiC-C PE without a Si vapor source. Thus, DA processes can be represented in a quadrant diagram as shown in Fig. 1: I: growth in SiC-Si PE, II: etching in SiC-Si PE, III: etching in SiC-C PE, IV: growth in SiC-C PE.

Previously, we have reported on the DA process for etching 4H-SiC surfaces with a CMP finish to more than 6 μm with a flat surface and epitaxial growth on surfaces with MSBs. However, the DA process has not been systematically investigated in terms of observation of surfaces obtained in environments such as SiC-Si PE and SiC-C PE, stability of the obtained surfaces and conversion rates of basal plane dislocations have not been investigated. In this paper, the dependence of the BPD-TED conversion ratio on surface morphology is systematically investigated by controlling the surface morphology before and after growth using the DA method.

Experiments

For the surface morphology control experiment, n-type substrates of 4H-SiC, which are 4° off toward <11-20> of CMP finish, were cut into small pieces of 10 mm × 10 mm and 10 mm × 25 mm. To investigate the BPD-TED conversion ratio at wafer size, 4- and 6-inch 4H-SiC full wafers were used in the experiments. The Dynamic AGE-ing® (DA) process performed epitaxial growth and sublimation etching on the Si surface of 4H-SiC at temperatures of 1700 - 1900 °C, process times of 10 - 300 min, under ultra-high vacuum, in SiC-Si PE and SiC-C PE environments.

In experiments aimed at observing the diffusion of surface adsorbed atoms and adsorbed molecules in SiC-Si and SiC-C PE environments, 4H-SiC (0001) on-axis substrates were used. Inverted mesa structures of about 250 μm were fabricated on this substrate using pulsed laser processing at 1064 nm. The prepared inverted mesa structures were processed by DA etching under SiC-Si and SiC-C PE at 1500 - 1700 °C for 20 min - 20 h.

Surface morphology was evaluated by scanning electron microscopy (SEM) and LE-ECCI method using SEM and atomic force microscopy (AFM). The etch-pit method using molten KOH at a temperature of 500 °C for 5 minutes was used as the defect detection method, and etch-pits were counted with an optical microscope. Defects on the full wafer surface were detected using photoluminescence (PL): SICA88.

Results and Discussions

Initially, the CMP-finished 4H-SiC substrates were processed under the four conditions of SiC-Si PE, SiC-C PE epitaxial growth and etching shown in the quadrant diagram in Fig. 1. Fig. 3 shows the SEM and AFM mapping images of the SiC surface processed under each condition as a quadrant diagram. From the SEM image of the DA-grown substrate in SiC-Si PE placed in the first quadrant, it can be observed that the terrace width is about 14 nm. This surface indicates that it has a minimum step height of 1 nm, which is the full unit cell height, and the surface roughness obtained from AFM is Ra = 0.15 nm, indicating that it is an atomically flat and smooth surface (Fig. 3 (I)). The SEM image of the substrate with DA etching in the SiC-Si PE located in the second quadrant also shows a step consisting of a terrace width of 14 nm and a surface roughness of Ra = 0.14 nm, indicating smooth surface morphology (Fig. 3(II)).
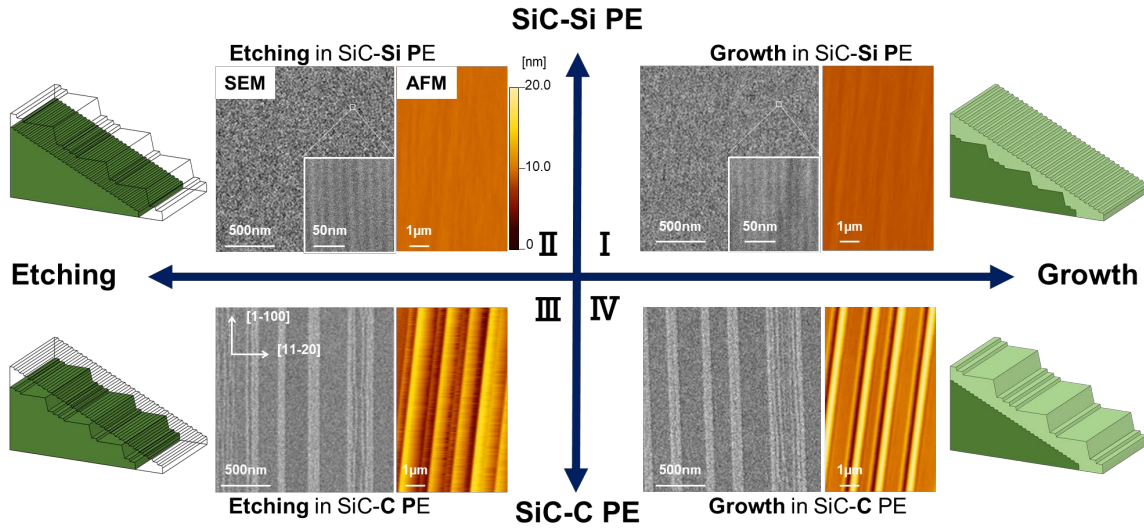
Fig. 3. Surface SEM and AFM mapping images of substrates under SiC-Si PE and -C PE grown and etched by DA method, respectively. Surface roughness of Ra = 0.15 nm for Process I, Ra = 0.14 nm for Process II, Ra = 2.3 nm for Process III, and Ra = 2.6 nm for Process IV. 10 μm × 10 μm area was observed by AFM. The schematic of the steps placed outside represents the surface obtained in each process.

On the other hand, the SEM image of the substrate DA-etched under SiC-C PE placed in the third quadrant showed several MSBs consisting of terrace widths of about 200 nm, clearly observing a surface different from that of the DA-etching of SiC-Si PE. The surface roughness value obtained from this substrate is rough surface morphology, as Ra = 2.3 nm (Fig. 3 (III)). The SEM image of the DA-grown substrate under SiC-C PE in the fourth quadrant shows multiple MSBs with terrace widths of several hundred nm. The surface roughness value obtained from this substrate is Ra = 2.6 nm, which indicates a rough surface (Fig. 3 (IV)). The DA process does not differ in surface morphology between growth and etching but suggests that smooth surfaces can be obtained in SiC-Si PE and rough surfaces with MSB in the environment of SiC-C PE.

We examined whether using SiC-Si PE in the DA process enables debunching of the surface where MSBs have already formed. First, a rough surface with MSBs formed on a 10 mm × 10 mm small piece of 4H-SiC was fabricated by DA growth over a 3 μm SiC-C PE layer at 1800 °C. A surface with a step height of about 10 nm and a terrace width of several hundred nm MSBs is observed on

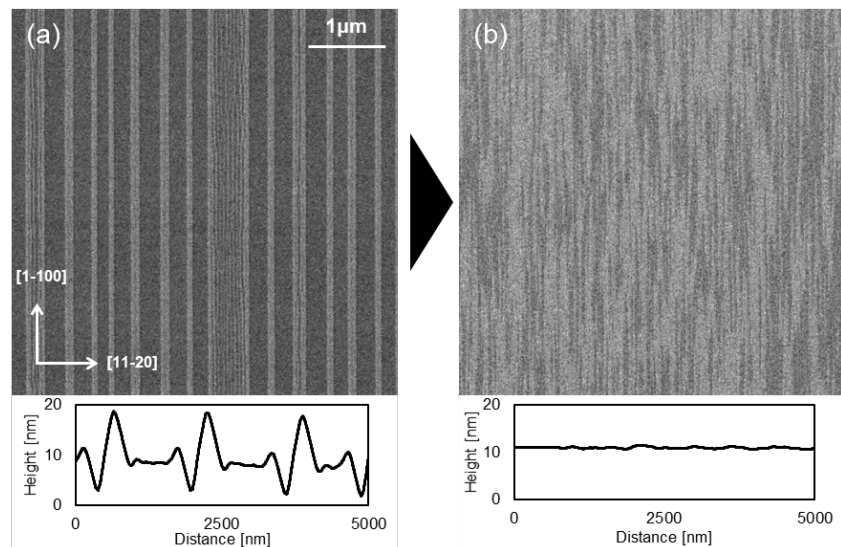**Fig. 4.** Surface SEM images and cross-sectional height profiles of (a) a substrate grown 3 μm by the DA process of SiC-C PE and (b) the substrate subsequently grown 3 μm by the DA process of SiC-Si PE.

the surface after DA growth in SiC-C PE (Fig. 4 (a)). DA growth of about 3 μm on this substrate was performed with a 3 μm SiC-Si PE at 1800 °C. Even though DA growth is performed on the surface where MSBs are formed, a micro-step terrace structure with a step height of 1 nm is observed, similar to the DA process in SiC-Si PE on CMP substrates. This debunching effect was also observed in the DA etching in SiC-Si PE. This effect is the first reported case of successful debunching of MSBs formed on 4H-SiC (0001) at 4° off and is clear evidence that the DA process in SiC-Si PE is an innovative planarization process that can enable debunching of MSBs.

The dependence of surface morphology on the etching depth of the DA process was examined. Six 4H-SiC substrates cut to 10 mm × 10 mm were processed by DA-etching of SiC-Si PE at 1800 °C for 10 - 180 min, respectively. Seven 4H-SiC substrates cut to 10 mm × 10 mm were subjected to DA-etching of SiC-C PE at 1800 °C for 10 - 180 min and 1900 °C for 15 - 30 min, respectively. Fig. 5 shows a variation in surface roughness Ra = 1.4 - 3.5 nm for the SiC-C PE. The AFM images in Fig. 5 (a) and (b) show that the peak-to-valley was about 16 nm at the 1.2 um etch step, whereas at 16 um, the MSB height was reduced to 11 nm. It is suggested that this shape development is expressed as changes in Ra. On the other hand, SiC-Si PE maintains smooth surface morphology and Ra = 0.2 nm or less, indicating that it is not time-dependent. This suggests that in DA etching in a SiC-Si PE environment, a smooth surface with an array of full unit cell height steps is obtained as a stable surface.
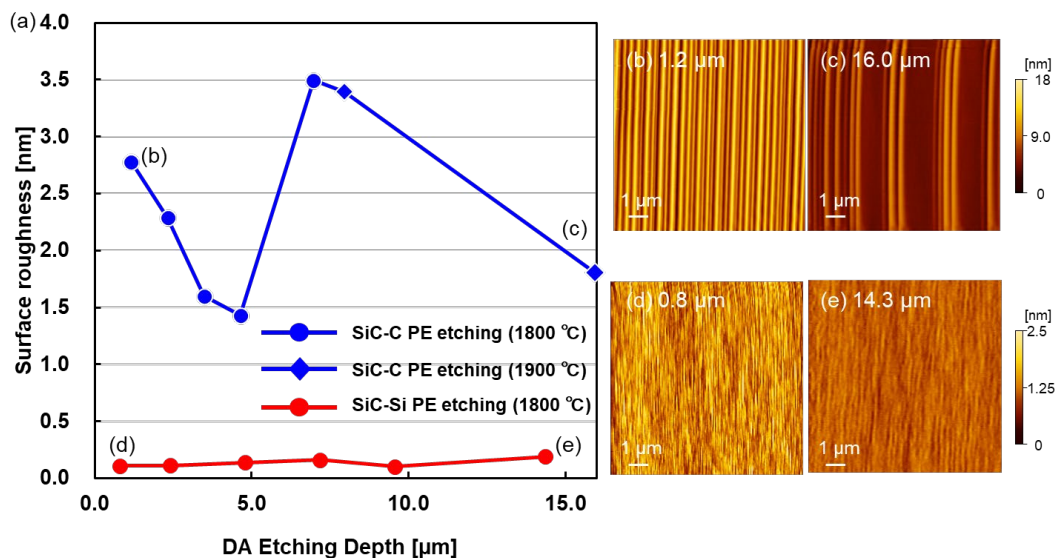

Fig. 5. (a) Graph of etching depth by DA process versus surface roughness (10 μm × 10 μm) obtained by AFM for a CMP-finished substrate. Red and blue lines indicate DA etching of SiC-Si PE and SiC-C PE, respectively. AFM mapping images of surfaces etched with (b), (c) SiC-C PE and (d), (e) SiC-Si PE, respectively.

We observed the surface diffusion of surface-adsorbed atoms and molecules in two DA etching environments, SiC-Si PE and SiC-C PE. Fig. 6 shows the surface morphology of a 4H-SiC on-axis substrate with a dislocation-free region formed by laser processing and DA etching, and Fig. 6 (a) and (b) show DA etching of SiC-Si PE and SiC-C PE, respectively. Concentric surface morphology is observed in the bottom of the inverted mesa structure after DA etching in SiC-Si PE (Fig. 6 (a)). This is evidence that the adsorbed atoms and molecules on the surface interact with the edges of the inverted mesa structure. On the other hand, a dendrite-like surface morphology appears in SiC-C PE (Fig. 6 (b)). This indicates that the surface adsorbed atoms and molecules in the SiC-C PE do not interact with the inverted mesa structure edge; instead, the surface etching reaction proceeds. This result suggests that differences in diffusion modes of surface-adsorbed atoms and molecules due to differences in phase equilibrium environments may enable differences in SiC-Si PE and SiC-C PE environments, as in the results mentioned above.

The surface morphology was controlled during DA etching and growth for the purpose of examining the systematic surface morphology dependence of the BPD-TED conversion ratio. The substrate was cut from a CMP-finished 4H-SiC n-type wafer into 10 mm × 25 mm pieces.

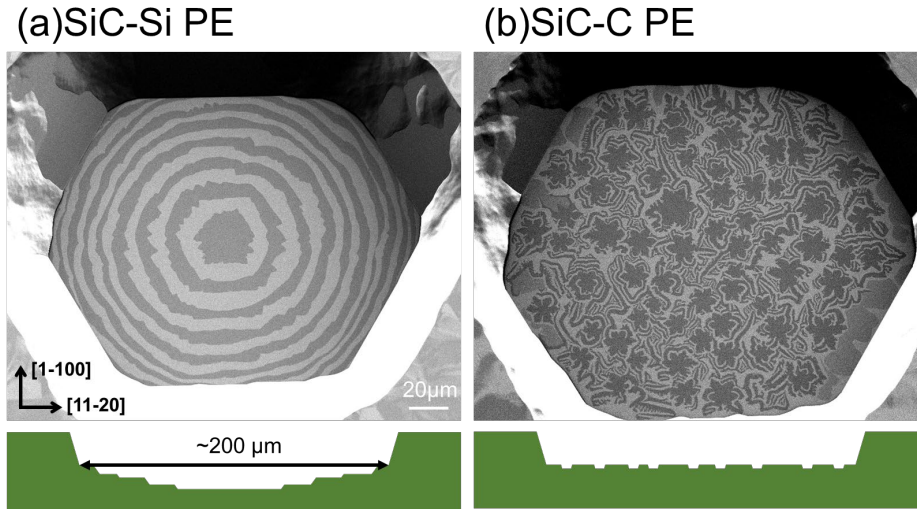## (a)SiC-Si PE   (b)SiC-C PE

Fig. 6. Inverted mesa structures with a basal plane region of approximately 200 μm in diameter were fabricated on on-axis 4H-SiC substrates using pulsed laser processing at 1064 nm. SEM (1 kV-ECCI) and cross-sectional schematic diagrams after etching with (a) SiC-Si PE at 1700 °C for 20 min and (b) SiC-C PE at 1500 °C for 20 h for the inverted mesa structures.

Experiments were performed as follows: DA growth was achieved at 1800 °C for 2 hours and etching for 1 hour. In all samples, etching was done first, followed by growth. Four process flow patterns were performed using SiC-Si and SiC-C PE for DA etching and growth. Next, the BPD density of the DA-grown epitaxial layer was measured by the etch-pit method using molten KOH etching at 500 °C for 6 minutes. Finally, the growth layer was removed by polishing, and the BPD density was measured at the substrate by the etch-pit method to calculate the BPD-TED conversion ratio.

Fig. 7 shows the worst BPD-TED conversion ratio of 31%, which is the result of DA etching under SiC-C PE followed by DA growth under SiC-Si PE (Fig. 7(a)). Under these conditions, the post-etching surface is rough, and the post-growth surface is smooth. The low BPD-TED conversion rate is consistent with the low BPD-TED conversion rate since this condition is contrary to both the
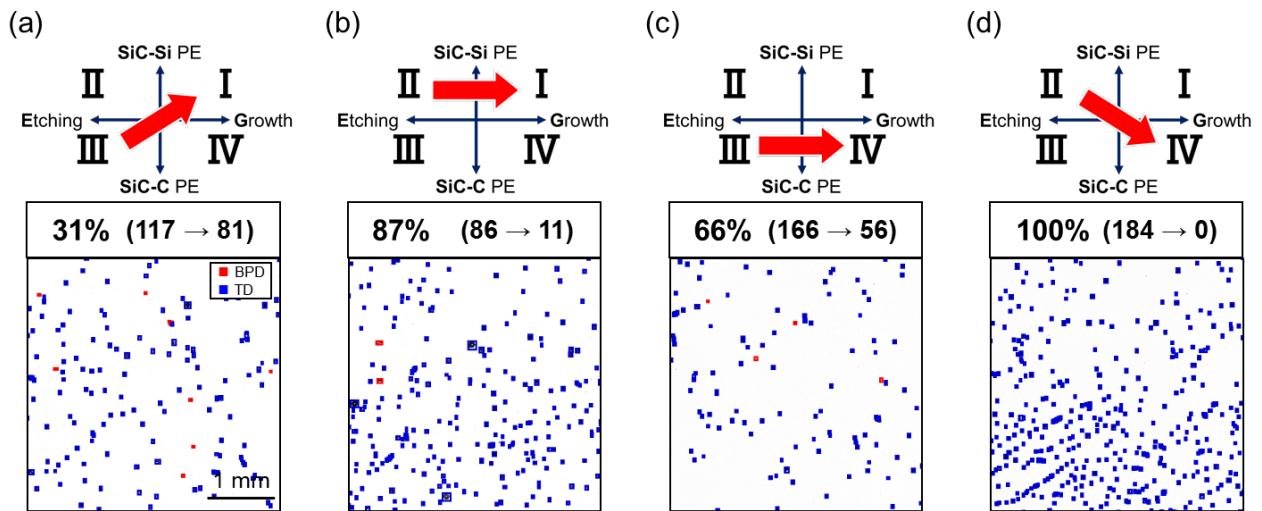

Fig. 7. Optical microscope image of the substrate using the etch-pit method after epitaxial growth. Blue marks indicate threading dislocations and red marks indicate BPDs, respectively. The four quadrants above the optical microscope image correspond to the process conditions described in the four-quadrant diagram shown in Fig. 1. The four-quadrant diagram shows the process flow for each substrate, with the starting point of the arrow representing the etching condition and the ending point representing the growth condition. The numbers above the optical microscope image are the BPD-TED conversion ratio, the number of BPD in the substrate, and the number of BPD in the growth layer in the same area taken from a 10 mm × 20 mm area.

arguments of Kimoto et al. and Myers-Ward et al. Next, the BPD-TED conversion ratio was 87 % when grown under SiC-C PE after etching under SiC-C PE (Fig. 7 (b)). In this case, the post-etching surface is rough, and the post-growth surface is also rough. Comparing Fig. 7 (a) and (b), it is clear that when both initial surfaces are rough, a BPD-TED conversion ratio of about 2.8 times can be obtained by growing to a rough surface. Next, the BPD-TED conversion ratio was 66 % when DA was grown in SiC-Si PE after DA etching in SiC-Si PE. In this case, the post-etching surface is smooth, and the post-growth surface is also smooth. This is the first result showing that only a flat initial surface is insufficient for BPD-TED conversion. Moreover, many epitaxial growth researchers aim for a flat surface after etching and after growth, suggesting that this is not optimal for BPD-TED conversion. Fig. 7 (a) and (c) show that when both post-growth surfaces are smooth, the BPD-TED conversion rate is about twice as high when the initial surface is flat. Finally, when DA etching was performed under SiC-Si PE followed by DA growth under SiC-C PE, the BPD-TED conversion ratio was 100 % (Fig. 7 (c)). In this case, the post-etching surface is smooth, and the post-growth surface is rough. This combination resulted in the highest BPD-TED conversion ratio compared to the other conditions.

Finally, we examined the BPD-free conversion of full 4, 6-inch wafers by etching under SiC-Si PE and then growing under SiC-C PE, the DA etching and growth conditions that resulted in the highest BPD-TED conversion ratio. The wafers after DA etching and growth were inspected by PL, and the BPD density was calculated, the results of which are shown in Fig. 8. By optimizing the surface morphology before and after growth through the DA process, the density of BPD was reduced by more than six orders of magnitude from the BPD density in the bulk wafer over the full wafer. Innovative surface morphology control by the DA process has shown great potential to break through the limitations of vapor phase processes and enable new applications that were not previously thought possible.
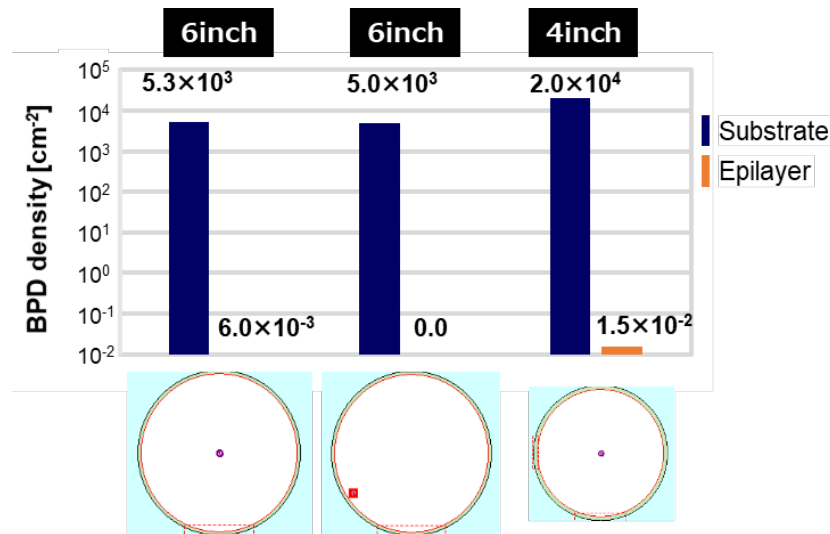

Fig. 8. BPD density detected by SICA on wafers before and after the process for DA etching under SiC-Si PE and DA growth under SiC-C PE. The images below the bar graph are a detection map generated by SICA inspection after DA growth.

Summary

In conclusion, this study provides a comprehensive investigation of the effect of 4H-SiC surface morphology during DA sublimation etching and DA epitaxial growth on the BPD-TED conversion ratio and provides substantial insight for optimizing the surface before and after growth. The experiments showed that utilizing SiC-Si PE in the DA process yielded a micro-step terrace structure with an atomically smooth surface, highlighting its effectiveness in debunching MSBs, a previously unreported achievement. This study showed that the combination of the DA process, SiC-Si PE and SiC-C PE environments, and the DA etching/growth significantly affected the BPD-TED conversion ratio. The optimum conditions, smooth post-etch, and rough post-growth surfaces achieved a

remarkable BPD-TED conversion ratio of 100 % in the 10 mm × 20 mm region. This result provides clear evidence that the BPD-TED conversion ratio can be controlled by surface morphology before and after growth. The debunching effect of MSBs by the DA process demonstrated in this study overcomes the limitations of the vapor phase process and opens up novel applications in the semiconductor industry. Furthermore, the elucidation of the surface morphology-dependent BPD-TED conversion mechanism in 4H-SiC by this study will greatly contribute to the growth and development of this field.

Acknowledgments

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