Defect and Diffusion Forum
ISSN: 1662-9507, Vol. 434, pp 51-59
doi:10.4028/p-yibcT9

Submitted: 2023-09-30
Revised: 2024-04-02
Accepted: 2024-04-05
Online: 2024-08-22

The Role of Defects on SiC Device Performance and Ways to Mitigate Them

Hrishikesh Das[1,a*], Joshua Justice[1,b], Swapna Sunkari[1,c], Petr Kostelnik[2,d], Tomas Novak[2,e], Sara Kochoska[3,f], Daeeun An[4,g]

[1]onsemi, South Portland, Maine, USA

[2]onsemi, Roznov, Czech Republic

[3]onsemi, Munich, Germany

[4]onsemi, Bucheon, South Korea

[a]hrishikesh.das@onsemi.com, [b]joshua.justice@onsemi.com, [c]swapna.sunkari@onsemi.com, [d]petr.kostelnik@onsemi.com, [e]tomas.novak@onsemi.com, [f]sara.kochoska@onsemi.com, [g]daeeun.an@onsemi.com

Keywords: crystal defects, extended defects, classification, micropipe, inclusion, stacking fault, BPD, yield, electrical test, statistics

Abstract. Several defects were analyzed through the manufacturing chain along with their impact on devices. High kill rate of micropipes were seen on both Diodes and MOSFETs as expected. The purity of micropipe detection was found to be affected by the presence of inclusions. Inclusions were successfully sub-classified and separated out from micropipes, based on their location depth from the wafer surface. The effect on devices was found to relate to how deep the inclusion was located, with the ones at the surface having the biggest impact. Various sources of Stacking Faults (SFs) were reported, with Basal Plane Dislocations (BPDs) in the crystal being a major contributor. Higher local densities of BPDs were found to have a more detrimental effect. SFs were sub-classified using the wavelength of each peak. The effect of both overall SFs and each SF sub-type on devices was determined, each sub-type having different effect on the device. Various ways of mitigating the effects of defects and dislocations are demonstrated. Reducing killer defects, SF nucleation probability, and BPDs propagation by epitaxial process optimizations are shown. Resilience up to 3500A/cm^2 against bipolar degradation is demonstrated by using an engineered buffer layer. Process and device design optimizations show high resiliency against crystal and epi defects and dislocations, with improved yield and lower leakage.

Introduction

With the ramp in production and supply of Silicon Carbide devices to the automotive industry, basic understanding of the role of defects on yield and reliability have become paramount. Along with this is the well understood reality that Silicon Carbide will fundamentally have more defects than Silicon. Co-existing with these defects and finding ways to mitigate them at every stage of manufacturing, becomes critical.

In our previous work [1-4], we have demonstrated the link of some of the epitaxial defects to device yield and reliability using a big data approach of analyzing millions of die. We have correlated not just the count of specific defects in the die, but also demonstrated how the actual defective area plays a role in the final device die outcome. There are also other publications which show the effect of the common defects on the device performance [5,6]. In this work, we look at how some defects and features evolve through the process flow starting from the crystal, and finally affect the device die. Further we show how at many of the steps whether in epitaxy or device processing, the effects of many of these defects can be mitigated to have minimal or reduced impact on final electrical performance.

Experimental

SiC wafers were characterized by using various tools at different steps [7]. A Rigaku XRT was used to capture dislocation maps on bare substrate wafers in both transmission and reflection mode. Molten Potassium Hydroxide (KOH) etching was used to delineate the dislocations on the surface, which were auto classified by a Lasertec SICA88 system. Micropipes and Inclusions were detected and sub-classified using a KLA CS8520 system. Multiple channels were used to sub-classify the defects. N-type epitaxial layers with a doping range between $1x10^{16}$ cm^{-3} and $1x10^{18}$ cm^{-3} were grown on 4º off-cut 4H-SiC 150 mm substrates in both single wafer and multi wafer reactors. Extended epitaxial defects including stacking faults were classified using a Lasertec SICA88. Surface and Infra-Red photoluminescence channels were used for the primary classification. Further, Stacking Faults were sub-classified using a ETAMAX MIPLATO system. The wavelength response of each defect was captured, and the defect classified by the peak position of the wavelength. Most of the analysis was done on tens of thousands of planar MOSFET wafers, with a limited number of JBS diode wafers. Each defect category was further split into defect areas that caused an effect on the devices and areas that do not cause any influence, iteratively. Additionally, the affected defective area caused by each defect was calculated for each die. These enhanced attributes were localized and aligned to the affected die and such statistics were collected on millions of die. Where required adjacent sister wafers from the same boule were selected as control wafers to verify the effectiveness of various process optimizations.

Results

Every wafer going into SiC production gets a pre-epitaxy scan to detect and classify the defects of importance, namely micropipes, scratches and other defects. Historically micropipes (MPs) used to be a significant issue for yield loss, however in recent years their density has reduced drastically. To detect them accurately typically a combination of scan channels are needed. After epitaxial growth MPs can split off into multiple screw dislocations (TSDs), and thus making it harder to be detected by the epitaxial layer scan. Fig. 1a shows the micropipe signature and detection, while Fig 1b,c show the dissociation of the MP into various dislocations.

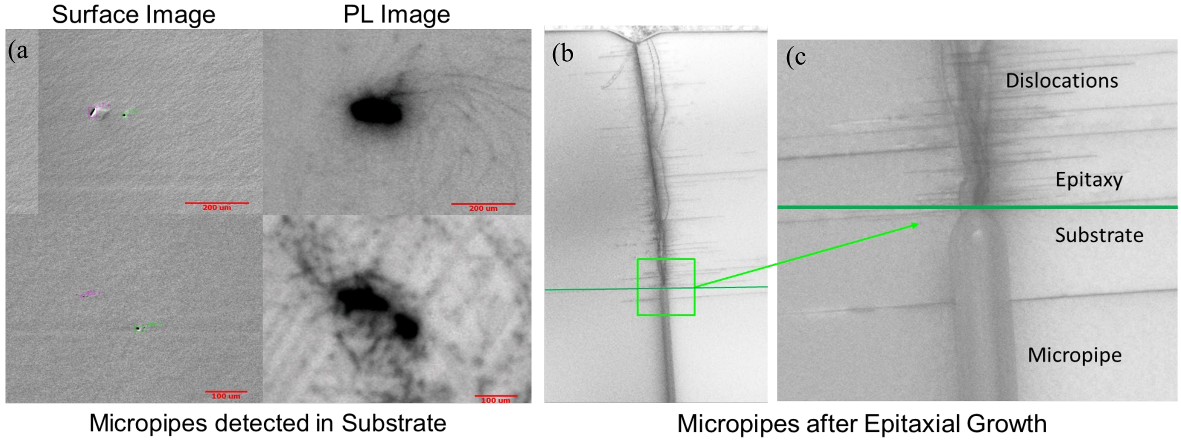

Fig. 1. (a) shows the identification micropipes using both surface and PL channels. Fig. 1b,c shows the TEM of a micropipe splitting into threading dislocations in the epitaxial layer.

Fig. 2 shows the effect of MPs on diodes and MOSFETs. Most of the die affected fail as expected, with high counts or presence of clusters of MPs guaranteeing a 100% fail rate. It is interesting to note that not 100% of die with micropipes fail. After performing failure analysis and tracebacks this is found to be due to two causes. One reason is because some of the epitaxial process can 'fill' in the MP sufficiently and the resultant dislocations do not cause outright device fails. While most of the die with these dissociated dislocations, have high leakage and fail, some of them can still pass the wafer sort tests. The second and more common reason is the fact that inclusions in the substrate get lumped and classified with the MPs. This is because it is quite difficult to separate out the signature of the inclusions from the micropipes. However, to accurately gauge the impact of these defects on the devices, it is important to separate out and sub-classify the different types of inclusions.

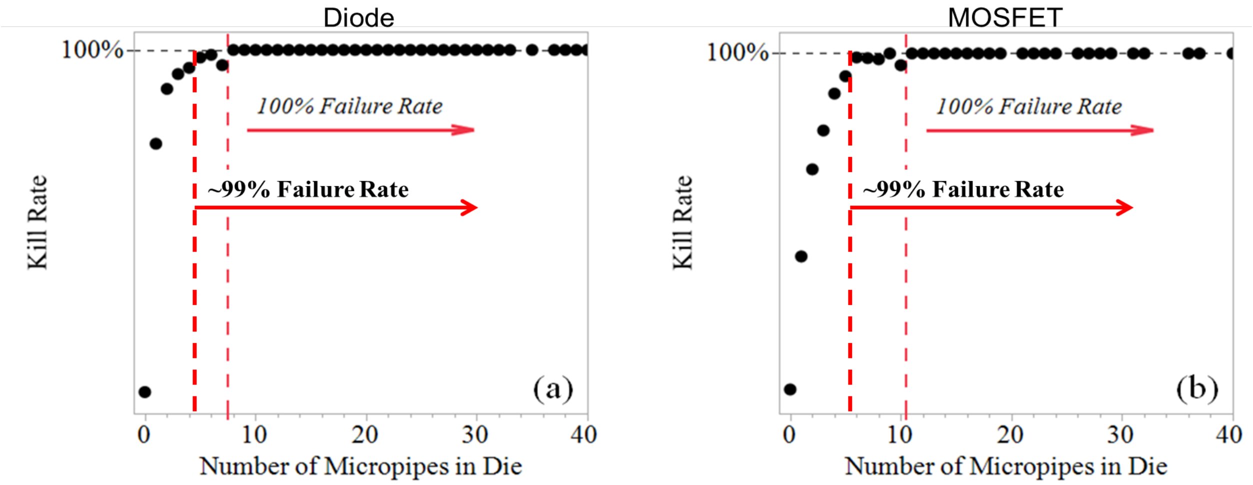

Fig. 2. Shows the kill rates of die as the number of micropipes contained within the die increase. In this case, the diodes are more sensitive than MOSFETs.

Unlike MPs that propagate through the wafers, inclusions are localized spatially within a wafer. Fig. 3 shows that the inclusions can roughly be defined as a function of their distance from the wafer surface. Using this definition, Fig. 3 also shows how these types of inclusions can be separated out from micropipe signatures using the multi detection channels of a KLA 8520. It is important to add that some amount of mixing or miss-classification within the inclusion sub-types is inevitable as the signals represent an almost continuous spectrum. This sub-classification is, however, good enough for analyzing the impact on devices.

In Fig. 4 the impact of the micropipes and the inclusion sub-types in both diodes and MOSFETs are compared to die without any defects. As expected, the micropipes have a very high impact on the devices. As for the inclusions, a strong trend is seen where the surface inclusions have the highest impact on the devices, whereas if the inclusions are located deeper from the surface, the impact reduces. Diodes are more sensitive to the surface inclusions, while the MOSFETs are sensitive to all the inclusions. The separation of the true micropipes from other categories enables screening these defects in high volume production, with minimal overkill and yield loss.

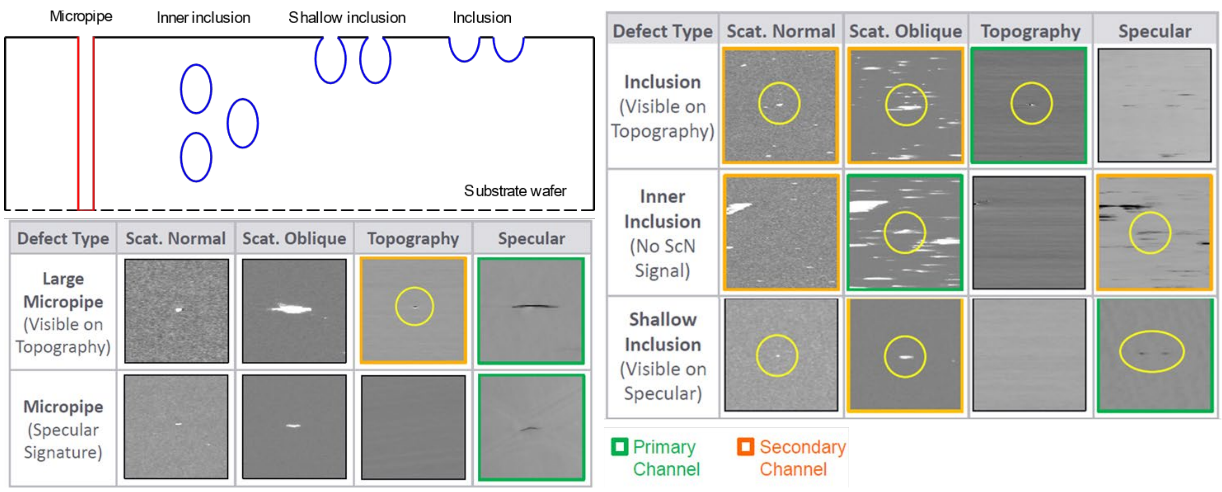

Fig. 3. Shows a scheme to differentiate inclusions based on their position from the surface of the wafers. To implement this in an automatic classification algorithm, various detection channels are used to separate out the defects.

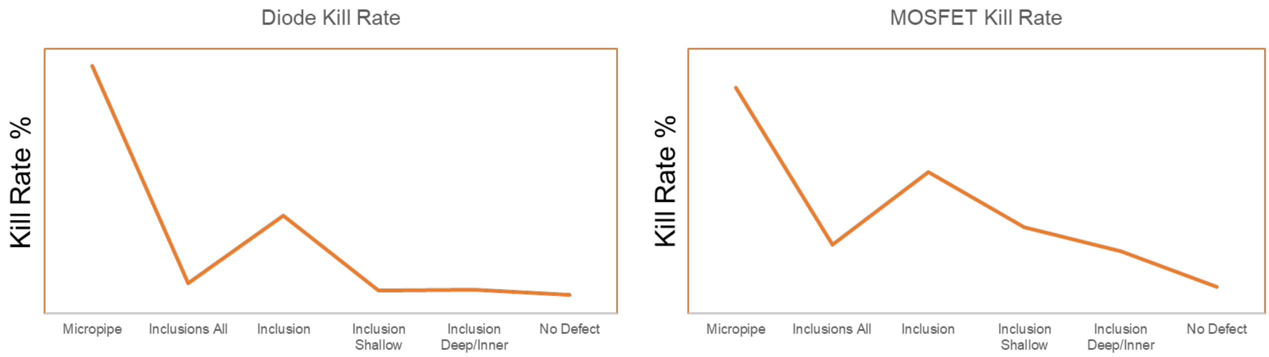

Fig. 4. The kill rates for micropipes and the inclusion sub types are plotted for both Diodes and MOSFETs in relation to dies without any defects. Relatively the inclusions on the surface and closest to it have the highest impact on the devices.

Characterization of the SiC dislocations start at the wafer or boule level using molten KOH etching or X-Ray Topography (XRT) [8,9]. There is a well-established relationship between the surface BPDs revealed by molten KOH etching and volumetric BPDs detected by XRT. Utilizing non-destructive detection of whole wafer dislocations, can help us understand how various defects nucleate from them downstream in the epitaxial growth step. Specifically, here we track the nucleation of stacking faults from substrate crystal defects. Fig. 5a plots the total number of nucleated stacking faults in the epi versus the BPD density in the substrate. A strong dependence is seen across many wafers and boules. It is important to note that in terms of absolute numbers the number of nucleated stacking faults are many orders of magnitude lower that the number of BPDs in the substrate. The nucleation is a probabilistic process depending on the local density of the BPDs. Wafer maps of SFs in the epilayer and BPDs in the substrate are also compared. Across many different underlying BPD density patterns, qualitatively the nucleated SF patterns match. This is shown in an example wafer in Fig. 5b,c. In the wafer maps, the BPD XRT scan has a zero-millimeter edge exclusion while the SF map has a 3mm edge exclusion. The regions of high BPD density correspond to higher SF nucleation in the epi. This insight leads us to conclude that the local higher density of the BPDs is disproportionately more harmful, than the overall wafer BPD density

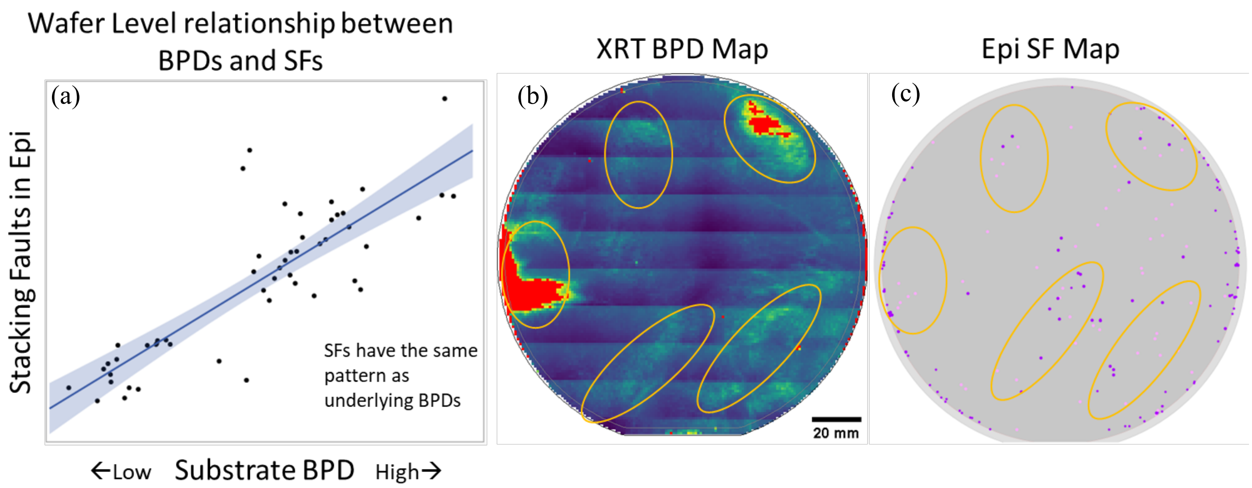

Fig. 5. The relationship between substrate BPD density and nucleated Stacking Faults after epitaxy is plotted and shows a strong trend (a). This is further checked qualitatively on several wafers, where higher SF nucleation is seen in higher BPD density areas of the wafers (b,c).

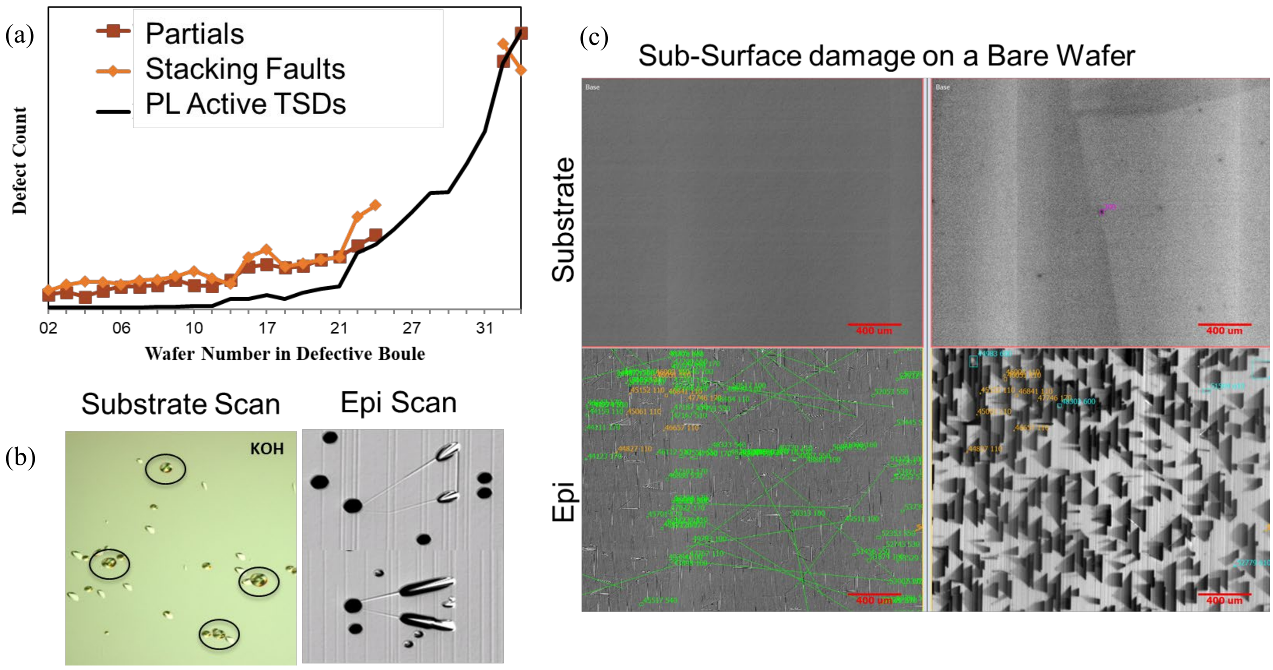

Fig. 6. The stacking fault nucleation can also be related to mixed screw dislocations as shown in (a) and (b). Further SF nucleation can also occur due to sub-surface damage left over from the wafering process as shown in (c).

The nucleation of SFs is not just purely due to BPDs. It is typically the case with everything else being equal. Other sources of SF nucleation can be TSDs, especially mixed type TSDs. This is seen very clearly in a particularly defective boule with a large number of TSDs increasing from one side of the boule to the other. Fig. 6a shows the wafer level trend of increasing SFs as the TSDs (PL active mixed TSDs) go up. Further after molten KOH etching, TSDs are detected at the vertex of the partials and stacking faults (Fig. 6b). Another source of SF nucleation is sub-surface damage left on the wafer pre-epi after the wafering process. Most of the time some of the sub-surface damage can be mitigated by the epi process itself, however severe sub-surface damage can be undetectable and also nucleate SFs after epitaxy as seen in Fig. 6c. This was verified, by regrinding and polishing the epi layer away using a better process. A second epi growth showed no SF nucleation. Sub-surface damage is not always caught even with modern scanning tools, so extra care needs to be taken that there is not any such damage areas left over. Another way of SF formation is relaxation of highly stressed crystal areas after high temp processing. So, there are quite a few ways that SFs can form in the active device regions and affect the device performance.

The die level effect of Stacking faults on both Diode and MOSFET devices was shown in [4]. When doing wafer level analysis, the effect of the SFs are also very clear on MOSFET device wafers. As the SF affected area of the device wafer increases, there is a loss of yield. Since there are many factors (Sub/Epi Killer defects, fabrication defects, parametric factors, etc.) affecting yield, many tens of thousands of wafer statistics are needed to see the clear trend (Fig. 7a). Looking at the die level data, the reason for the yield loss is clear. As the SF density in the die increases the kill probability increases due to increased leakage both on the drain current and the channel (Fig. 7b,c). SFs have only a very weak impact on diodes.

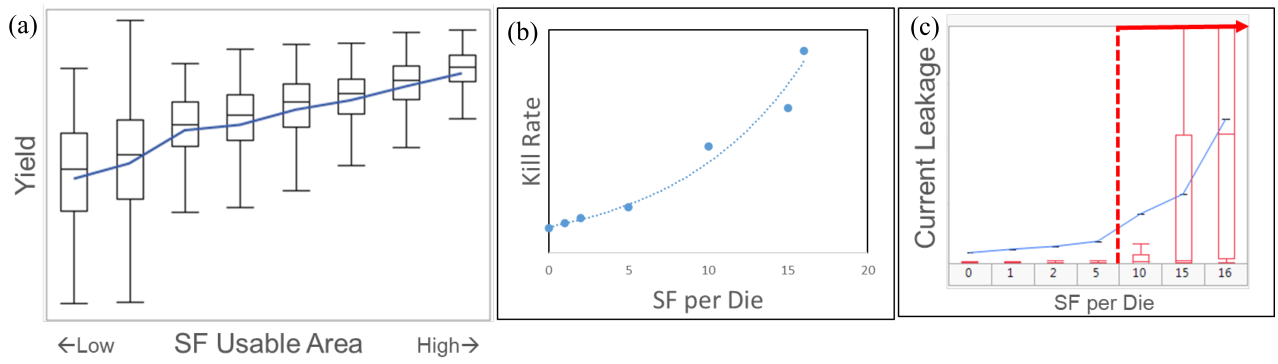

Fig. 7. The impact of the stacking faults is shows as a yield loss per wafer as a relation of the affected portion of the wafer with SFs in (a). A die level analysis shows the increasing probability of the die failing with increasing SF density in the die (b). The failing mechanism is typically increased leakage as shown in (c).

While Stacking Faults have been classified by the major SiC mass-production defect classification tools of KLA and Lasertec very well, sub classification of the type of stacking fault has been only recently introduced by ETAMAX. SFs are sub classified by getting a wavelength response from each SF location and then determining the position of the peak PL intensity. Fig. 8a shows sub-classification of various epitaxial SFs using this scheme. It is interesting to observe that different substrate vendors have different portions of the SF sub-types as seen in Fig. 8b. We can infer different nucleation probabilities based on the base distribution of crystal defects for each vendor. While the overall effect of SFs was shown earlier, the effect of each SF sub-type is not very well understood. A few wafers are run through the full MOSFET device loop. Fig. 8c shows the impact of the various SF sub-types on the device. This shows that each sub-type can have different impact to the device performance. This can be used to target the exact source of the SFs or the conversion probability to a more benign SF type if possible. Since these statistics are from a limited number of wafers, a larger data set is needed and will be analyzed in the future to make a more definite conclusion.

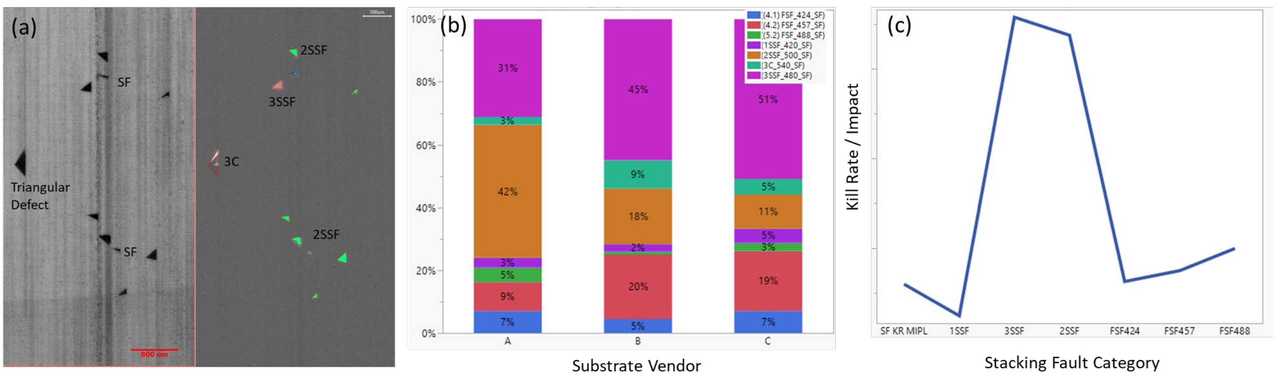

Fig. 8. Sub-classification of Stacking Faults based on the position of the peak wavelength is shown in (a). Various substrate vendors show different distributions of SF sub-types after the same epitaxial process (b). The impact of the SF sub-types on MOSFETs is shown in (c).

Defects evolve, transform, and are added at each stage of the production process from crystal growth, wafering, epitaxy, and device fabrication. At each stage, optimizations can reduce defects or convert them into less harmful variations, or even deactivate them as far as effect on devices. One very effective step for reducing and transforming defects is epitaxy. Modern enhancements in reactor design have largely reduced downfalls. In addition, optimizing the epitaxial processes can further reduce other killer defects like nucleated triangular defects. This is shown in Fig. 9a using controlled wafers from the same boule (sister wafers). At this point traditional epi killer defects have become a much lower part of the yield fallout for devices. As seen earlier SFs primarily nucleate from crystal defects. However, epitaxial process can shift the nucleation probability to some degree. Fig. 9b shows three different epitaxial processes on adjacent sister wafers, that show reduced SFs in the wafers. Though this helps to a limited extent, the major improvement has to come from the crystal quality.

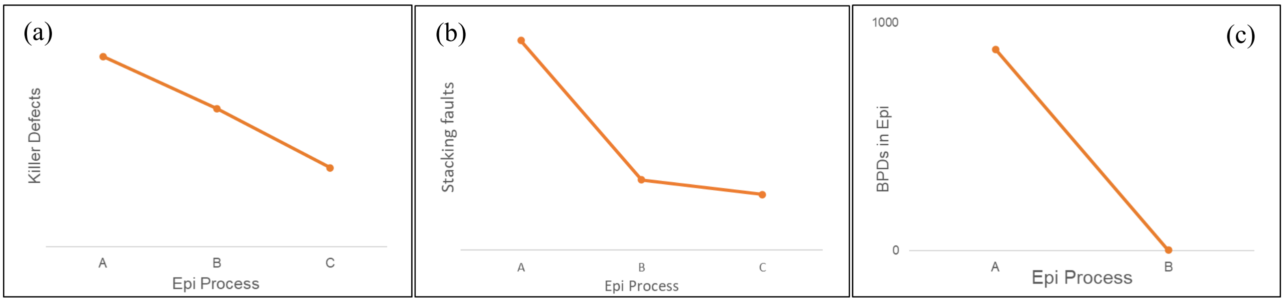

Fig. 9. Shows how various epitaxial processes can help reduce nucleation of (a) Killer triangular defects, (b) of stacking faults on wafers having the same density of BPDs, and (c) suppress propagation of BPDs to zero in the epitaxial drift layer.

Basal Plane Dislocations can be fully mitigated in the epitaxial layer and converted to TEDs. This has largely stopped being an issue for modern epitaxial layers below 50µm. This is shown in Fig. 9c using an optimized buffer layer. Effectively there are zero BPDs in the epitaxial layers. However, there is still a large density of BPDs in the substrate or within the buffer layer where they had converted. Under high enough minority carrier injection reaching these BPDs in the substrate or the buffer, bipolar degradation is seen [10]. There have been many ways to reduce this effect, by lifetime engineering of the epi drift or buffer layers, or recently also by hydrogen implantation for engineered substrates [11]. Fig. 10a shows the pulse body diode stress applied to MOSFETs with two different epitaxial buffers. Both the buffers result in zero BPDs in the epitaxial drift layer. Buffer "B" is clearly much more resilient to minority carrier injection and sees a response only at an extremely high current density of 5000 A/cm^2. Fig. 10b shows the degraded die showing the expanded stacking faults.

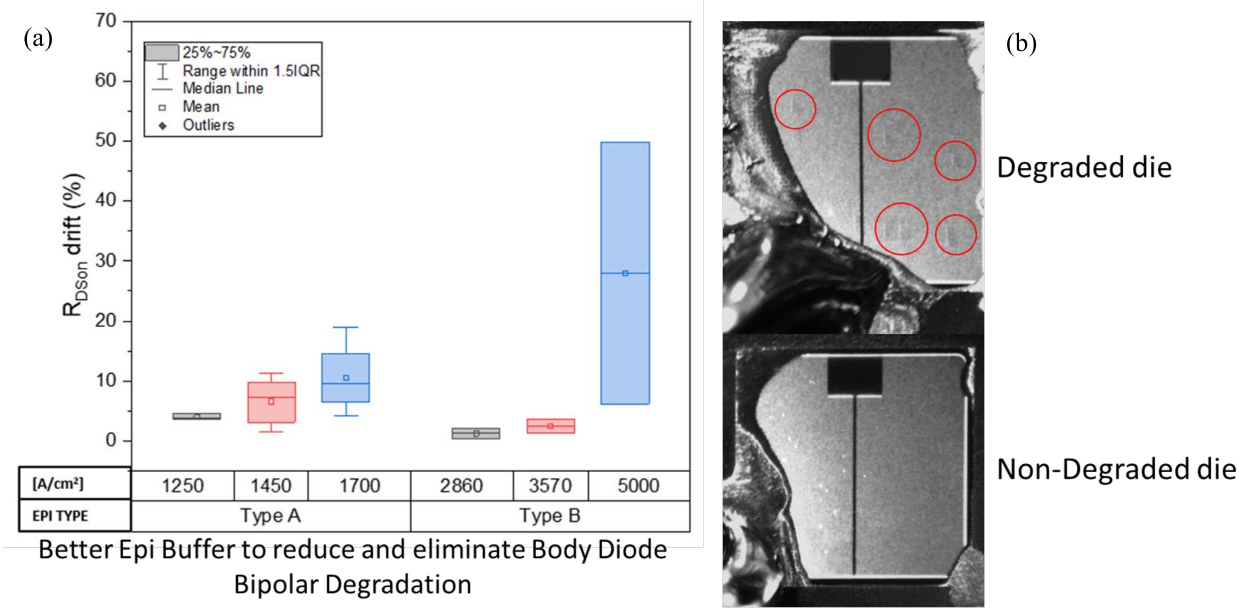

Fig. 10. (a) Body diode stress of normal BPD free epi (Type A) and an engineered epi (Type B) showing higher resiliency. The SF expansion in the degraded vs non-degraded die is shown in (b).

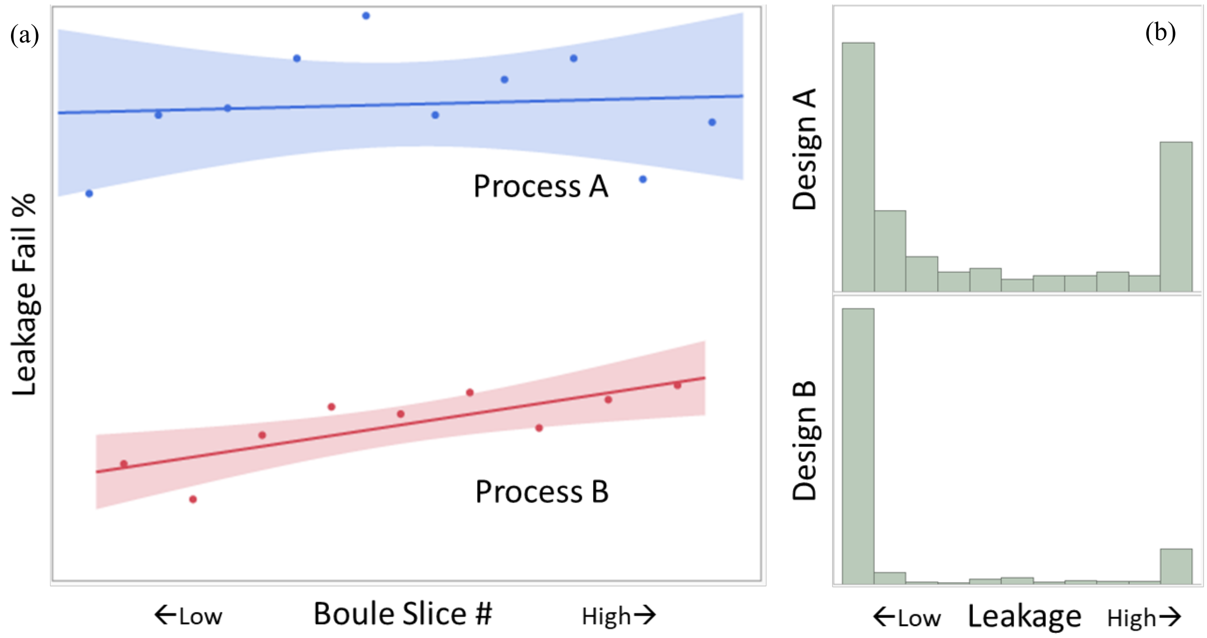

Fig. 11. (a) Process optimization showing a lower leakage fail rate from dislocations on alternating (sister) wafer slice numbers (b) Design change leading to lower dislocation related leakage distribution on wafers with the same underlying dislocation density

Device processing and design optimizations offer several paths to make the devices less sensitive to dislocations and defects. Fig. 11a shows a process optimization run on alternate slice wafers from the same boule, that shows lower leakage fails that are sensitive to dislocations. A design optimization shown in Fig. 11b shows a large reduction of high leakage current making the device less sensitive against defects. This is quite effective in both increasing yield and robustness.

Summary

In summary, understanding the evolution of the various defects throughout the manufacturing pipeline is very important to ensure yield and robustness of the devices. While major defect types are well understood, a focus on sub-classification of the defect and dislocation types can lead to better understanding of defect evolution and their effect downstream. Both inclusions and Stacking Faults were sub classified using new schemes and their impact on devices evaluated. Various ways of dealing with the defects were highlighted. This includes various strategies using epitaxy, process, and design optimizations. To understand the effect of defects in the presence of the many sources of variations in SiC production, large dataset-based statistics are needed to get clear trends and make accurate conclusions. In addition, many of the defect propagation and nucleation are probabilistic in nature. Understanding this, it is very much possible to not just live, but to thrive in the sea of SiC defects.

References

[1] H. Das, S. Sunkari, J. Justice, H. Pham and K.S. Park, Mater. Sci. Forum, 963, pp 284-287, (2019)

[2] H. Das, S. Sunkari, J. Justice, H. Pham, G. Park, and Y. Seo, Materials Science Forum, 1004, pp. 458-463, (2020)

[3] T. Neyer, M. Domeij, H. Das, and S. Sunkari, 2021 IEEE International Reliability Physics Symposium (IRPS), pp. 1-6, (2021)

[4] H. Das, S. Sunkari, J. Justice, and D. Hamann, Materials Science Forum, Vol. 1062, 406–410 (2022).

[5] E. Van Brunt, A. Burk, D. J. Lichtenwalner, R. Leonard, S. Sabri, A. Gajewski, A. Mackenzie, B. A. Hull, S. Allen, and J. W. Palmour. Mater. Sci. Forum, 924, pp 137-142, (2018)

[6] D. Baierhofer, B. Thomas, F. Staiger, B. Marchetti, C. Förster, and T. Erlbacher, Defect and Diffusion Forum, Vol. 426, pp. 11–16, (2023)

[7] PC. Chen, WC. Miao, T. Ahmed, Nanoscale Res Lett 17, 30 (2022)

[8] I. Manning, Y. Matsuda, G. Chung, E. Sanchez, M. Dudley, T. Ailihumaer, and B. Raghothamachar, Mater. Sci. Forum, Vol. 1004, pp 37-43, (2020)

[9] T.H. Eun, I.G. Yeo, J.Y. Kim, S.S. Lee, H.S. Seo, M.C. Chun, and S.K. Hong, Mater. Sci. Forum, Vol. 1004, pp 51-56, (2020)

[10] S. Kochoska, M. Domeij, T. T. Pham, S. Maslougkas, S. Sunkari, J. Justice, and H. Das, Materials Science Forum, Vol. 1091, pp. 43–47, (2023)

[11] N. Hatta, S. Ishikawa, K. Ozono, K. Masumoto, K. Yagi, M. Kobayashi, S. Kurihara, S. Harada, K. Kojima, Key Engineering Materials, Vol. 948, pp. 107–113 (2023)