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Emission of Trapped Electrons from the 4H-SiC/SiO_2-Interface via Photon-Irradiance at Cryogenic Temperatures

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Abstract. For a reliable MOSFET performance it is crucial to identify and reduce device performance limiting 4H-SiC/SiO_2 interface defects. Previous studies have focused on the quantification of the interface states density, however, the atomic defect structure is still to be investigated. Here, we introduce a new approach based on opto-electrical measurements, which allow to determine the energetic position of interface defects. The measurement routine is performed at cryogenic temperatures to suppress the thermal emission of electrons, which were trapped at interface states during the cooldown processed (from $300\,\mathrm{K}$ to $15\,\mathrm{K}$) while a positive gate voltage of $50\,\mathrm{V}$ was applied. At $15\,\mathrm{K}$ the photon-assisted emission of trapped electrons is measured in dependence on the photon's energy ($1.8\,\mathrm{eV}$-$3\,\mathrm{eV}$). The reduction of the threshold voltage is taken as an indicator for the amount of released charges after each photon irradiation. We found an enhanced emission efficiency at certain photon energies, especially at $2.8\,\mathrm{eV}$. Near-interface-traps (NITs), reported by Afanasev *et al.* are located close to the measured trap level with $E_{\mathrm{NIT}} = E_{\mathrm{C,\,SiO2}} - 2.77(5)\,\mathrm{eV}$. Recently, El-Sayed *et al.* suggested wide-angle O-Si-O bonds as defect configuration, that act as electron traps and have a similar energy as the measure trap level.

Introduction

4H-SiC/SiO_2 interface defects impact the device performance of modern 4H-SiC power MOSFETs (metal-oxide-semiconductor field-effect transistors). The mismatch between the amorphous dielectric SiO_2 and the 4H-SiC crystal creates interface states near the electron channel of the device. Hence, during operation electrons can be trapped in 4H-SiC/SiO_2 interface states, which prohibits the devices from operating at their theoretical limit [1, 2, 3]. Despite intensive experimental investigations regarding 4H-SiC/SiO_2 interface states in MOSFETs only quantitative analyses have been conducted [2, 4, 5, 6]. Recently, defects on the 4H-SiC side of the interface have been studied in more detail [7, 9] suggesting, among others, P_{bC}-centers as likely defect candidates [7, 8]. In this work, we introduce a measurement technique particularly sensitive to defect states located at the SiO_2 side of the interface. The experimental procedure uses the interplay between photon-assisted electron emission and cryogenic temperatures to slow down competing emission processes, including the phonon-assisted detrapping or tunneling processes. As thermal emission becomes very unlikely, it is possible to trigger the emission of trapped electrons via photon-irradiance. Depending on the photon's energy it is possible to determine the energetic position of trap states relative to band edges. A theoretical study suggests a stretched bond in a disordered SiO_2 as a characteristic defect with a similar energy as measured in our experiment [11].

Charged Interface Defects at Cryogenic Temperatures

Our experimental approach to characterize interface defect states in 4H-SiC n-channel MOSFETs is based on opto-electrical measurements at cryogenic temperatures. Before the actual experiment is described the needed requirements are stated. In this section it is proved that defect states can be charged by applying a gate voltage of $50\,\mathrm{V}$ during cooldown and remain charged as long as the gate voltage is kept above $9\,\mathrm{V}$.

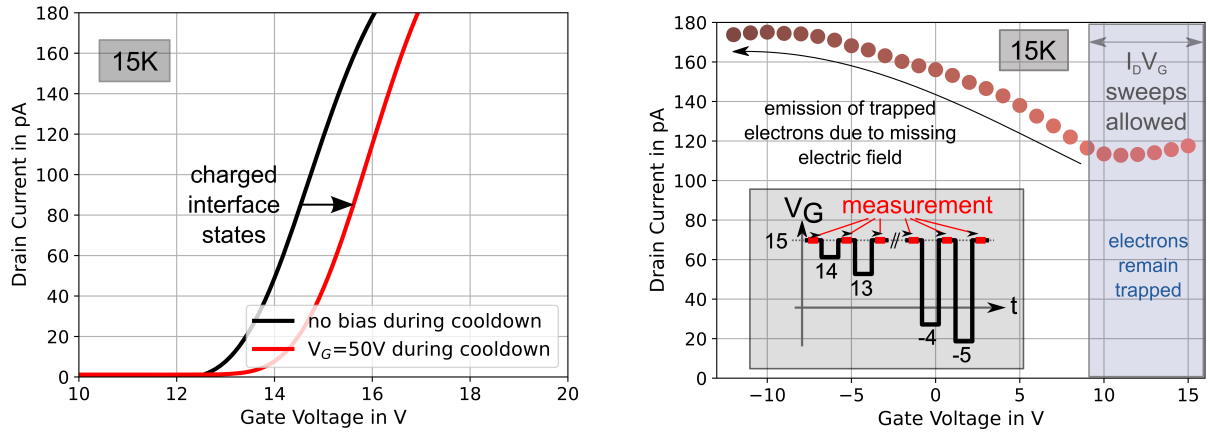

Fig. 1: (a) Two transfer characteristics at 15 K are shown, which are shifted relative to each other due to trapped charges at the 4H-SiC/SiO_2 interface. The black curve was recorded at 15 K without any bias at the gate during cooldown resulting in uncharged interface states. Both characteristics were measured from 20 V to 4 V (downward sweep direction), so no trapped electrons were emitted electrically before the measurement. (b) Prove that electrons remain trapped at interface states as long as the gate voltage stays above 9 V. The measurement is performed as follows: $V_{G,\,step}$ = 15,14,15,13,15,12,15,...,15,-4,15,-5V. Each time the gate is biased with 15 V the drain current is measured and plotted.

In order to prepare charged 4H-SiC/SiO_2 interface defects at cryogenic temperatures, a positive gate voltage needs to be applied during the cooldown from 300 K to 15 K. Fig. 1(a) shows the difference in the MOSFET's transfer characteristics between charged and uncharged defect states. The black line was recorded without applying a gate voltage during cooldown or at cryogenic temperatures. Whereas, the red curve was measured after a cooldown with a gate voltage of V_G =50 V. This left the device with charged interface states leading to a strong shift in the transfer characteristic towards more positive gate voltages as trapped charges act as additional gate potential. A second experiment with charged defect states showed that the gate voltage V_G must be kept above 9 V to avoid electric field induced emission at 15 K. The results of this experiment can be seen in Fig. 1(b), where the gate voltage was decreased step by step from 15 V to −5 V. Between each step the gate voltage was set back to 15 V and the corresponding drain current was measured and plotted. Below 9 V electric field induced emission is detected.

Experimental Setup and Procedure

Based on the findings above we can now introduce a measurement routine that uses the possibility to store charges at interface defect states at cryogenic temperatures and the photon-assisted electron emission. For this, a state of the art n-channel 4H-SiC-MOSFET with deposited oxide and post oxidation anneal is placed inside a Lakeshore CRX-6.5K cryogenic probe station. The device has separate gate, source, drain and 4H-SiC bulk contacts. A Keithley 2636B Source Measurement Unit is used to perform electrical measurements. The source and 4H-SiC bulk contacts are grounded while the drain and gate contacts can be biased. An Oriel Instruments Cornerstone 260 monochromator provides monochromatic light, which is transmitted to the device via an optical fiber. Prior to the experiment the imide was removed from the front side of the device to make the transistor better accessible for photons. The performed measurement routine consists of three phases, as shown in Fig. 2. **(I)** During the cooldown process from 300 K to 15 K the gate is biased with a DC voltage of 50 V to accumulate electrons at the 4H-SiC/SiO_2 interface, where they can be trapped at defect states. **(II)** When a temperature of 15 K is reached, the electrons remain trapped as there is very little thermal energy available

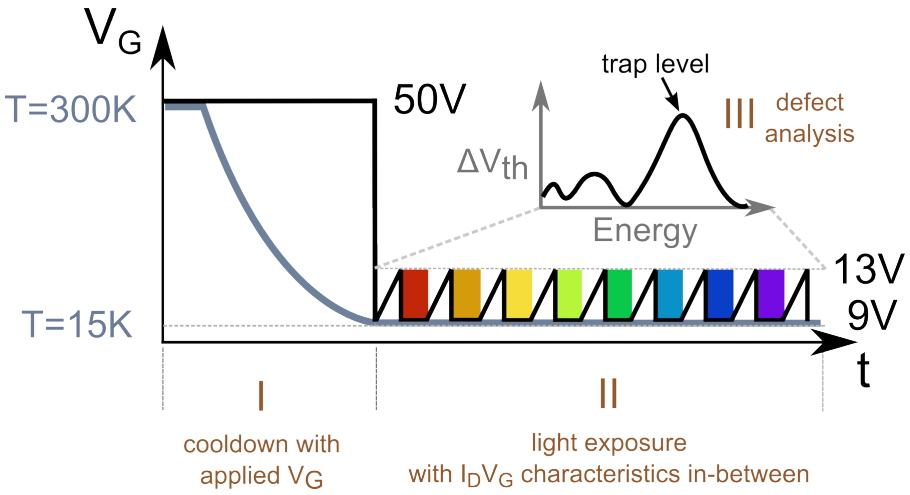

Fig. 2: The measurement principle: At 300 K a gate bias of 50 V is applied to the MOSFET test structure in order to fill trap states at the 4H-SiC/SiO_2 interface with electrons. During the cooldown to 15 K the bias is kept at 50 V. When the cryostat has reached its base temperature (15 K) the gate bias is switched to 9 V. The drain contact is constantly kept at 1 V from now on. The first transfer characteristic is recorded as a reference. In the next step the 4H-SiC MOSFET test structure is exposed to light with a photon energy of 1.8 eV (red), while the gate voltage is kept at 9 V. With the help of photons the trapped electrons can be emitted. With each iteration the photon energy is increased up to 3 eV (purple). After each light exposure another transfer characteristic is measured to determine the reduction of trapped charges at the interface. A trap level can be detected when the threshold voltage shifts more at a certain photon energy, since a trap state is depopulated by the help of the photons' energy. The result is plotted in Fig. 3.

for thermal emission processes (see Fig. 1(a)). The gate voltage is always kept above 9 V during the experimental procedure, otherwise the trapped electrons emit electrically also at cryogenic temperatures (see Fig. 1(b)). In this phase the transfer characteristic measurement and photon exposure are alternated. With each repetition the photon energy is increased stepwise from 1.8 eV to 3 eV. The photon-assisted emission of trapped charges leads to a shift in the measured transfer characteristic. **(III)** In the data analysis we investigate the difference in the threshold voltage (defined as the gate voltage needed to reach a drain current of 5 pA) as a function of the photon energy. At certain photon energies the emission of trapped charges happens more efficiently indicating the depopulation of a trap level. Note that a different readout current, 50 pA for example, would lead to the same result. In this case 5 pA were chosen, since all measured transfer characteristics have a corresponding gate voltage value to this drain current value.

Experimental Results

Fig. 3 shows the recorded transfer characteristics between 9 V and 13 V at 15 K. The sweep started at 9 V in order to avoid electric field induced emission of trapped charges and stopped at 13 V to reduce the electrical recharging of trap states. Note that each transfer characteristic was recorded after photon irradiation with the light source turned off. With increasing photon energy the transfer characteristics shift towards more negative gate voltages due to the photon-assisted emission of trapped electrons. This leads to a measurable threshold voltage change as a function of the successive photon energy $h\nu_i$, which is plotted in Fig. 4(a). With the first light exposure at 1.8 eV the ionization threshold is reached for a number of defect states at the 4H-SiC/SiO_2 interface leading to an increased change in the threshold voltage. Another enhanced drop in threshold voltage can be observed around 2.8 eV. In a control experiment with the light turned off no changes in the threshold voltage could be measured, since no optical energy was provided for the depopulation of charged interface states. To emphasize

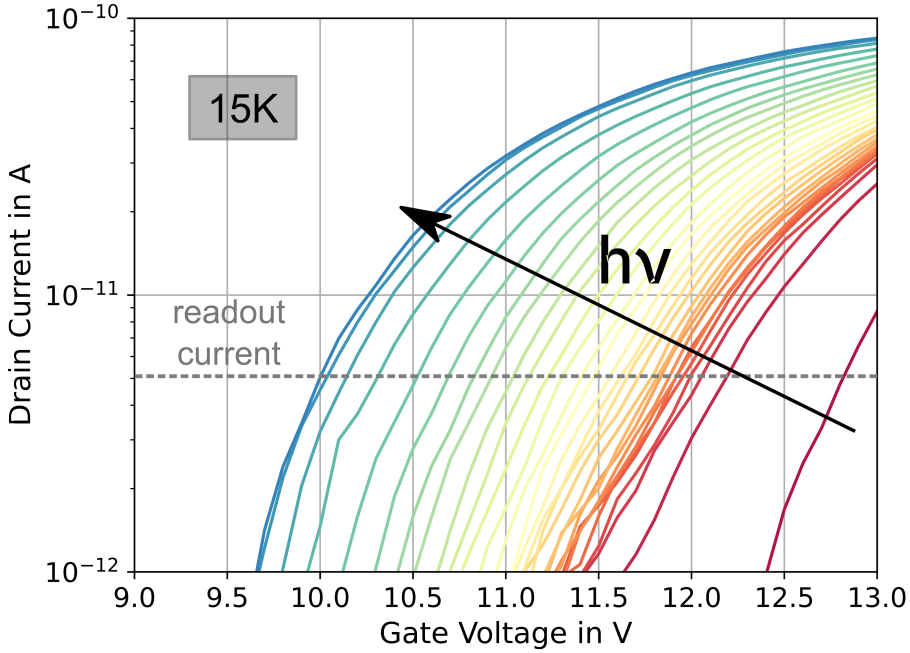

Fig. 3: At 15 K the transfer characteristics are measured after each photon exposure (1.8 eV to 3 eV). The transfer characteristics shift towards more negative gate voltages, since charges can escape from the interface defect states with the help of photons and no longer act as additional gate potential. In order to investigate the wavelength dependent light impact the threshold voltage was extracted at a readout current of 5 pA (see Fig. 4(a)).

changes in the measured threshold voltage we look at differences $(V_{\text{th, i}} - V_{\text{th, i+1}})$ of successive photon energies $h\nu_i$ (see Fig. 4(b)). In the range between 2 eV and 2.6 eV a detail analysis is difficult due to poor energy resolution as well as intensity variations and is left open for further experiments. However, a pronounced peak around 2.8 eV can be seen. Hence, photons with 2.8 eV seem to very effectively depopulate a trap state near the 4H-SiC/SiO_2 interface.

Identification of Traps

In 1997, Afanasev *et al.* measured near-interface-traps (NITs), that could be emptied by an optical energy of 2.77(5) eV [10]. The experiments were performed on thermally oxidized SiC, mutually having a very different interface microstructure compared to modern deposited and annealed oxides. A recent theoretical study by El-Sayed *et al.* reported on a strongly localized electron, which appears in a disordered oxide due to a wide O–Si–O angle [11] and has a similar energy value of about 3.17 eV. Based on these findings and our experimental results we draw a band diagram of the 4H-SiC/SiO_2 interface in Fig. 5, where the measured trap level (NIT) is depicted on the SiO_2 side of the interface and located 2.77 eV below the conduction band edge of SiO_2. If the gate voltages is above 9 V, electrons remain trapped in the near-interface-traps (NITs), since they lie below the Fermi level E_F. In this configuration only photons with 2.77 eV or more can provide the energy needed for the trapped electrons to overcome the potential barrier and emit into the conduction band of the SiO_2. When $V_G \approx 0$ V, the reduction of band bending at the interface shifts the trap levels above the Fermi level E_F and by that enables trapped electrons to emit into the conduction band of 4H-SiC (see Fig. 1(b)). Note that the energy difference between the near-interface-traps and the conduction band edge of 4H-SiC is only about 70 meV. With this picture of near-interface-states located 2.77 eV below the conduction band of the SiO_2 it is possible to coherently explain the electrical and optical behavior of the detected trap level.

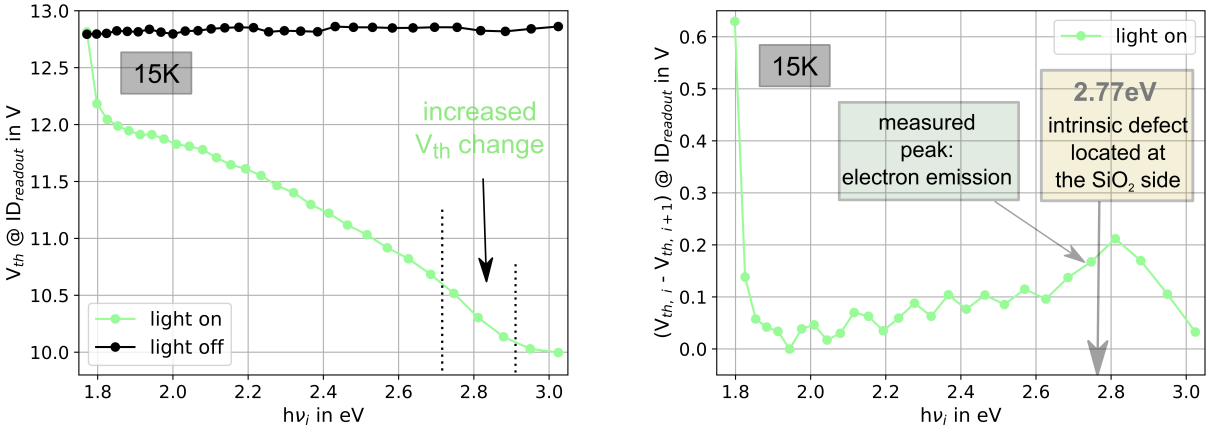

Fig. 4: (a) Shows the change in threshold voltage with dependence on the photon energy. To prove that the measured effect is due to the light a control measurement was performed, where the light source of the monochromator was turned off. In this case no significant change in the threshold voltage can be measured. (b) The threshold voltage difference $(V_{\text{th, i}} - V_{\text{th, i+1}})$ of successive photon energies is plotted against the photon energy $h\nu_i$. A pronounced peak can be seen around $2.8\,\text{eV}$, which correlates with the energy values reported in literature [10, 11], that were attributed to an intrinsic defect located at the SiO_2 side of the interface.

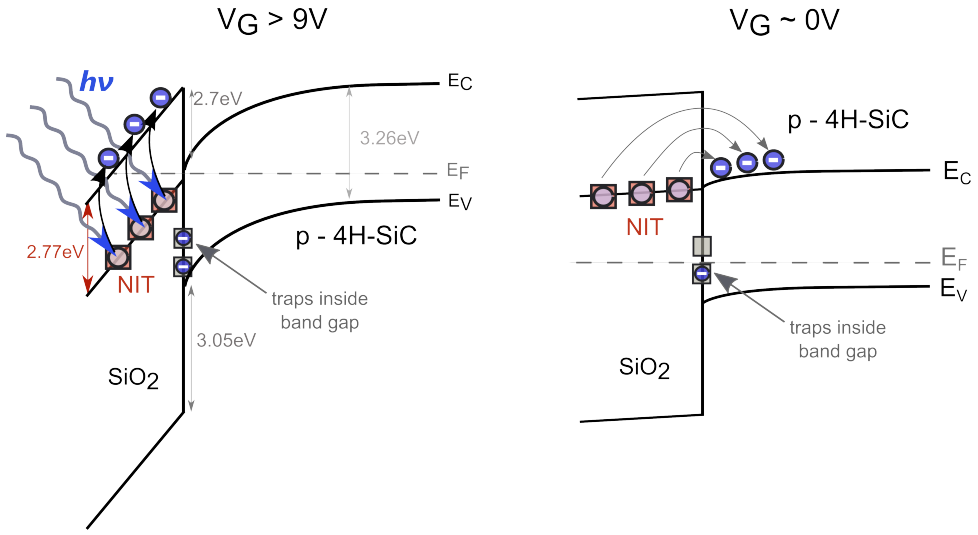

Fig. 5: Near-interface-traps (NITs) at the SiO_2 side of the interface, energetically located $2.77(5)\,\text{eV}$ below the conduction band of the SiO_2 [10]. Left: Only when the gate voltage stays above $9\,\text{V}$ electrons remain in trap states. With the help of photons electrons can directly emit from the trap state. Right: When the gate voltage is around $0\,\text{V}$ the band bending at the interface is reduced and hence, electrons can emit from trap states without the help of photons.

Conclusion

Our experiment shows that electrons can be trapped at 4H-SiC/SiO_2 interface states by applying $50\,\text{V}$ at the gate during the cooldown process and remain stored in interface traps at $15\,\text{K}$, as long as the gate voltage stays above $9\,\text{V}$. With the help of photons with energies ranging from $1.8\,\text{eV}$ to $3\,\text{eV}$ trapped electrons can overcome the potential barrier of the trap state and emit into the SiO_2 conduction band.

Based on the threshold voltage change with respect to the photon energy it is possible to identify the optical excitation energy of the trap level. Our experiment suggests $2.8\,\mathrm{eV}$ as a very efficient photon energy to promote the depopulation of a trap state located on the SiO_2 side of the interface. The measured energy is consistent with the reported value of near-interface-traps (NITs). Hence, we conclude that an intrinsic electron trap level located in the SiO_2 is present in state of the art n-channel MOSFETs with deposited oxide and post oxidation anneal. Although, the nature of the intrinsic electron trap is still under debate a recent theoretical study suggested a strongly localized electron at a wide O–Si–O angle.

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