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Body Diode Reliability of 4H-SiC MOSFETs as a Function of Epitaxial Process Parameter

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Abstract. In this paper, the authors continue the experimental evaluation of bipolar degradation for different 1.2 kV SiC MOSFETs. All the devices are stressed by pulsed repetitive forward current through the body diode with current densities varying from 1000 A/cm^2 up to 5000A/cm^2. The 1.2 kV SiC MOSFETs are split into two major groups based on the differences in epitaxial material (Type A and Type B) that are subjected to the pulsed forward current stress through the body diode. Additionally, there is a third group with Type B epitaxial material, where p+ implantation process at different temperature is applied to evaluate potential impact on bipolar degradation. Devices are electrically characterized on the Keysight B1505A power device analyzer, both before and after stress testing to trace the drift in the electric parameters. Lastly, the drift in parameters observed in some of the devices, are additionally correlated by an electroluminescence (EL) and scanning acoustic tomography (SAT) analysis.

Introduction

The presence of basal plane dislocations (BPDs) in SiC MOSFETs threaten their reliability when the body diode is operated in bipolar mode [1-4]. The bipolar degradation in SiC MOSFETs arises from stacking fault (SF) expansion from BPDs preset in the SiC epitaxial layer or the substrate. Expansion of the SF is triggered due to carrier recombination at a BPD [4-6]. From the BPDs present in the epitaxial layer, the expansion starts at lower current levels. The presence of BPDs in the substrate and their propagation into the epitaxial layer is a known phenomenon, and thus epitaxial processes are adapted to achieve a high conversion rate of the BPDs into TEDs [7].
In [1-2], both 1.2 kV and 1.7 kV SiC MOSFETs experience a significant increase in on-resistance (R_{DSon}), when the body diode is stressed at higher forward currents. The R_{DSon} increase depends on the number of BPDs present in the drift region and, once the threshold current is exceeded, the R_{DSon} drift rapidly increases beyond acceptable levels. The degradation is also present even if the number of BPDs is zero in the epi region. Therefore, the SF expansion is triggered from the BPDs present in the SiC substrate once sufficiently high current densities are conducted through the body diode.
1.2 kV SiC MOSFETs are divided into two primary categories, Type A and Type B, based on the differences in epitaxial material. Type A refers to the older epi material, while Type B represents an improved epi. In the initial chapter, devices from both epi material types are examined. The devices from both groups are classified according to the number of BPDs in the drift layer, as depicted in Table I. Group A includes several bins with a range of defects in the epitaxial layer, from 0 BPD to

a maximum of 4 BPDs. In contrast, Group B only has one bin with 0 BPD devices. The process of mapping and localization of defects is performed using Infra-Red photoluminescence (IR-PL) [8]. However, the BPDs do not originate only from the epitaxial growth or substrate, but it could be also induced during the fabrication processes. In [9] shows BPDs induced during some of the later post-processing stages in p-n SiC diodes, which are dependent on the p+ implantation concentration, energy and temperature.
In the second chapter, authors concentrate on 1.2 kV SiC MOSFETs that are manufactured using different p+ implantation temperatures. The devices are divided into two groups, those with high temperature p+ implantation (Group C) and those with room temperature p+ implantation (Group D), as shown in Table I. Unlike the previous two groups, specific binning and defects mapping in the epi layer does not apply for groups C and D. Each device undergoes stress testing with pulsed forward current through the body diode at varying current densities. After the stress testing, the devices are post-evaluated using EL and SAT to identify the root cause of observed parameter drifts and confirm the bipolar degradation.

Table I. 1.2 kV SiC MOSFETs grouped as a function of epitaxial material type and number of BPDs present in the epi layer.

<table>
<tr><th rowspan="2">Group ID</th><th rowspan="2">Epi Type</th><th colspan="2">Defects in epi layer</th><th rowspan="2">P+ implantation temperature</th></tr>
<tr><th>BPDs</th><th>Other</th></tr>
<tr><td rowspan="4">Group A</td><td rowspan="4">A</td><td>0</td><td rowspan="5">No SF, no Micropipes, no Partials</td><td rowspan="5">High temp.</td></tr>
<tr><td>1</td></tr>
<tr><td>2</td></tr>
<tr><td>4</td></tr>
<tr><td>Group B</td><td>B</td><td>0</td></tr>
<tr><td>Group C</td><td>B</td><td colspan="2">Non-mapped</td></tr>
<tr><td>Group D</td><td>B</td><td colspan="2">Non-mapped</td><td>RT</td></tr>
</table>

Epitaxial growth optimization for improved reliability

The following analysis focuses on 1.2 kV SiC MOSFETs split in two groups due to differences in the epitaxial material. Type A epi is applied for Group A devices and for Group B, Type B which represents the new epitaxy process. The differences on material level are not subject in this paper. The improved material has an improved engineered buffer that increases the robustness of the buffer to carrier injection, while also suppressing non-killer defects. The devices from both groups are continuously stressed with pulsed forward current through the body diode with current densities varying from 1000 A/cm^2 up to 1700A/cm^2. During the stress test, the temperature is maintained below the maximum junction temperature $T_{J,max}$ = 175°C by maintaining short pulse width of 50 us and frequency of 100 Hz. Each device is electrically characterized on the Keysight B1505A power device analyzer, both before and after stress testing to trace the drift in the electric parameters.
For Group A, a strong dependence of R_{DSon} drift was observed depending on the number of present BPDs in the epitaxial layer and applied stress current density, as presented in [2]. However, at a sufficient high current density ~1700 A/cm^2 even the group of zero BPDs present in the drift layer shows significant R_{DSon} drift, exceeding 100% after 1 million pulses.
With the epitaxial material (Type B) applied for Group B SiC MOSFETs significant improvement in body diode reliability is achieved. Fig. 1 shows R_{DSon} drifts measured up to 4 million cycles for Group B SiC MOSFETs mapped by the number of BPDs present in the drift layer, with maximum of 4 BPDs. Compared to Group A, Group B shows no drift in any parameter up to 1 million pulses. Fig. 2 shows the comparison, as most critical parameter the R_{DSon} drift as a function of the different epi and different current densities. The characterization of Group B at 1 million pulses shows R_{DSon} drift being well below 2%, which is very difficult to distinguish between measurement error vs actual parameter drift. Therefore, some of the devices are further stressed up to 15 million of pulses and still observed R_{DSon} drift is below 2.5%.

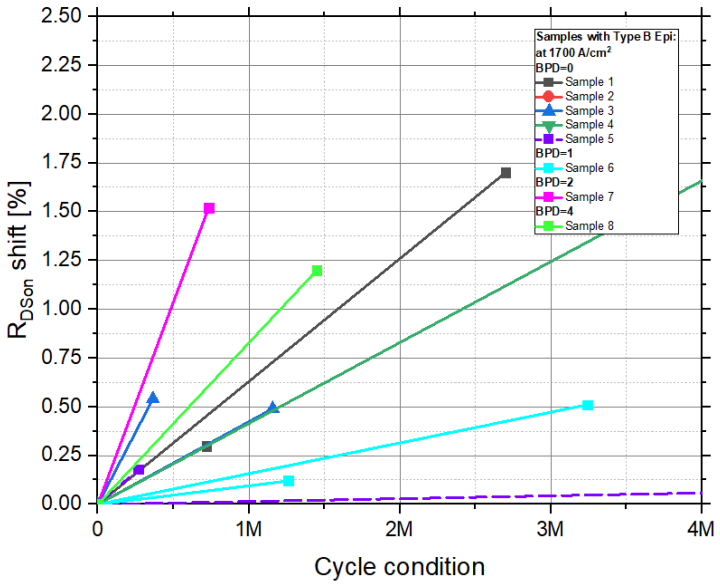


Fig. 1. The R_{DSon} drift results after few million pulses on 1.2 kV SiC MOSFETs Group B mapped by the number of present BPDs, varying from zero BPD to maximum 4 BPDs per device. Devices are stressed at current density of 1700 A/cm^2.

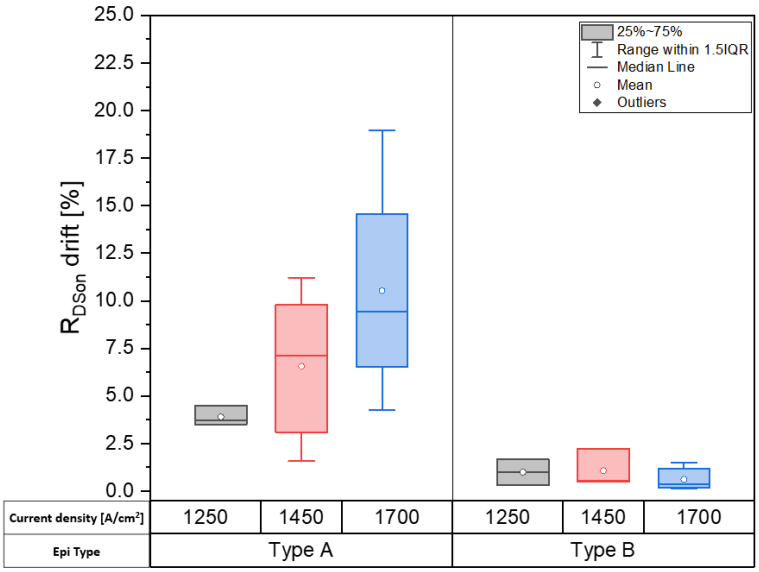


Fig. 2. The R_{DSon} drift results on 1.2 kV SiC MOSFETs Group A vs Group B extracted at 1 million pulses. Devices are stressed at current densities varying from 1250 A/cm^2 to 1700 A/cm^2 and grouped by the different epi material Type A and Type B respectively. Each box contains minimum of 10 devices and devices with different number of BPDs.

Bipolar degradation induced by fabrication process

The SiC MOSFETs, now using a new epitaxial material, have shown considerable enhancements in body diode reliability after enduring rigorous pulsed forward current stress tests. This means there is no drift in any device parameters, unlike what was observed in previous chapter for the old epitaxy. As a result, Type B epitaxial material is used for the next group of devices.

In this part, a new set of 1.2 kV SiC MOSFETs are fabricated using the Type B epitaxy. These devices underwent a p+ implantation process at both high and room temperature, forming Group C and Group D respectively. The devices are stressed under the same conditions with a pulsed forward current through the body diode as before. Thanks to the improvements in the epitaxy material, no degradation was observed for current densities up to 1700 A/cm^2. Consequently, this parameter was increased and stressing current densities now reach up to 5000 A/cm^2. For the SiC

MOSFETs fabricated with RT p+ implantation significant R_{DSon} drift of 50% is observed when exceeding the current density of 5000 A/cm^2 compared to high temperature of implantation where R_{DSon} is below 10%. Potentially, the RT implantation process introduces additional damage in the SiC crystal, resulting into measured drift in parameters as shown in Fig. 3. The current density levels used for this stress analysis may not reflect real-world application values at this stage, but it was necessary to determine the degradation threshold level. Therefore, the combination of the improved epitaxial layer and the RT p+ implantation process provides a cost-effective solution while maintaining the reliability of the SiC MOSFETs. Finally, Fig. 4 illustrates the trend of R_{DSon} drift results in 1.2 kV SiC MOSFETs after 1 million pulses. The shift from Type A to Type B epitaxy has significantly improved the body diode's robustness against bipolar degradation, requiring an increase in the stress current density. Regardless of the p+ implantation temperature, the R_{DSon} drift remains bellow 5% up to 3500 A/cm^2 with major impact noticeable at 5000 A/cm^2.

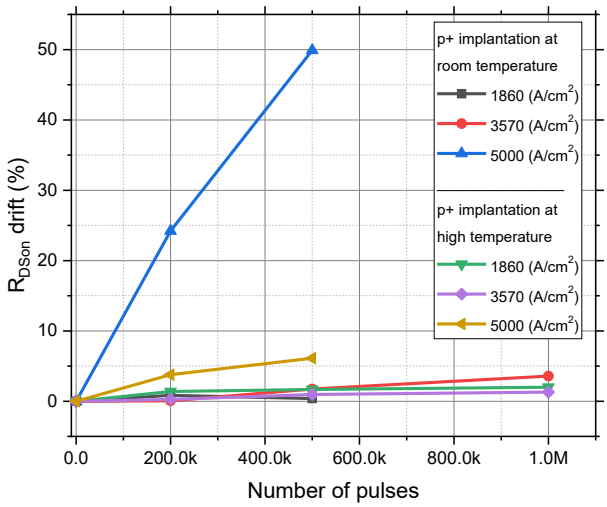


Fig. 3. The R_{DSon} drift results from 1.2 kV SiC MOSFETs Group C after number of pulses grouped by the different fabrication process. Devices are stressed at current densities exceeding 1800 A/cm^2 up to 5000 A/cm^2.

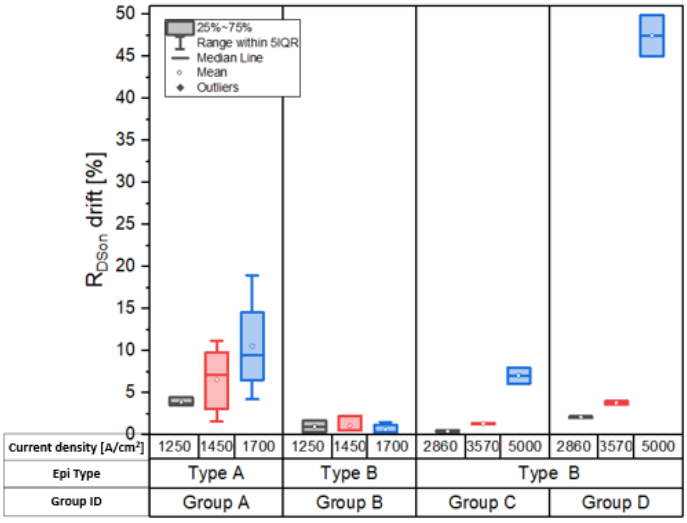
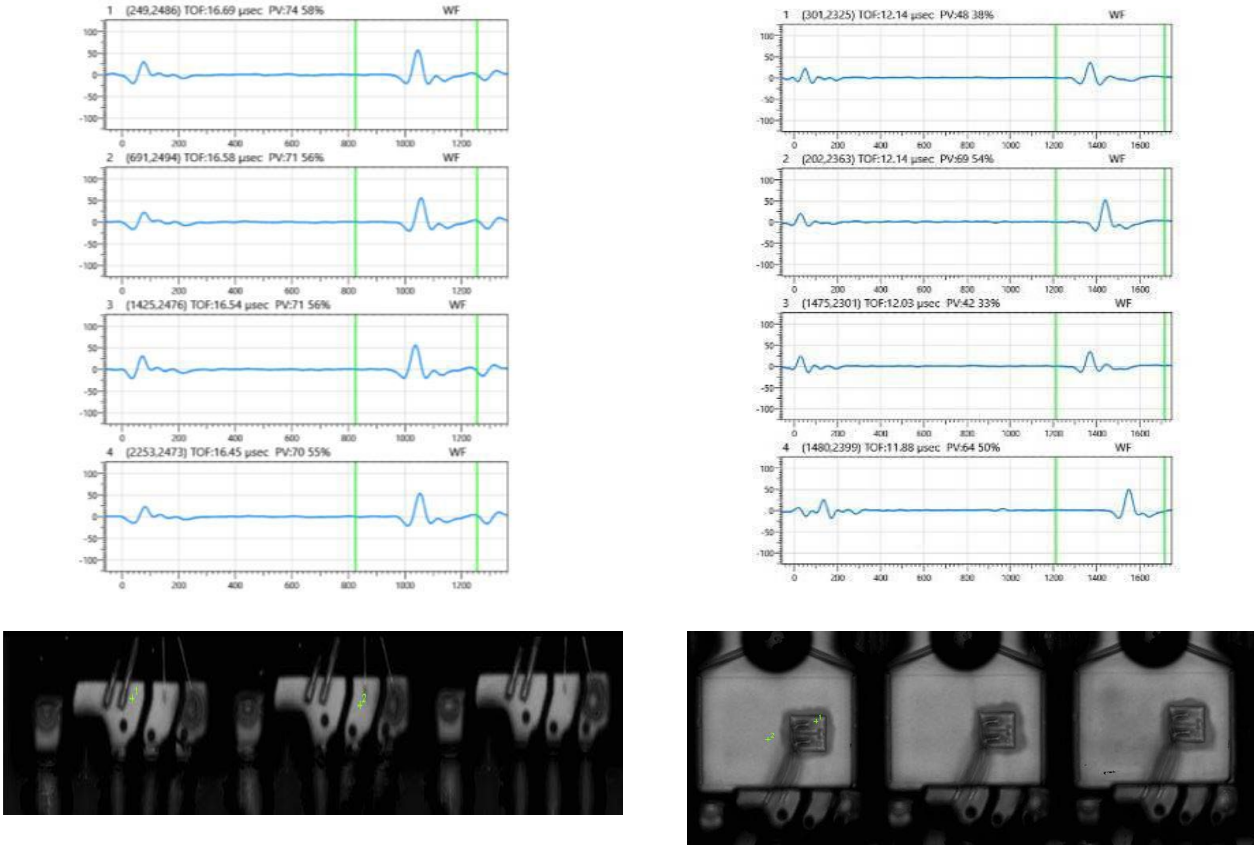


Fig. 4. The R_{DSon} drift results on 1.2 kV SiC MOSFETs extracted at 1 million pulses. Devices are stressed at current densities varying from 1250 A/cm^2 to 5000 A/cm^2, grouped by the different epi material Type A and Type B respectively. In Group D, a RT p+ implantation process is applied.

Post-analysis of the stressed devices

Since the current densities are extremely high, devices are significantly more thermally stressed than before, where the current densities did not exceed 1700 A/cm^2. To avoid wrong interpretation of the measured R_{DSon} drift, devices were submitted to failure analysis. Primarily, devices are analyzed with scanning acoustic tomography (SAT) to check for device delamination issues and secondary the electroluminescence (EL) to verify actual SF expansion due to the high current density being applied for the stress test.

a. SAT analysis



a) b)

Fig. 5. Scanning Acoustic Tomography results on 1.2 kV SiC MOSFETs stressed under forward body diode stress at extremely high current densities: (a) SAT shows no delamination on the lead layer (b) SAT shows no delamination on the die and dap layer of the SiC MOSFETs stressed under forward body diode stress.

After the continuous pulsed forward body diode stress, the devices from Group C and D were submitted for failure analysis prior to the electroluminescence. The body diode stress was conducted at extreme current densities varying from 2800 A/cm^2 to 5000 A/cm^2. This current levels significantly heat the devices during the stress test although the device temperature was constantly monitored to prevent thermomechanical failure. In Fig. 5, the SAT results show the success to avoid any delamination in the die or lead layer with this stress test methodology.

b. Electroluminescence

After the SAT analysis showing no issue of delamination, the devices from Group C are analyzed under electroluminescence. Devices are back side grinded, where a small current is being conducted through the body diode to illuminate the defects inside the crystal structure. From the captured EL images, creation of only minor stacking faults is observed although the devices are stressed at these extreme current densities. In Fig. 6a shows a fresh device as a reference. Fig. 6b and 6c, show dots

and triangular stacking faults, which is in a very small number compared to results previously observed in [2]. The device that was subject to stress at 5000 A/cm^2, as shown in Fig. 6d, displays a significant number of triangular stacking faults. These SFs are believed to be a result of the RT p+ implantation process, as devices fabricated at high temperature process do not exhibit the same quantity of defects in the EL analysis.

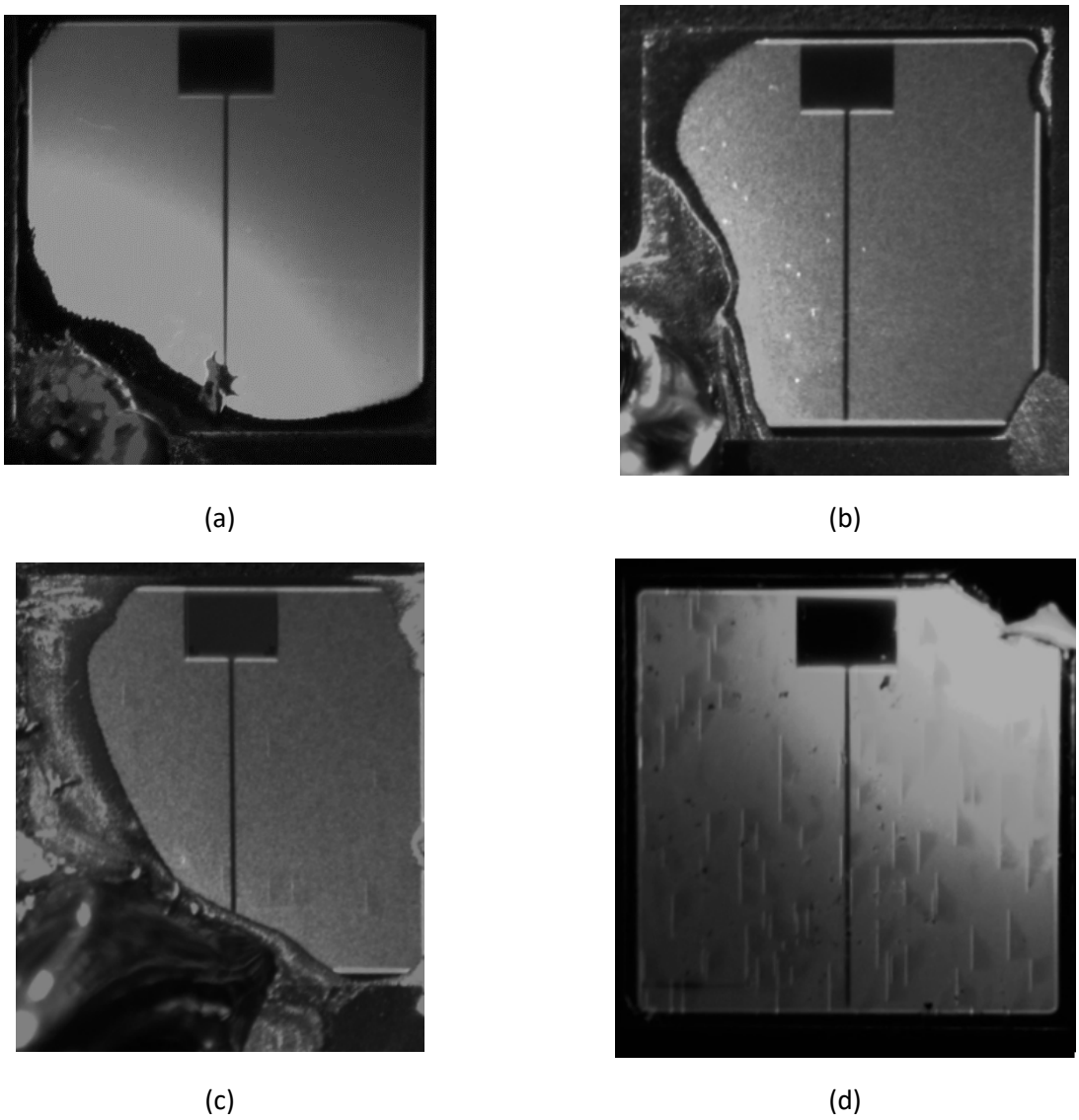


Fig. 6. Electroluminescence analysis on 1.2 kV SiC MOSFETs after body diode stress at extremely high current densities: (a) non-stressed device, (b) stressed at ~ 3571 A/cm^2, (c) ~ 5000 A/cm^2 and (d) ~ 5000 A/cm^2

Summary

Bipolar degradation in SiC MOSFETs is influenced by the number of defects in substrate, the epitaxial growth and as well the fabrication process. The amount of BPDs in substrate has decreased significantly with the improvements in crystal growth. Still depending on the quality of the epi layer, with sufficient hole density, the substrate defects can penetrate and expand as stacking faults through the epi region and cause bipolar degradation issues.

For the two types of epi material analyzed in this paper, a significant difference in device degradation is observed. Devices with Type B epi shows significant improvement in R_{DSon} drift < 2.5% over same technology with Type A and BPD=0, where R_{DSon} drift was reaching even 20%. The improvements in Type B epi material are implemented in the devices of Group C and D. The

devices with high temperature p+ implantation show no signs of degradation even when exceeding stress with 4000 A/cm^2. The devices with the RT p+ implantation up to 4000 A/cm^2 shows R_{DSon} drift < 5%, which is in acceptable range. Once this threshold is exceeded, the R_{DSon} drifts is exceeding 10% drift. This current stress levels might not be applicable in a real application now, but in foreseeable future might not be an unrealistic case. The devices with the improved epitaxy even in combination with the RT p+ implantation process shows promising trade-off in body diode reliability and cost saving.

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