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Crystal Originated Defect Monitoring and Reduction in Production Grade SmartSiC™ Engineered Substrates

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Abstract. Power devices electronics based on Silicon Carbide (SiC) are emerging as a breakthrough technology for various applications. The link between the quality of SiC substrates and device performance has been widely discussed [1]. Smart Cut™ technology offers the opportunity to integrate a high quality SiC layer on a low resistivity handle wafer. Moreover the crystal quality of a single donor wafer can be replicated multiple times to provide an epitaxy-ready substrate in high volume [2]. Nevertheless, some extended grown-in defects of SiC starting material, like micro-pipes or bulk inclusions, may generate surface defects called "Crystal Originated Defects" (COD) on transferred layers. This paper explains how SmartSiC™ defect density can be reduced by limiting the number of extended defects on donor wafers. Specific inspection recipes were developed to monitor the starting material and the replicated engineered substrate: COD root-causes and effects were analyzed. We demonstrated how a well-suited quality control of donor wafers plays a major role to guarantee defect-free SmartSiC™ wafers.

Introduction

Power devices growing market requires new technical solutions to both lower manufacturing cost and to increase the device yield. Despite the significant progress in 4H-SiC material supply and quality, raw material manufacturers are struggling to fulfill market demand. Nowadays the main players in SiC power devices are starting the processing of 200 mm SiC substrates, therefore high volume production of prime crystal grade 200 mm 4H-SiC substrates is still a challenge [3-4].

SmartSiC™ engineered substrates demonstrated the capability to combine a cost effective process (the Smart Cut™ process applied to SiC materials, explained in Fig.1) with high quality crystal grade and ultra low resistivity.

In addition, as detailed in [5], Smart Cut™ technology can be extended to 200 mm wafers to overcome the risk of large size SiC substrates shortage.

Crystal Originated Defects Generation Mechanism

Smart Cut™ technology (Fig. 1) consists in several steps including hydrogen implantation of the 4H-SiC starting wafer, enabling to control the transferred thickness (typically less than 1 μm). The implanted wafer is bonded to a handle material before splitting (step 5). Because a key step of this process is to split a thin monocrystalline SiC layer from a donor, the defectivity of the starting material has an impact on the total usable area of SmartSiC™ wafers.

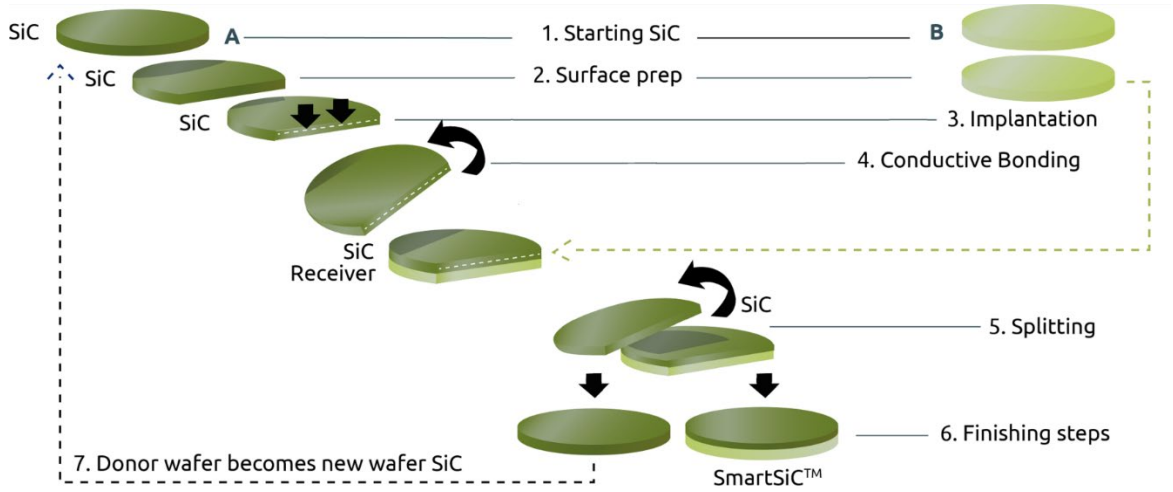


Fig. 1. Smart Cut™ process description, as adapted to SiC.

Depending on its quality, the donor substrate (starting SiC, step 1) can show different grown-in defect types, like micro-pipes and inclusions [6-7]. Some donor extended defects affect the integrity of the surface layer transferred using Smart Cut™ process, and can generate a Crystal Originated Defect (COD) after SmartSiC™ manufacturing, as schematized in Fig 2.

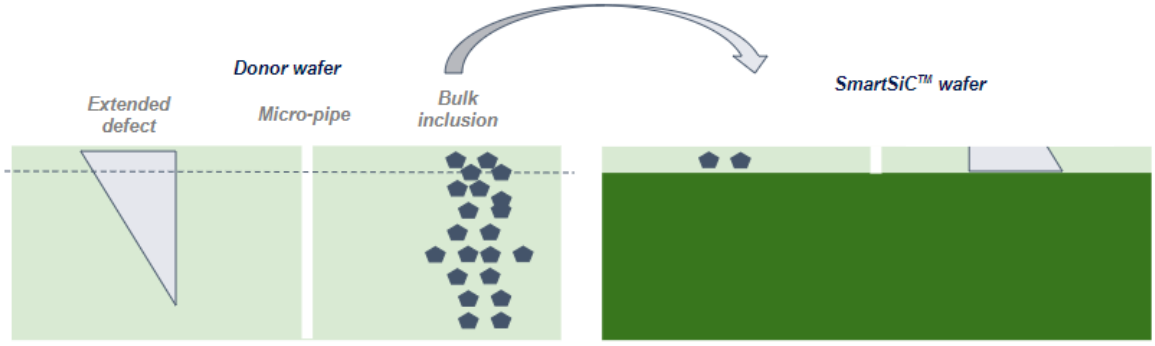


Fig. 2. Crystal Originated Defect generation from a 4H-SiC donor.

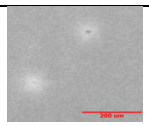
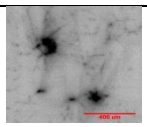
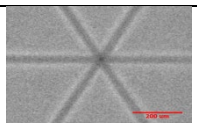
Donor Wafer Extended Defects Characterization

In this study the incoming defectivity of the donor was measured with SICA88 tool (Lasertec) consisting of a Nomarski difference interferential contrast (DIC) microscope for surface defects imaging and ultra-violet photoluminescence (UV-PL) setup for crystal defects characterization. We used 313 nm wavelength for PL excitation and a near-infrared filter to collect the images with a CCD sensor.

An Automatic Defect Classification (ADC) algorithm was optimized to capture and classify the extended grown-in defects of 4H-SiC, based on both surface and PL image properties.

Three classes of substrate defects were found to be the most critical for a successful layer transfer process: *micro-pipes*, *inclusions* and *extended dislocation arrays*. Table 1 illustrates the defects as imaged using SICA88 UV-PL channel.

Table 1. UV-PL images of extended substrate defects.

Micro-Pipes	Inclusions	Dislocation array
		

Micro-pipes are well-known SiC defects consisting in a hollow core associated with a superscrew dislocation [7]. State-of-the art SiC manufacturers can limit micro-pipe generation to reach a density below 0.1 defects/cm^2.

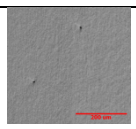
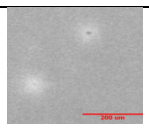
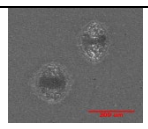
The mechanism of formation of "inclusion" defects during SiC crystal growth (especially Carbon inclusions) was described in [8] and [9]: large inclusions (>100 µm) are generally well controlled by suppliers, whereas smaller inclusions (< 20 µm) are often not specified.

Star-shaped dislocation arrays nature and effect were studied in [10]. The defect consists of a center area with high density of threading dislocations and six arms of dislocation arrays. Nowadays even prime grade 4H-SiC substrates show several star-shaped crystal defects per wafer.

Correlation of 4H-SiC grown-in defects to SmartSiC^{TM} quality

Similarly as for donors, engineered substrates defects were imaged using SICA88 surface DIC channel. A specific ADC was developed on a deep learning basis to classify SmartSiC^{TM} defect types. An adapted and fine tuned inspection allows estimating the contribution of starting material defects to substrate total usable area for devices manufacturing. Table 2 shows an example of donor extended defects and related Cristal Originated Defect (COD) replicated to the transferred layer:

Table 2. Donor micro-pipes images and corresponding COD on SmartSiC^{TM}.

Donor defectivity		SmartSiC^{TM} COD
DIC	PL	DIC
		

Therefore, donor defectivity control is crucial to guarantee prime grade SmartSiC^{TM} substrates.

Fig. 3 illustrates the link between SiC starting materials and SmartSiC^{TM} grade: donor wafer extended defects are mirrored into the replicated substrate.

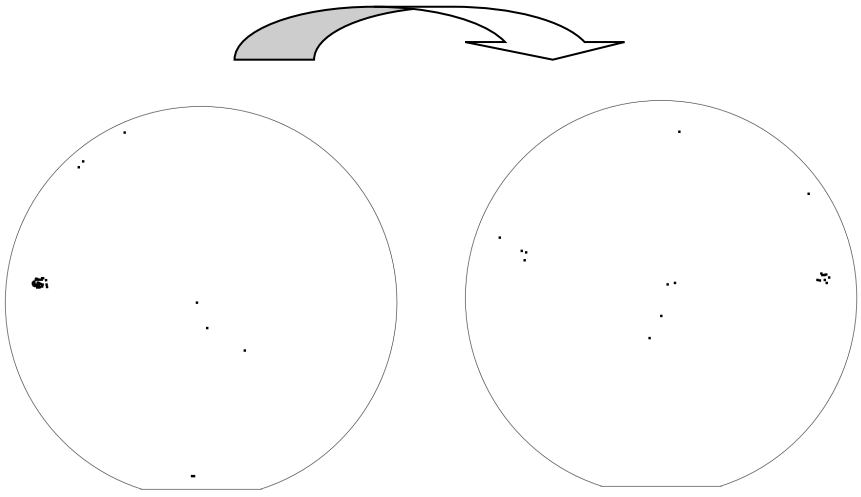


Fig. 3. SmartSiC™ defect map correlation to donor quality (from SICA88 inspection): donor wafer with crystal defect signature (left) and corresponding replicated SmartSiC™ (right)

As shown in Fig.4, selecting high quality starting materials allows manufacturing engineered substrates with less than 0.1 defects/cm^2:

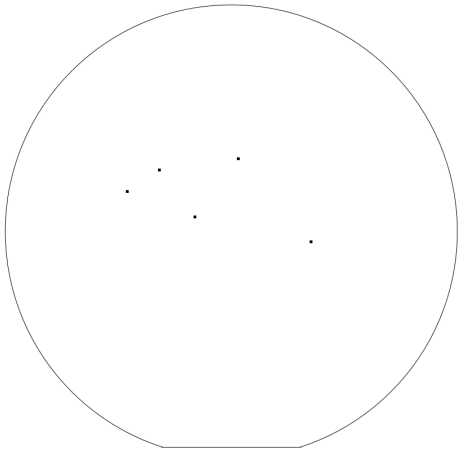


Fig. 4. SICA defect map for prime grade SmartSiC™ from high quality donor.

Summary

In this work, we showed how 4H-SiC donor material extended defects (micro-pipes, inclusions and star-shaped dislocation arrays) generate Crystal Originated Defects (COD) after SmartSiC™ manufacturing. A well-suited metrology was developed to monitor critical defects and we demonstrated the relation between donor and SmartSiC™ quality.

Novel Smart Cut™ approach allows selecting best-in class donor wafers and replicating their quality multiple times. Thus SmartSiC™ technology is able to provide both 150 mm and 200 mm high quality engineered substrates to growing power device market.

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