Analysis of Lattice Damage in 4H-SiC Epiwafers Implanted with High Energy Al Ions at Elevated Temperatures

Submitted: 2023-09-30

Accepted: 2024-04-15

Online: 2024-08-22

Zeyu Chen^{1,a*}, Yafei Liu^{1,b}, Qianyu Cheng^{1,c}, Shanshan Hu^{1,d}, Balaji Raghothamachar^{1,e}, Reza Ghandi^{2,f}, Stacey Kennerly^{2,g}, Charles Carlson^{3,h}, Dannie Steski^{3,i} and Michael Dudley^{1,j}

¹Department of Materials Science & Chemical Engineering, Stony Brook University, Stony Brook, NY 11794 USA

²GE Research, Niskayuna, NY, 12309, USA

³Brookhaven National Laboratory, Upton, NY, 11973, USA

^azeyu.chen@stonybrook.edu, ^byafei.liu@stonybrook.edu, ^cqianyu.cheng@stonybrook.edu, ^dshanshan.hu@stonybrook.edu, ^ebalaji.raghothamachar@stonybrook.edu, ^fghandi@ge.com, ^gstacey.kennerly@ge.com, ^hccarlson@bnl.gov, ⁱsteski@bnl.gov, ^jmichael.dudley@stonybrook.edu

Keywords: 4H-SiC; Heated high energy ion implantation; Lattice strain; HRXRD

Abstract. 4H-SiC wafers with 12 μm epilayers were blanket implanted to a depth of 12 μm with 5 x 10¹⁶ cm⁻³ Al ions via Tandem Van de Graaff accelerator located at Brookhaven National Laboratory with energy range of 13.8 to 65.7 MeV at room temperature, 300 °C and 600 °C. High resolution X-ray diffraction measurements reveal the implanted layers are characterized by tensile strains. However, the dynamic annealing process reduces the level of tensile strains as the temperature of implantation is increased. Analysis indicates that the implant temperature of 600 °C is not sufficient to minimize lattice damage due to implantation and a higher implantation temperature will be required. This preliminary experiment will guide the optimization of implantation conditions for fabricating superjunction devices.

Introduction

Silicon Carbide (SiC) is a wide bandgap semiconductor with great potential for power devices. Its properties, such as a wide bandgap, high breakdown voltage, and thermal stability, allow SiC devices to operate in harsh environments like high temperature, voltage, and frequency [1]. 4H-SiC high voltage devices that can withstand 1.7 to 6.5 kV are in demand for applications like hybrid systems, shipboard and power grid systems, and high-speed trains. These devices are usually fabricated on 4H-SiC wafers with thick epilayers to increase breakdown voltages [2] but uniformly doping such thick epilayers is difficult. A solution is to use multi-step high energy ion implantation via the system developed at Brookhaven National Laboratory (BNL)'s Tandem Van de Graaff accelerator facility [3], which is capable of implanting ions at energies up to 150 MeV. Using this system, medium voltage charge balance devices, 2 kV and 3.8 kV superjunction structure PIN diodes have been demonstrated [4-6]. However, high energy ion implantation introduces significant lattice strain by displacing host atoms in the epilayer so characterizing this strain is important to understand the damage caused by high energy implantation.

Previously, synchrotron X-ray plane wave topography (SXPWT) and reciprocal space mapping techniques have been used to characterize strain distribution within the 12 μ m epilayer of a 4H-SiC epiwafer high energy implanted with 5.56 x 10¹³ cm⁻² Al ions at room temperature. The results show that the strain level of implanted region is around 2.5 x 10⁻⁴ higher than that of the region without implantation [7]. The intensity profile extracted from the topograph is fitted by Rocking-curve Analysis by Dynamical Simulation (RADS) and the corresponding strain profile within the epilayer indicates a maximum strain of around 2.4 x 10⁻⁴. Thus, for a 12 μ m 4H-SiC epiwafer, high energy implantation with Al ions at room temperature results in significant tensile strain. An annealing temperature as high as 2000 °C is found to be required to completely recover this strain [8]. Such

high temperatures, however, cause the wafers to end up with rough surfaces, undesirable for device fabrication.

One approach to lower annealing temperature is carrying out high energy implantation at high temperatures since the dynamic annealing effect will reduce the lattice strain to some extent in the asimplanted wafer. Dynamic annealing effect has been studied for many years. Kuznetsov and coworkers [9] proposed that reduction of lattice damage due to dynamic annealing effect is due to annihilation of the point defects (vacancies and interstitials) generated during implantation. The extent of lattice damage after heated implantation depends on the rate of generation and annihilation of the point defects.

Conventional implantations at temperatures as high as 600 °C have been shown to suppress the generation of basal plane dislocations (BPDs) due to the strain induced by implantation [10]. In this study, a high temperature stage designed for high energy implantation at the Tandem facility at BNL has been employed to carry out preliminary high energy implantation experiments on 4H-SiC wafers at different temperatures and the wafers analyzed by high resolution X-ray diffraction.

Experiment

4H-SiC wafers with 12 μ m epilayers were blanket implanted with Al ions by multi-step high energy implantation at room temperature (RT), 300 °C and 600 °C at BNL via the Tandem Van de Graaff accelerator with energy range of 13.8 to 65.7 MeV. The concentration of the implanted Al ions is 5 x 10^{16} cm⁻³. The wafers were characterized by high resolution X-ray diffraction (HRXRD) to analyze the effect of temperature on the lattice strain generated by the implantation. Rocking curves and reciprocal space mapping (RSM) in (0008) reflections were carried out on a Bede D1 diffractometer with Cu K α (λ =1.54056 Å). The beam was conditioned by a MaxFlux multilayer mirror and channel-cut Ge (004) monochromator at 40 kV and 30 mA. For triple axis scan and RSM, a channel-cut Si (111) analyzer was placed in front of the detector (see Fig. 1 for schematic of the experimental setup).

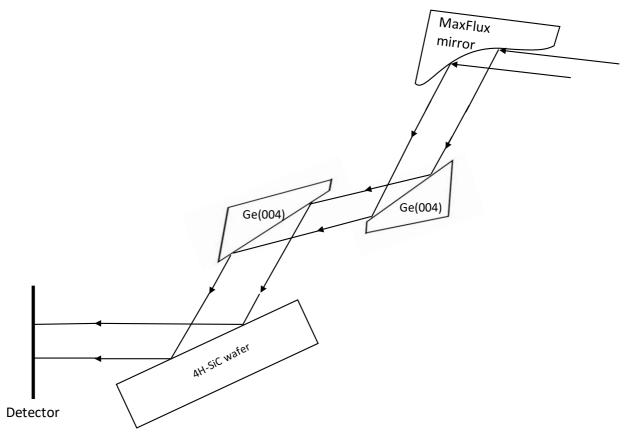


Fig. 1 Schematic of experimental setup of HRXRD.

Results & Discussion

Triple axis $\omega - 2\theta$ scans have been conducted for reference unimplanted epi-wafer and implanted epi-wafers. Fig. 2 shows the curves plotted with offset on y axis (intensity) to indicate the differences. For the reference wafer, as expected only one peak with full width half max (FWHM) of 11" is observed indicating that the wafers have high crystal quality and no significant strain between epilayer and substrate. In the case of the implanted wafers, the $\omega - 2\theta$ curves show two peaks, where the lower intensity main peaks are diffracted from the substrate and the high intensity satellite peaks are diffracted from the implanted epilayer. The lower intensity of the substrate peak is due to relatively thick epilayers that attenuate diffracted intensity from the substrate. The shape of the curves suggest that the implanted layers retain crystalline structure but suffer from the damage due to the implantation. It is noted that satellite peaks for the implanted wafers are located on the left side of the main peak, indicating that the tensile strain along [0001] direction exists in the wafers. The separations between the main peak and the satellite peak are 58", 40" and 32" for wafer implanted at RT, 300 °C and 600 °C, respectively. As the implant temperature increases, the separation between the main and satellite peaks decreases, which means that the extent of the tensile strain decreases as implant temperature increases. Such result also illustrates that dynamic annealing effect has been successfully activated. Since the flux, fluence and concentration are the same for the implanted wafers, the rate of point defect generation can be expected to similar. Moreover, lower tensile strains in heated implanted wafers indicates that the annihilation rate of point defects is higher at high temperatures.

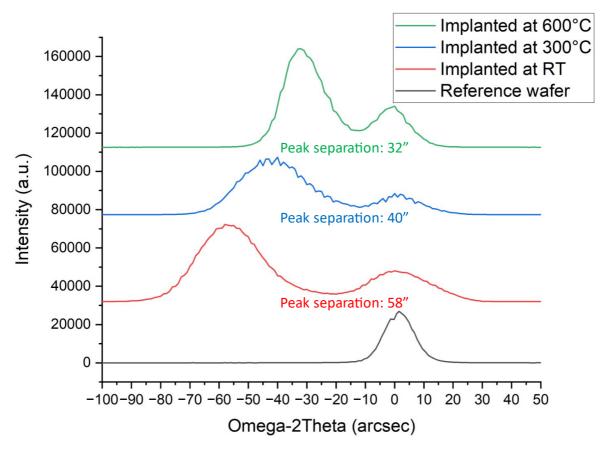


Fig. 2. Triple axis $\omega - 2\theta$ scans of reference unimplanted 4H-SiC epiwafer and 4H-SiC epiwafers implanted at RT, 300°C and 600°C. The curves are plotted with offset along y axis (intensity) to show the differences.

0008 RSMs were recorded to understand the nature of the strain in the sample, as shown in Fig. 3. The RSMs correlate with the triple axis scans showing two peaks and satellite peaks have higher intensity than the main peak. The two peaks line up vertically indicating no tilt and the satellite peaks

are located on the negative side of the main peak along the y axis, indicating the epilayers have tensile strain after the implantation which correlates with the results of the triple axis scan. Lattice strain can be estimated by the following equation:

$$\frac{\Delta d}{d} = -\Delta Q_{y} d \tag{1}$$

where d is the lattice spacing of 4H-SiC (0008) and ΔQ_y is the change in peak position along the vertical axis in the RSM. The changes of peak positions are measured to be -3.3/ μ m, -2.6/ μ m and -1.6/ μ m for epiwafers implanted at RT, 300°C and 600°C, respectively. By applying Eq. 1, strain in the implanted layer with respect to substrate are calculated as 4.1 x 10⁻⁴, 3.3 x 10⁻⁴ and 2.0 x 10⁻⁴ for wafer implanted at RT, 300°C and 600°C, respectively. Such results have been summarized in Table.1. Higher implantation temperatures thus triggers dynamic annealing, leading to mitigation of tensile strain due to implantation.

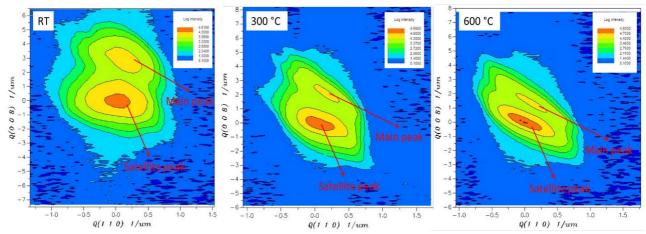


Fig. 3. (0008) RSMs of implanted wafers at (a) RT (b) 300°C and (c) 600°C. Two peaks are shown in the RSMs, where the main and satellite peaks are highlighted.

Table 1. HRXRD results of 4H-SiC epiwafers subject to high temperature, high energy implantation.

Sample ID	Implanted Al ion concentration (cm ⁻³)	Implantation Temperature (°C)	Strain (from RSM)
Reference	-	-	-
1	5 x 10 ¹⁶	RT	4.1 x 10 ⁻⁴
2	5 x 10 ¹⁶	300	3.3 x 10 ⁻⁴
3	5 x 10 ¹⁶	600	2.0 x 10 ⁻⁴

Compared with conventional implantation at energies below 1 MeV, where dynamic annealing temperature of 600°C is usually sufficient [10,11,12], wafers implanted at high energy in thick epilayers clearly require higher implantation temperatures to achieve lowest tensile strain after implantation in order to lower the temperatures for the activation annealing process and prevent surface roughness due to higher temperature annealing [8]. Implantation at temperatures higher than 600°C are therefore planned for the next round of implantation runs at the Tandem facility at BNL. Wafers implanted at higher temperatures will be characterized by triple axis HRXRD and RSMs and compared with current results.

Summary

High resolution X-ray diffraction measurements have been applied to characterize 4H-SiC wafers with 12 μ m epilayer which has been blanket implanted with 5 x 10¹⁶ cm⁻³ Al ions at room temperature, 300 °C and 600 °C. Triple axis $\omega - 2\theta$ scans and reciprocal space maps show two peaks where the high intensity satellite peaks corresponding to the implanted layers is located at the negative side of the main peaks (substrate), indicating tensile strains exist in the epilayers after implantation. Strain values of 4.1 x 10⁻⁴, 3.3 x 10⁻⁴, and 2.0 x 10⁻⁴ are calculated based on the peak separation from the reciprocal space map for wafers implanted at RT, 300°C and 600°C, respectively. Strain values decreased as temperature of implantation is increased indicating that dynamic annealing process has been successfully activated. However, implant temperature at 600°C is not sufficient to achieve lowest lattice strain due to implantation in the wafers. Future implantation experiments at temperatures higher than 600°C will be conducted and compared to optimize the dynamic annealing process.

Acknowledgement

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0001028. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

Work at Brookhaven National Laboratory was sponsored by the U.S. Department of Energy under Contract No. DE-SC0012704 with Brookhaven Science Associates, LLC.

This research used resources of the Advanced Photon Source, a U.S. Department of Energy (DOE) Office of Science User Facility operated for the DOE Office of Science by Argonne National Laboratory under Contract No. DE-AC02-06CH11357. The Joint Photon Sciences Institute at SBU provided partial support for travel and subsistence for access to Advanced Photon Source.

References

- [1] J. Guo, Y. Yang, B. Raghothamachar, T. Kim, M. Dudley, J. Kim, J. Cryst. Growth 480 (2017) 119-125.
- [2] T. Liu, S. Hu, J. Wang, G. Guo, J. Luo, Y. Wang, J. Guo and Y. Huo, IEEE Access, 7 145118-145123. (2019)
- [3] P. Thieberger, C. Carlson, D. Steski, R. Ghandi, A. Bolotnikov, D. Lilienfeld, P. Losee, Nucl. Instrum. Methods Phys. Res. B: Beam Interact. Mater. At. 442 36-40. (2019)
- [4] R. Ghandi, C. Hitchcock, S. Kennerly, ECS Transactions 104 67 (2021)
- [5] R. Ghandi, A. Bolotnikov, S. Kennerly, C. Hitchcock, P.-m. Tang, T.P. Chow, 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), IEEE, 126-129 (2020)
- [6] R. Ghandi, C. Hitchcock, S. Kennerly, M. Torky and T. P. Chow, 2022 International Electron Devices Meeting (IEDM), pp. 9.1.1-9.1.4 (San Francisco, CA, USA, 2022)
- [7] Z. Chen, H. Peng, Y. Liu, Q. Cheng, S. Hu, B. Raghothamachar, M. Dudley, R. Ghandi, S. Kennerly and P. Thieberger, Materials Science Forum 1062, 361-365 (2022)
- [8] Z. Chen, Y. Liu, H. Peng, Q. Cheng, S. Hu, B. Raghothamachar, M. Dudley, R. Ghandi, S. Kennerly and P. Thieberger, ECS J. Solid State Sci. Technol. 11 065003 (2022)

- [9] A. Yu. Kuznetsov, J. Wong-Leung, A. Hallen, C. Jagadish, and B. G. Svensson, Journal of Applied Physics 94, 7112 (2003)
- [10] S. Mancini, S. Jang, Z. Chen, D. Kim, Y. Liu, B. Raghothamachar, M. Kang, A. Agarwal, N. Mahadik, R. Stahlbush, M. Dudley, W. Sung, proceeding of 2022 IEEE International Reliability Physics Symposium (IRPS) (2022)
- [11] Z.C. Feng, S.C. Lien, J.H. Zhao, X.W. Sun and W. Lu, Thin Solid Films 516.16 (2008) 5217-5222.
- [12] M. Rawski, J. Żuk, M. Kulik, A. Droździel, L. Lin, S. Prucnal, K. Pyszniak and M. Turek, Proceedings of the VIII International Conference ION (2010)