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The Elusive Bulk Inclusion, Sizing, Wafer- and Ingot-Level Localization and their Effect on Dislocation Generation and Epitaxial Defectivity in 4H-SiC

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Abstract. Results from optical defect inspections, and X-ray topography, on wafers from entire 4H-SiC ingots provide a clear visualization on the positional dependance of bulk inclusions in ingots with respect to growth stages, looking to both density and size. It is also clear while studying the superpositioning of Laue–Bragg interference densities that the different categories of said defectivity generate new crystallographic defects, dislocations. These in turn lead to significant reductions in usability of wafers, and the lack of tracing such defects, cause an increased difficulty to predict the final device yield, as is displayed by growing epitaxial layers on materials heavily affected by bulk inclusions.

Introduction

Wide-bandgap semiconductor-based electronics are constantly being developed, with 4H-Silicon Carbide (4H-SiC) leading the way in next generation power devices. Within power electronics, SiC carries intrinsic advantages with higher thermal operation and lower switching losses compared to Silicon-based electronics [1-2]. The fundamental understanding of 4H-SiC crystal growth is also expanding in-line with an increasing commercialization of 4H-SiC wafers, with more key actors and larger facilities ramping up production and thus, increasing the global availability. When scaling up, and larger amount of data becomes available, you realize the outliers is a significant part of the distribution.

Herein, we investigate a defect seemingly overshadowed by more typical and apparent defects, for example micropipes and dislocation. Expanding the understanding of 4H-SiC defectivity with novel results on Bulk Inclusion (BI) tracing and sizing, and the consequences following its presence. We deep-dive into the consequences of such defects, showing how they can affect yield in thin 4H-SiC bonded layer technology. The mere presence of them close to the wafer surface, depending on their size, causes traceable decorations in grown epitaxial layers and directly impacts device yield. We show the ability to pin-point them in the wafer volume (3D) using commercial optical defectivity inspection tools, sizing and, classifying them with respect to their impact on consecutive product or device steps. In addition, many commercial systems used today also have an interaction-volume in orders of several um in the surface sensitive channels, easily mis-bin the presence of such defects as surface contaminations, possibly giving rise to misrepresented yield approximations, unnecessary wafer scrap and, wafers being graded too low. A better understanding of BI will assist in superior yield approximation and material allocation with respect to how sensitive a product is to different sizes of BIs.

Experimental Details

In this work, defectivity data from several thousand 200 mm 4H-SiC N+ production and development grade wafers, produced in-house, have been used to create accurate theoretical models for defect and dislocation visualization, with their spatial and volumetric dependance as a function of crystal growth stages. The optical defectivity inspection tools used were KLA Candela 8520 and, to verify and align results, a Lasertec SICA88. Specially developed recipes on the former were used to,

not only localize, but also sub-categorize bulk inclusions in ranges of 60 nm to more than 1 µm. The results are compared with conventional recipes that are tailored to include standardized defects with sizing and classification of surface contamination calibrated towards reference wafers with polystyrene latex (PSL) particles on the surface. For dislocation data, a handful of wafers per ingot were scanned using a Rigaku XRTmicron and post-processed using in-house developed recipes using XRT Toolbox software. Epitaxial growth was done using an ASM LPE108 single-wafer CVD reactor. Processing of data was done with in-house made analytical software using primarily Python and R.

Experimental Results and Discussion

Generally, during data acquisition in commercial inspection tools, contrast images are generated based on some inherent normalization rules set in the software by either supplier or user. A system can contain several light sources, and several receiving signal detectors, at various angles. The acquired dataset is further processed by filtering noise from signals, using once again, pre-set rules to find contrast points that could be potential defects. The selected contrast point then goes through a hierarchy of different binning rules, looking to the data from one or more signal detectors, and if all criterias are fulfilled, it gets binned as a defect. If it fails to fulfill all pre-set defects in a binning hierarchy, it is considered noise and becomes undefined. More modern tools utilize machine learning to execute similar logic as mentioned above.

Experienced users can tailor the above logic to find the flaws in the material that do not necessarily fall under what is conventionally tracked in production environments, and this is exactly what is done in this work. We have used a finely tuned recipe, which utilizes several non-standard optical properties from different light sources and signal detectors, to find and sub-categorize volumetric defects in individual 4H-SiC wafers. Post-processing of the data using mathematical models can then construct a 3D visualization of the results of entire ingots. An example of this can be seen in **Fig. 1**, highlighting BIs of various sizes in an R&D ingot, grown under conditions favoring BIs formation, by combining data from all wafers belonging to it, here showing small (green), medium (blue) and large (red), BIs with approximate sizes of <300 nm, >300 nm and >1 µm, respectively.

In **Fig. 1** there is a clear dependance on both the planar position and size of BIs as a function of the lateral position in the ingot, which corresponds to different stages during the crystal growth process. The detailed explanation for this is quite complex and not within the scope of this work, several factors can play a part. Examples of this could be the crystal growth rate, growth thickness,

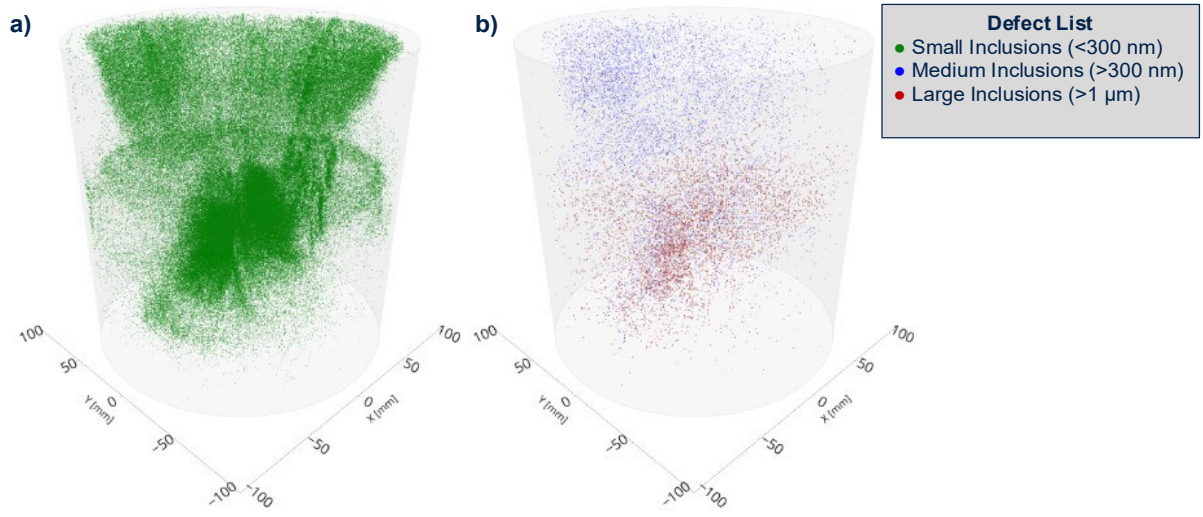

Fig. 1. 3D picture of entire R&D ingot used to produce 200 mm test wafers, showing real positions and distributions of a) smaller (green), b) medium (blue) and large (brown) Bulk Inclusions. Note that Z-axis is not to scale and exaggerated to ease interpretation.

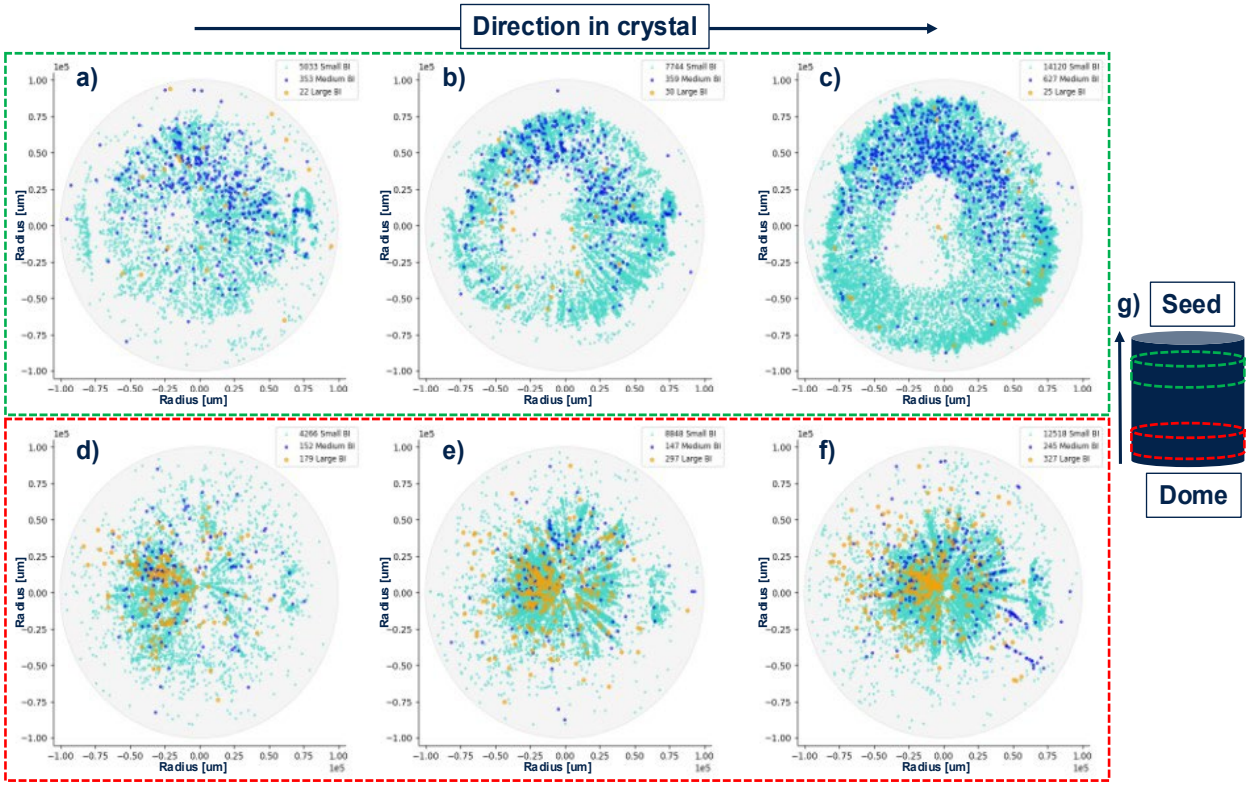

Fig. 2. Gradient of small (light blue), medium (blue) and large (brown) bulk inclusions in two separate regions, a)-c) green segment closer to seed and d)-f) red segment closer to the dome, moving from g) dome to seed position.

stoichiometry of powder changing as a function of growth-time and rate, deterioration of graphite parts and their respective coatings, variation in the magnetic field strength, temperature gradients and so forth. All of which can give rise to circumstances where particles land on the growth front, briefly interrupting it, to evaporate or impinge, and eventually get overgrown to form voids or inclusions.

In **Fig. 2**, defectivity plots of BIs for individual wafers, belonging to the ingot shown in **Fig. 1**, can be seen. In **Fig.2 a)-c)** the density of small and medium BIs increases and propagates outward as we move closer to the seed, while the segment closer to the end of the growth cycle, the dome, shown in **Fig. 2 d)-f)**, shows less small and medium BIs but with the addition of large BIs, propagating outward as we move further away from the seed and close to the dome, the end of the crystal growth cycle. It is clear looking at the density and gradient of the defects that portions of these would be well within

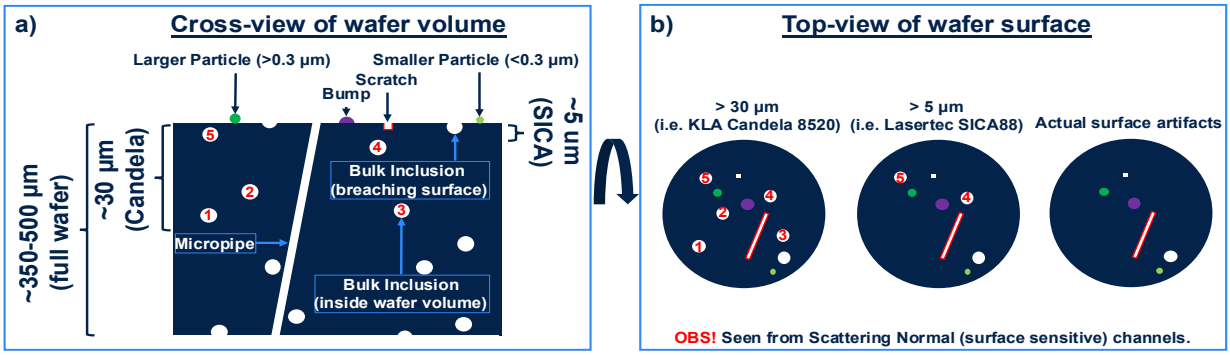

Fig. 3. Illustration of commercial defectivity on bare 4H-SiC substrates, including Bulk Inclusions, as seen a) cross-view of wafer volume with approximate interaction depths of KLA Candela 8520 and Lasertec SICA88 scattering normal and b) top-view showcasing which features would be registered as topographical defects using standardized recipes.

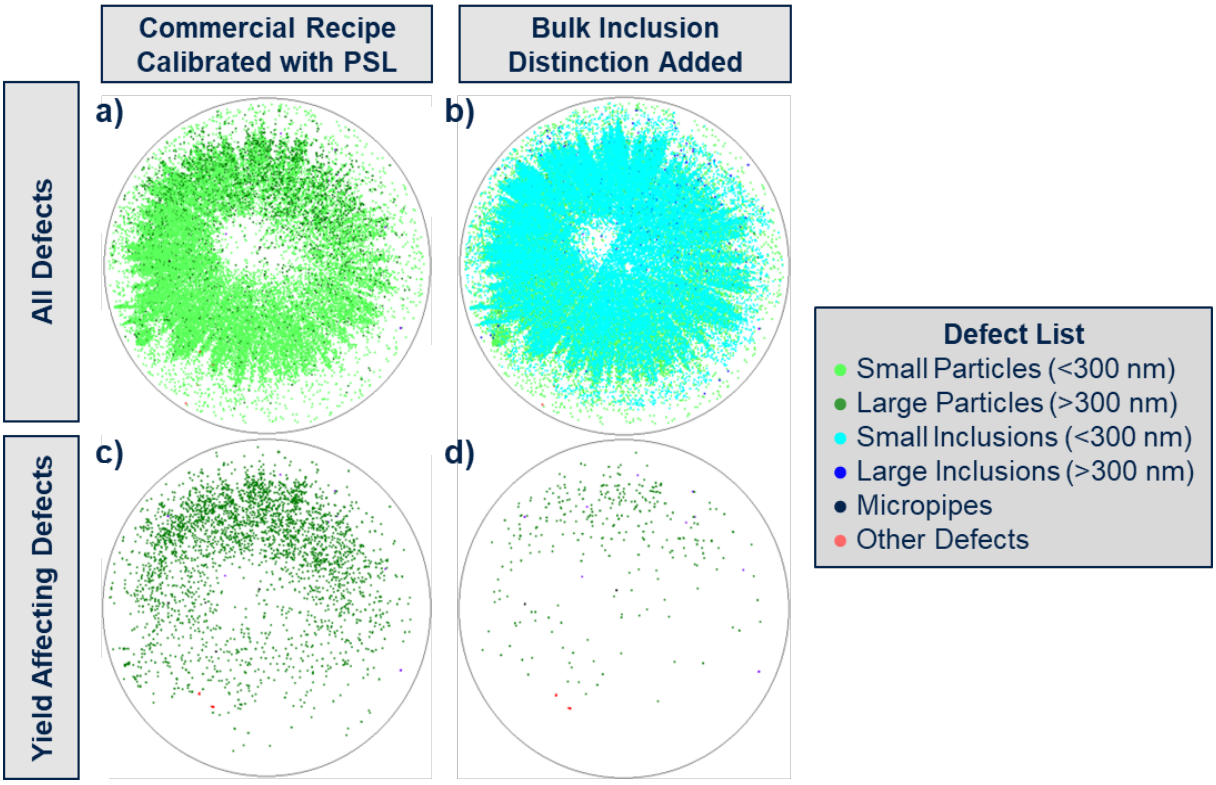

Fig. 4. A wafer severely affected by small and medium inclusions scanned with KLA Candela 8520, showing surface defectivity scan as seen a) using standard recipe calibrated with a PSL wafer and b) same scan but adding logic to improve distinction between surface and volumetric artifacts with c) and d) only showing the defects with high likelihood of affecting final yield.

the first 5-30 µm of a wafer surface, the interaction volume for the surface sensitive channels in commercial defect inspection tools, where the final inspection would be done for final grading. Many of these would give the same contrast signature as surface contaminations, even though they are inside the substrate volume, potentially causing wrongful classifications. While the ingot presented in this paper belongs to the outliers in terms of BIs density, this defectivity has been found in all major 4H-SiC N+ substrate suppliers at the time of writing.

Due to BIs size and position in the volume, it is difficult to accurately classify them, and they can even be mistaken for other defects. While this heavily depends on refractive index of the material, wavelength and angle of incidence of light sources, an example could be made for 4H-SiC N+ material with the tools used in this work, KLA Candela 8520 and Lasertec SICA88, having an interaction volume of roughly ~30 µm and ~5 µm, respectively, in the surface sensitive channels, see illustrative example in **Fig. 3**. A very common mis-binning is surface related defectivity, impurity particles or smaller voids, seen in **Fig. 3 a)** showing common defects as seen from a cross-view of a wafer volume and in **Fig. 3 b)** how different systems could misinterpret signals from BIs looking to the scattering normal channel, the surface sensitive channel most commonly used for cleanliness and surface condition determination.

The difficulty of distinguishing between the classification of surface contaminations and close-to-surface inclusions are exemplified in **Fig. 4**, showing a wafer that is highly affected by small and medium BIs. The center-symmetrical pattern of the distribution suggests crystallographic origin and not cleanliness related. However, automated grading systems will have difficulties making that distinction of the feature unless there is a well-trained image recognition module. Another approach is utilizing gaussian-filters specific to the ingot to assist in smoothing out the inclusion trends by removing such noise on post-scan data to get the real surface contamination.

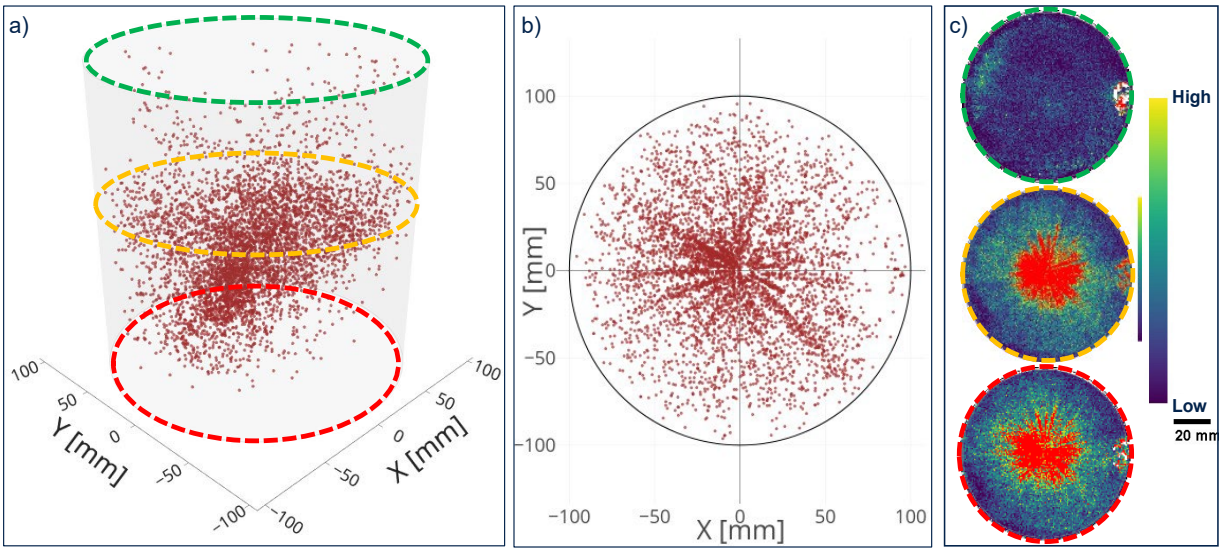

Fig. 5. Large Bulk inclusions (brown) as seen in a) an ingot b) projected to a 2D-plane with c) associated TSD maps. The green, orange and red rings in a) is a positional correspondence of the c) green, orange and red ring around the TSD maps.

Fig. 5 highlights another potential detrimental effect of BIs, specifically those categorized as slightly larger (>1 µm). In **Fig. 5 a)** we see an ingot volume highlighting the larger BIs along with three segments, green, orange and red, with corresponding TSD data collected with XRT in **Fig. 5 c)**. The final segment, encircled by red dash line in **c)**, has a TSD distribution that perfectly coincides with the 2D projection of all large BIs in the ingot, seen in **b)**. It is clear by superpositioning the 2D projection of large BIs, as seen in **b)**, with XRT data, that >95% of them generate their very own TSD. This TSD then continues to propagate from the point of the BIs, to the end of the dome. For medium and small BIs, the conversion-rate appears much lower.

Furthermore, it was hypothesized that an inclusion close to the wafer surface could affect the epitaxial growth due to local changes in thermodynamic driven surface diffusion. The local surface directly perpendicular to a void, close to the surface, could have a higher state of Gibbs free energy than the surrounding landscape due to changes in thermal conductance contributed by the void, its interface, and/or if the void is occupied by a different material, for example pure C. To verify this, a slightly thicker epitaxial layer, using standard 1200 V device conditions, was grown on two wafers, see **Fig. 6**, with slightly different localization of large BIs, wafer A and B, as seen in **Fig. 6 a)** and **d)**, respectively. Superpositioning of the epitaxial defects, seen in **Fig. 6 b)** and **e)**, with corresponding BI map, shows that large BIs close to the surface, at ~30 µm depth or less, tends to decorate the epitaxial layer with micropits at a very high conversion-rate. For small and medium BIs, the conversion is less likely to happen and requires the inclusion to be closer to the surface. Additional work needs to be done to fully understand the relationship between the latter two.

In **Fig. 6 c)** and **f)** the TSD maps of the wafers are also shown, pre-epitaxial growth, highlighting another example of how well TSD generation can be associated with BIs. TSD continues to propagate as TSD in epitaxial layers, a known phenomenon, and can increase the likelihood of leakage current in electronic devices [3, 4]. Micropits generated from sub-surface BIs can degrade most devices, showing that such sub-surface defectivity can be detrimental for device yields. The effect on longevity could also be a concern but requires further investigations.

Another significant consequence of larger voids and inclusions in the volume of 4H-SiC is hole-generation in thin 4H-SiC layers bonded on carrier substrates, i.e. polycrystalline 3C-SiC. If the layer thickness of the final bonded mono-SiC material is equal to or less than that of the diameter of an inclusion, a hole will be generated, creating a pathway directly down to the carrier substrate [5]. While the consequences of this depend on the nature of the carrier substrate, consecutive epitaxial growth and device yield are certain to be compromised as the defectivity generated will behave like that of a micropipe.

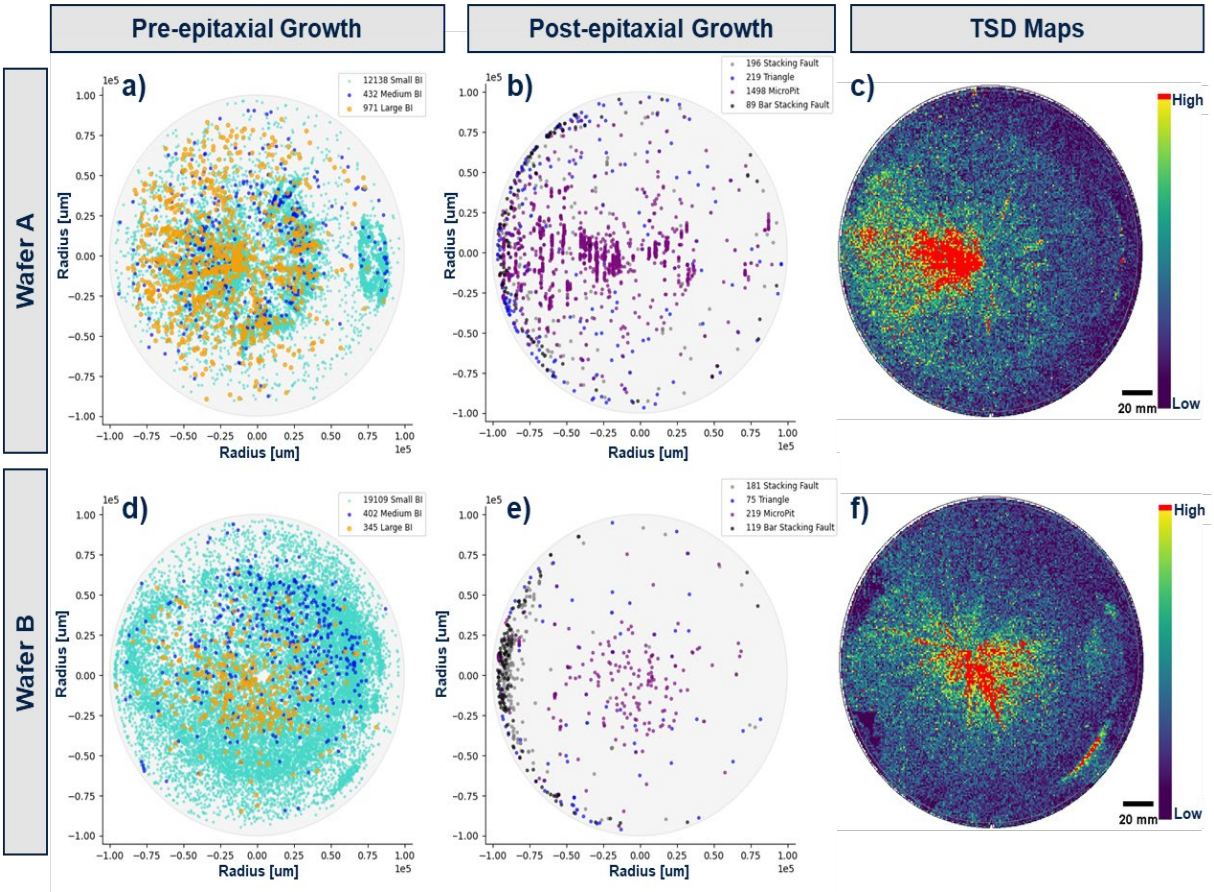

Fig. 6. Defectivity and dislocation maps of two wafers heavily affected by Bulk Inclusions seen before epitaxial growth, a) and d), after epitaxial growth, b) and e), and corresponding Threading-Screw Dislocation maps, c) and f).

Summary

Models based on empirical data pulled from thousand production and development grade wafers have been used to construct 3D visualization of BIs inside the volume. These aid in visualization of size, spatial and volumetric trends of BIs that can be directly linked to different crystal growth stages. The ability to pinpoint the defects sets the framework for which continuous studies can be done to understand the consequences on device yields. In this work it is already shown how BIs significantly affect dislocation generation, showing how all larger BIs (>1 μm) generate TSDs, and how BIs close to surface will decorate the epitaxial layers as micropits due to changes in the energy landscape on the surface above the BIs. The presence of BIs in commercial material is global, but the defect detection routines and procedures used today have not put emphasis on tracking this sort of defect yet. As the field progresses, pushes the limits of 4H-SiC crystal growth techniques, growth rates, thicknesses and, sizes, this type of defectivity will inevitably become more prominent.

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