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Advanced Defects Study and Monitoring in New Generation 4H-SiC Devices

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Abstract. A new design approach for 4H-SiC material is ongoing to improve the electrical performance of devices. As seen in silicon devices, multi-epitaxial growth enhances performance by reducing on-resistance (Ron). However, devices built on SiC face several challenges due to very low dopant diffusion (e.g., phosphorus and aluminum) and defect evolution during epitaxial growth. Monitoring defects like prismatic faults, stacking faults, partial dislocations, and micropipes, especially after regrowth, is essential to assess their impact on device performance. Defects with a high killer ratio must be closely tracked to understand their evolution. In this work, we will show a method for early-stage process characterization and defect root-cause identification through sensitive inspections, effective reviews, and accurate defect classification to detect critical defects in 4H-SiC material when more than one epitaxial step is considered.

Introduction

The global semiconductor market is expected to grow significantly. Considering the expansion to 8” wafer size and strong dedicated investments, the silicon carbide (SiC) power device market will reach $9B by 2028 [1]. This growth is driven by rising demand for efficient power electronics in electric vehicles (EVs), renewable energy systems (smart grids), IT infrastructures (AI, data centers), and other applications, thanks to the significant benefits over traditional silicon-based semiconductors. To achieve market leadership, semiconductor companies must quickly transition to high-volume manufacturing (HVM) with Zero Defect standards [2], preventing productivity bottlenecks during fab ramp-up. Sensitive inspection, effective review, and reliable AI-based defect classification during R&D and maturity phases are critical solutions for early detection of process flaws and killer defects, determining yield and accelerating time to result (T2R).

Coupling high-quality 4H-SiC substrates with an efficient epitaxial growth process is a promising approach to enhance the performance of power electronic devices [3,4,5,6]. Optical microscopy is the most widely used method for detecting defects in this technology, and defects are classified based on size, shape, and intensity. Typical macroscopic defects on SiC material (Figure 1), easily detectable due to their size and contrast, are considered killers for devices. More challenging defects, especially those smaller than 1 µm, require advanced characterization techniques such as inline defect detection and AI-based classification.

In Table 1, defects of interest are reported along with their typical electrical behavior. Micropipes act as conductive paths, increasing leakage current and decreasing blocking voltage. The

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characteristic hole that permeates the entire material, from the substrate to the epitaxy, causes a reduction in breakdown voltage and allows unexpected current to flow through the device during reverse bias. Typical hard failures are localized in active regions.

Threading Screw Dislocation (TSD) with pits generates inhomogeneities on the surface and on the gate oxide in MOSFET devices. They can cause a slight increase in leakage current and a local reduction in breakdown voltage. Additionally, oxide instability during electrical stress tests is detected. Such defects can expand under reverse bias stress, leading to hard failure of the device during standard operation.

Stacking Faults (SFs) are crystallographic defects without optical counterparts, detectable only by photoluminescence techniques. A recent and exhaustive classification is reported in [7]. Most SFs cause only a very slight increase in leakage current and are not directly connected with hard device failure. Nevertheless, if SF density exceeds a critical value, which strongly depends on the device considered, leakage current issues can become severe. In MOSFET devices, SF density should be kept below 0.5 cm^{-2}. Additionally, Single Shockley SF (1SSF) can expand via ultraviolet irradiation [8] and/or current flow, potentially inducing bipolar degradation and hard device failure.

Morphological and extended defects are recognized as responsible for electrical hard failures. Due to their typical size and shape, they are easily detected with optical methods and screened during the Front-End process flow.

In Figure 2, the high-sensitivity inspection mode is shown, and the results reveal an improved capture rate of sub-micron defects while confirming the macroscopic defects normally tracked by standard process control solutions. Another key element is the ability to perform 100% defect sampling classification, allowing precise correlation between the results from the final electrical test and the defect typology. In Figure 3, DefectWise® high-purity and high-accuracy, fully integrated classification technology is presented.

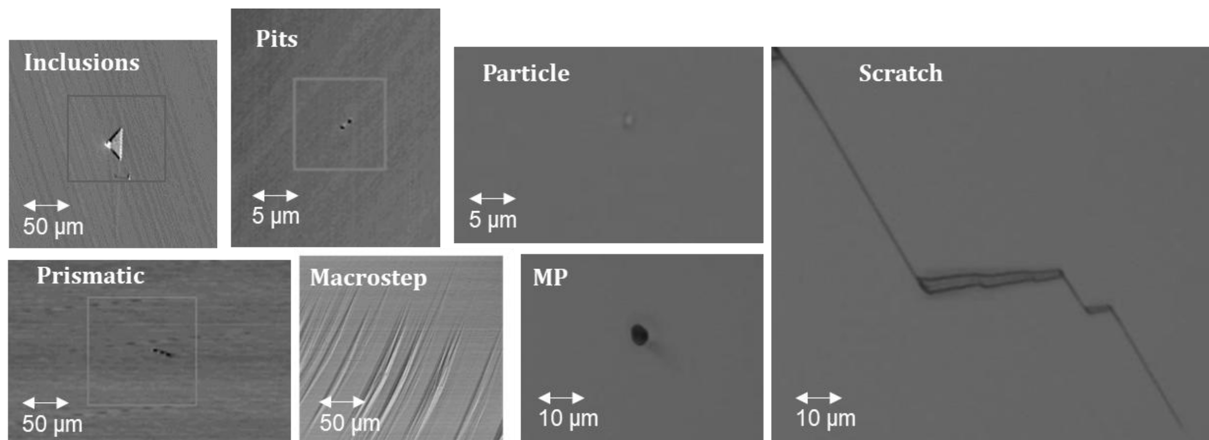

Fig. 1. Collection of morphological defects detected on SiC Epitaxial layer.

Table 1. SiC defects of interest.

Defect	Technique	Typical Size	Risk/Typical Failure
Micropipe	Optical microscope	~1 µm	**HIGH** Electrical Destructive Failure
Threading Screw Dislocation (with superficial pit)	Scanning electron microscopy X-Ray Topography Optical Microsocope + PL	< 1 µm	**MID/LOW** High Leakage Current and/or Oxide instability
Stacking Faults	Photoluminescence	> 1 µm	**LOW** High Leakage Current and/or Oxide instability
Morphological Extended Defects (Carrots, Triangles, Particles)	Optical microscope	>> 1 µm	**HIGH** Electrical Destructive Failure

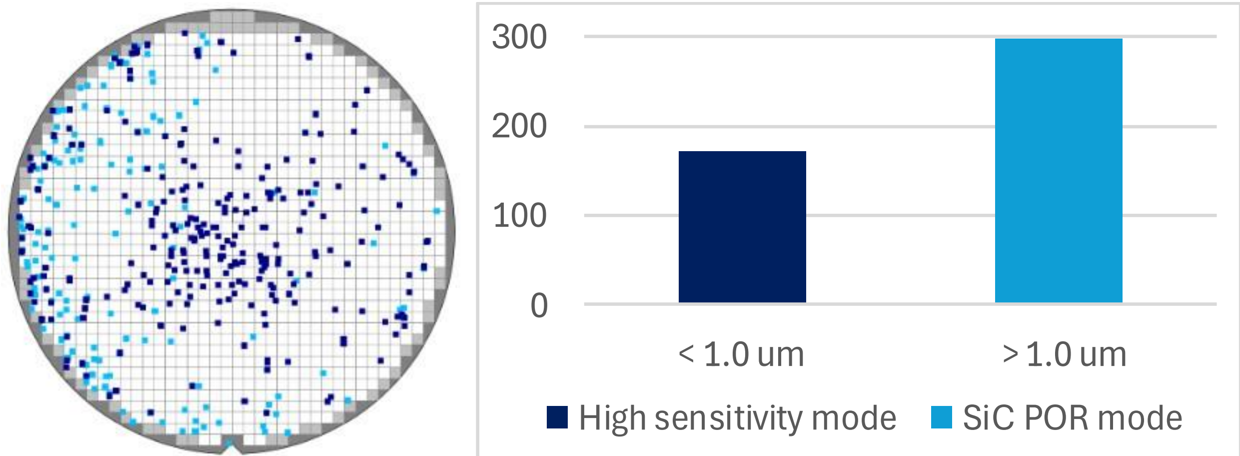

Fig. 2. Enhanced detection of sub-1μm defects in next-generation PMOS devices utilizing KLA's Corp's 20x high-sensitivity inspection mode on the 8935 inspector.

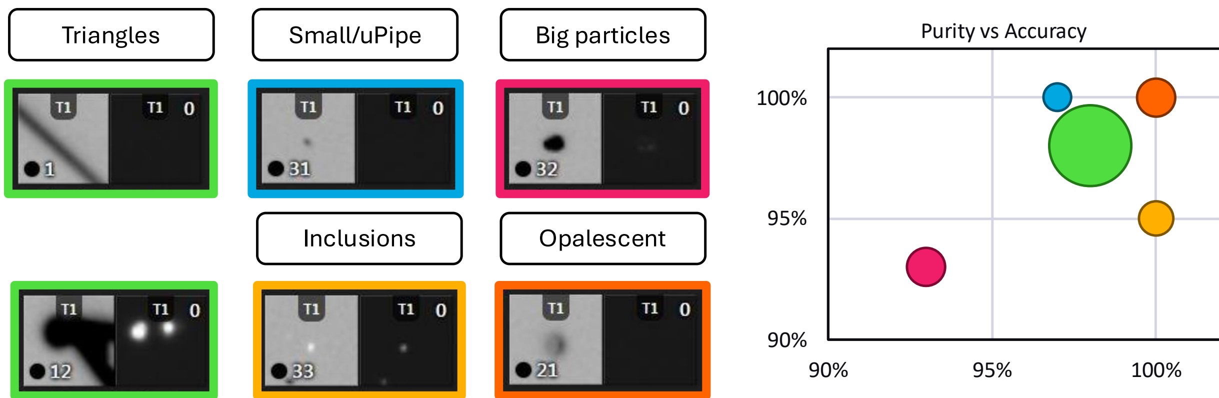

Fig. 3. Example of classification of common defects in SiC by using KLA's AI-based solution (DefectWise®).

Experimental

Multi-epitaxial growth is a strategy used to improve device performance, particularly in minimizing on-resistance (Ron) [9,10,11], thanks to superjunction-like drift layers. While this approach is common in silicon devices, SiC devices face challenges due to the low diffusion coefficients of dopants (e.g., phosphorus and aluminum) and the evolution of crystal defects during the multi-epitaxial process [12,13,14].

In Figure 4, a sketch of the epitaxial stack sent for inspection is shown. The first thick epitaxial layer, generally ranging from 5 to 10 µm, underwent ion implantation and was then epitaxially regrown with a thin layer ranging from 1 to 2 µm. Dedicated inspections were conducted to explore the interface quality between the epitaxial layers. The results (not presented here) showed a smooth interface free from defects generated by ion implantation.

Fig. 4. Sketch of epitaxial stack underwent to highly sensitive mode inspection.

In Figure 5, the typical increase in defectivity, depicted here as Defect Die percentage within a 5x5 mm grid, is shown. This increase is mainly due to the expansion of defects already present on the surface of the first epitaxial layer, new defects caused by surface contamination, and, to a minimal extent, dislocations propagated along the first epitaxial layer (e.g., basal plane dislocations) that convert into extended defects during the second epitaxial layer step (typically stacking faults and carrots).

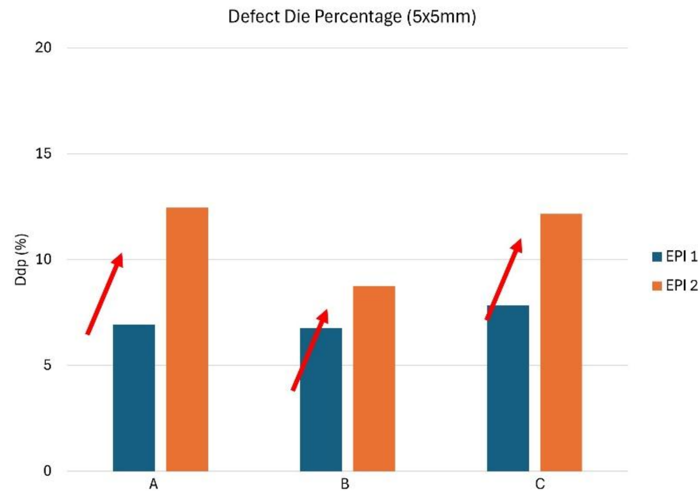

Fig. 5. Typical Increasing of Defect Die percentage (average ~ 4%) due to multi step epitaxial layer by considering three different substrate quality levels.

Figure 6 shows the evolution of defects from Epi1 to Epi2. To define the killer ratio (KR) of structured defects, it is necessary to detect and monitor defects after regrowth. Studies on prismatic defects and complex (carrots) stacking faults (Figure 6 A, C) provide insights into how defects propagate and the potential degradation of device performance. Additional partial dislocations after regrowth (Figure 6 B, D) must be detected, classified, and monitored to assess their impact on final electrical performance and process flow. Despite the limited size increase after the regrowth process, micropipes (Figure 6 E, F) are known to have a KR close to 100%, and their evolution is fundamental to identifying crystallographic changes and quantifying the portion of the surface impacted by their enlargement.

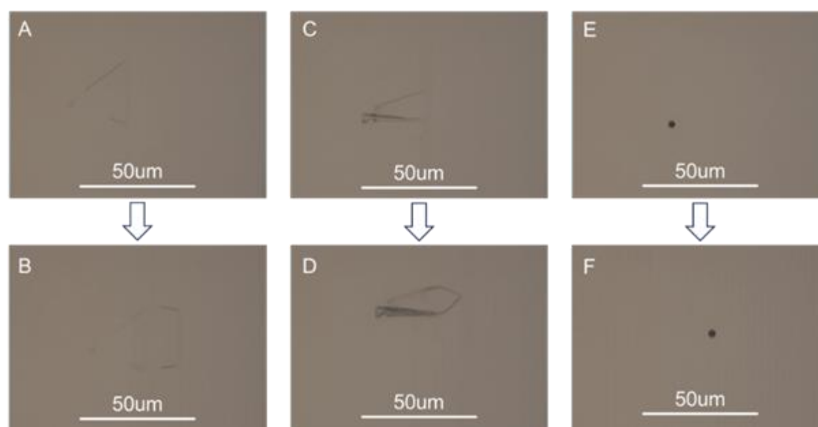

Fig. 6. Evolution of defects from the epitaxial layer (A, C, E) to thin epitaxial regrowth (Fig. B, D, F). In detail: evolution of prismatic (A→B), complex Stacking Faults (C→D) and micropipe (E→F).

The most relevant results were the efficient detection of submicron defects by optical means in high-sensitivity mode, as shown in Figure 7. Among all the submicron defects detected, the Threading Screw Dislocation (TSD) stands out due to the importance of screening such defects. Literature works [15] confirm that pits or nano-pits on the epitaxial surface, caused by the propagation of dislocations such as TSD, negatively affect device performance.

Usually, high leakage current in diode devices corresponds exactly with the presence of pits. In the case of MOSFET devices, the failure is even more severe, resulting in gate oxide breakdown and device burnout.

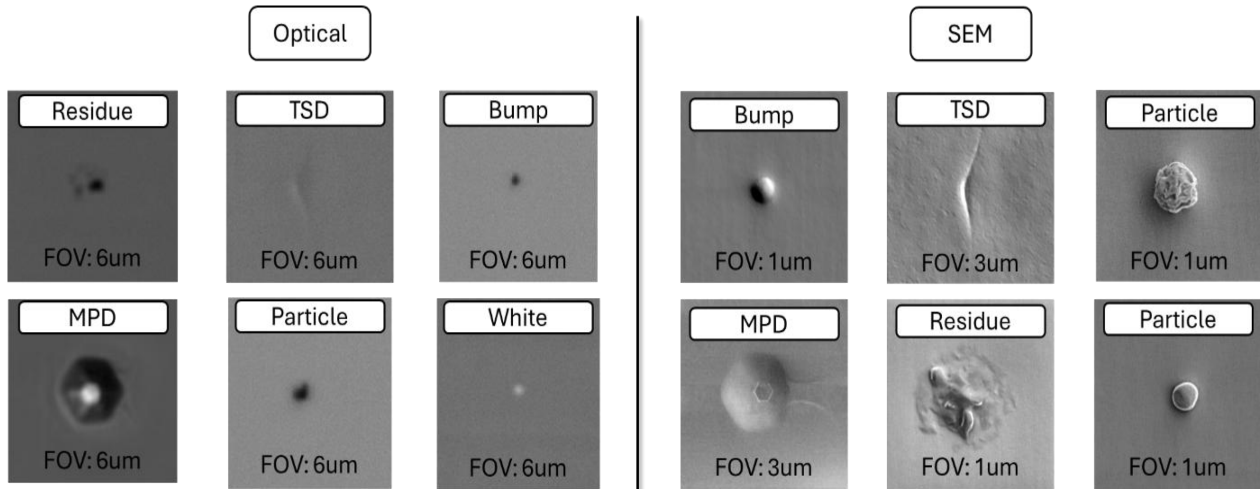

Fig. 7. Sub-micron defects detected by High Sensitivity mode inspection and related optical (Left) and SEM (right) review.

The **KLA 8935** high-throughput, high-sensitivity, top-side inspection system is designed for 150–300 mm bare and patterned wafers. It features a high-resolution, high-numerical-aperture optical microscope paired with an LED light source. A key capability of the system is its concurrent brightfield (BF) and darkfield (DF) inspection, which significantly expands its range of applicable use cases. The 8935 can be integrated with the DefectWise® deep-learning AI solution, enabling real-time 100% defect classification with high purity and accuracy.
The **Micro-SR™** fully automated optical review system operates in synergy with the 8 Series inspection systems. It is designed for high-throughput, high-resolution, high-quality image acquisition of sub-micron defects, supporting efficient defect review and analysis.
The **eDR7380™** electron-beam wafer defect review and classification system provides high-resolution images of defects and uses a machine-learning automatic defect classifier to produce an accurate defect Pareto. The data generated by the eDR7380 enables faster defect sourcing in development, quicker excursion detection, and more accurate, actionable data during production. The defect information produced by the eDR7380 helps accelerate time to market for multiple bare substrate types (SiC, GaN, glass, sapphire, POI piezoelectric-on-insulator, etc.) and device types (power, LED, photonics, RF, MEMS, etc.). Built on a flexible, configurable platform, the eDR7380 reviews and classifies a wide range of defect sizes and types for multiple wafer sizes (150–300 mm) and wafer thicknesses (180–1500 µm).

Results and Discussion

A new multi-epitaxial stack has been presented, and each layer is fully characterized. The use of higher magnification (20x) inspection mode significantly enhances the detection of sub-micron defects, while AI-based classification improves the accuracy and consistency of defect identification. This strategy enables effective tracking of defect evolution throughout the process.
Improvement in defect detection is mandatory in multi-epi technology because new defects triggered by the second epitaxial layer step can exhibit atypical and challenging characteristics from a metrology point of view, mainly due to the very low thickness of the second grown layer, which leads to very small defect sizes. TSDs that do not generate pits on the surface of the first epitaxial layer can do so on the surface of the second epitaxial layer, with a relatively small size (< 1 µm). SFs can be generated starting from BPDs that propagate through the first epitaxy up to the surface and appear very small in photoluminescence channels (< 10 µm).

Correlation between electrical testing and defect mapping highlights the importance of identifying high-impact defects, such as micropipes, which exhibit a strong killer ratio. The combination of high-resolution inspection, inline review, and precise classification supports the fine-tuning of next-generation power MOSFET development. Overall, this approach accelerates time-to-result while ensuring compliance with demanding industry standards.

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