Defect and Diffusion Forum
ISSN: 1662-9507, Vol. 452, pp 9-14
doi:10.4028/p-S58gNE

Submitted: 2025-09-09
Revised: 2025-12-17
Accepted: 2026-02-23
Online: 2026-05-18

Formation Mechanism and Reduction of Surface Pits on 4H-SiC Epitaxial Layer

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Keywords: 150 mm 4H-SiC, hot-wall reactor, surface pit.

Abstract. Surface pits in silicon carbide (SiC) epitaxial layers have a significant impact on various types of SiC devices, potentially causing electric field concentration and degrading device performance. The formation mechanism of surface pits remains unclear. In this work, the mechanism was investigated through the molten KOH etching experiments, and we confirmed that surface pits originate from dislocation defects in the substrate, particularly TSDs. The dislocations negatively impacted the step-flow growth of epitaxy, leading to pit formation. Further investigations into the effects of growth temperature, C/Si ratio, and epitaxial-layer thickness on pit formation revealed that low temperatures and silicon-rich conditions could effectively suppress pit formation. Both the density and size of surface pits increased significantly with the increase in epitaxial layer thickness. Therefore, this work proposes a model for the formation mechanism of surface pits, where the competition between step-flow growth and spiral growth is a key factor in controlling the size of surface pits.

Introduction

Compared to traditional silicon semiconductors, 4H-SiC offers revolutionary advantages in high-voltage and high-power applications, owing to its wide bandgap, high breakdown electric field, and high thermal conductivity [1]. With the accelerated popularization of new energy vehicles, the demand for 4H-SiC power devices in automotive applications has been increasing.

For the fabrication of 4H-SiC power devices, chemical vapor deposition (CVD) is one of the key technologies to conduct the homo-epitaxial growth. Nowadays, the defects in epitaxial layers remain a primary challenge in device fabrication, as epitaxial layer defects adversely affect the reliability of 4H-SiC power devices. With the continuous development of 4H-SiC epitaxial technology, killer defects (such as triangular defects and carrot defects) have been effectively controlled and significantly reduced [2,3]. However, the impact of non-killer defects (e.g., surface pits) on 4H-SiC devices has gradually become apparent, potentially increasing leakage current and causing long-term reliability issues [4,5]. Thus, understanding the formation mechanisms of surface pits and thus decreasing formation during the epitaxial process is crucial, which could effectively enhance device reliability.

In this work, we investigated the origin of surface pits and explored the influence of epitaxial process parameters on surface pit density during the growth of 4H-SiC epitaxial layers on 150 mm 4° off-axis substrates using a hot-wall horizontal single-wafer reactor. By optimizing key process conditions (such as the carbon-to-silicon (C/Si) ratio and growth temperature), high-quality 4H-SiC epitaxial wafers with low surface pit defect density were successfully achieved, and the formation mechanism of surface pits was revealed. This research holds significant scientific and engineering value for advancing the large-scale application of 4H-SiC epitaxial materials in high-voltage and high-power devices, as well as for improving device reliability.

Experimental

The epitaxial growth was conducted using a horizontal hot-wall reactor. Trichlorosilane (TCS) and ethylene (C_2H_4) served as the silicon and carbon precursors, respectively. Hydrogen (H_2) was used as both carrier and dilution gas, while nitrogen (N_2) was employed for n-type doping. Homoepitaxial growth was performed on commercial 150 mm, 4° off-axis n-type 4H-SiC substrates with an off-cut orientation towards <11-20>. Substrates from the same manufacturer, ingot, and with closely matched lot numbers were selected for comparative experiments to eliminate performance variations caused by substrate quality differences. The TSD density of all substrates used was controlled within the range of 200–400 cm^{-2}. The epitaxial process temperature varies between 1550°C and 1650°C, and the chamber pressure was maintained at 100 mbar. The introduced C/Si ratio was varied by C_2H_4 gas flow rate, while keeping the TCS flow rate constant.

A SICA88 instrument was used to analyze the number and distribution of pit defects with a 3 mm edge exclusion. Thickness of 4H-SiC epitaxial layer was evaluated by Fourier-Transform Infrared spectroscopy (FTIR) with 5-mm edge exclusion. These measurements were performed along the radial direction because the thickness showed concentric distribution.

Results and Discussion

Molten potassium hydroxide (KOH) treatments were performed on the epitaxial layer to investigate the origin of surface pits. Defect inspections were conducted at identical locations on the same substrate, the same epitaxial wafer, and the epitaxial wafer after KOH treatment. Using the synchronous positioning function of SICA88, differences in defects at the same positions were compared. The correlation between pit defects on the epitaxial wafer and defects on the substrate was investigated, as illustrated in Fig.1. When examining the same location on the substrate (Fig.1(a)), no microscopic defects were observed at the position where pit defects appeared on the epitaxial wafer surface (indicated by arrows in Fig.1(b)). However, after KOH treatment, dislocation defects in the substrate were exposed at precisely the same position on the epitaxial wafer (Fig.1 (c)). This indicated that the pit defects did not originate from surface microscopic defects of the substrate, but rather from dislocation defects in the substrate. The dislocation defects likely propagated from the substrate to the epitaxial layer during the epitaxial process, and common dislocation defects in the substrate include threading edge dislocations (TEDs), threading screw dislocations (TSDs), and basal plane dislocations (BPDs) [6]. Based on the morphological characteristics of the etched pit, the dislocation defect shown in Fig.1(c) was likely TSDs or TEDs, rather than the BPD [7]. Based on the differences in the Burgers vectors of TSDs and TEDs, their etched pit morphologies vary significantly. The etched pits formed by TSDs showed a hexagonal structure and they were considerably larger than those formed by TEDs [8]. Therefore, as illustrated in Fig.1, the pit defects on the epitaxial wafer originated from the TSD defects in the substrate. The step-flow growth (along the <11-20> direction) dominated the epitaxial growth of 4H-SiC. If TSDs are present in the 4H-SiC substrate, spiral growth (non-<11-20> direction) would occur at the TSD sites, resulting in the formation of surface pits.

According to the identification of the correlation between surface pits and substrate dislocations, the effects of growth temperature, C/Si ratio, and epitaxial layer thickness on the formation of surface pits were investigated to reduce pits density. Under a fixed C/Si ratio of 0.8, 4H-SiC epitaxial layers with a thickness of 10 μm were grown at temperatures of 1570℃, 1590℃, 1620℃, and 1650℃, respectively. This was to investigate the effect of growth temperature on surface pit defects. The results, as shown in Fig.2(a), indicated that the density of surface pits decreased significantly with decreasing growth temperature. This might be because the low temperatures suppress the spiral growth of dislocations, thereby reducing the formation of surface pits. Moreover, we explored the role of the surface C/Si ratio in pit formation. The growth temperature was fixed at 1570℃, while C/Si ratios of 0.8, 0.9, 1.0, and 1.1 were employed during epitaxial growth of a 10 μm-thick epitaxial layer. The results presented in Fig.2(b) demonstrated that the surface pit density decreased as the C/Si ratio was reduced. The underlying mechanism is that a lower surface C/Si ratio suppresses the spiral growth of dislocations [9], thereby effectively reducing the formation of pit defects.

Additionally, the evolution of pit size as the thickness increases was studied to investigate the formation of pit defects. Under the conditions of a C/Si ratio of 1.0 and a growth temperature of 1570℃, 4H-SiC epitaxial layers with varying thicknesses (6 μm, 12 μm, 30 μm, and 60 μm) were prepared to investigate the influence of epitaxial thickness on surface pit defects. As revealed in Figs.2(c) and 2(d), both the density and size of surface pits increased significantly as the epitaxial layer thickness increased. Based on the detection resolution of the SICA88 surface defect inspection system, the number of pits within different surface size ranges was compared across layers of different thicknesses (see Table 1). The results showed a gradual increase in the total number of detected pit defects and the number of large-sized pits, with increasing epitaxial layer thickness. This indicated that pit defects enlarged progressively during epitaxial growth until they reached the resolution limit of the inspection equipment and became detectable. Given that the pit defects originated from TSDs in the substrate, it could be concluded that the initial density of TSDs in the substrate were the fundamental factor determining the final number of pit defects in the epitaxial layer.

Finally, based on the origin of surface pits and the effects of growth parameters on these pits, we proposed a model of the formation mechanism of surface pits (Fig.3) [10]. The formation of surface pits essentially stemmed from the competition between step-flow growth of dislocations and spiral growth of dislocations. The dynamic balance between these two growth directly determined the size of surface pits. This mechanism underlying the interaction between step-flow growth and spiral growth is similar to that of micropipes formation [11]. The size of pits along non-<11-20> direction increased when spiral growth of dislocations dominates. For the step-flow growth prevails, spiral growth of dislocation was suppressed, leading to a significant reduction in the size of pits non-<11-20> direction. The size of pits along the non-<11-20> direction primarily determined the overall size of the pits. The pits with a size over the detection resolution of the SICA88 inspection system could be detected. Under low-temperature or silicon-rich growth conditions, the spiral growth at TSD dislocations was suppressed, which reduced the average size of the pits, thereby decreasing the density of surface pits.

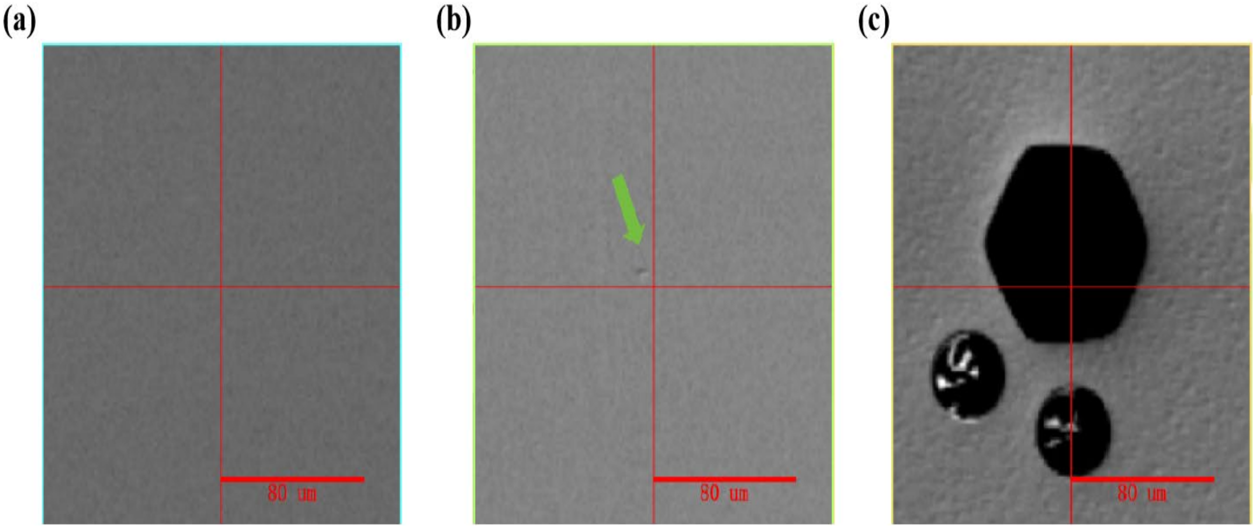

Fig. 1. The surface morphology of (a) the substrate and (b) the epitaxial wafer, and (c) the epitaxial wafer after KOH treatment. All surface morphologies were taken from the same location by SICA88.

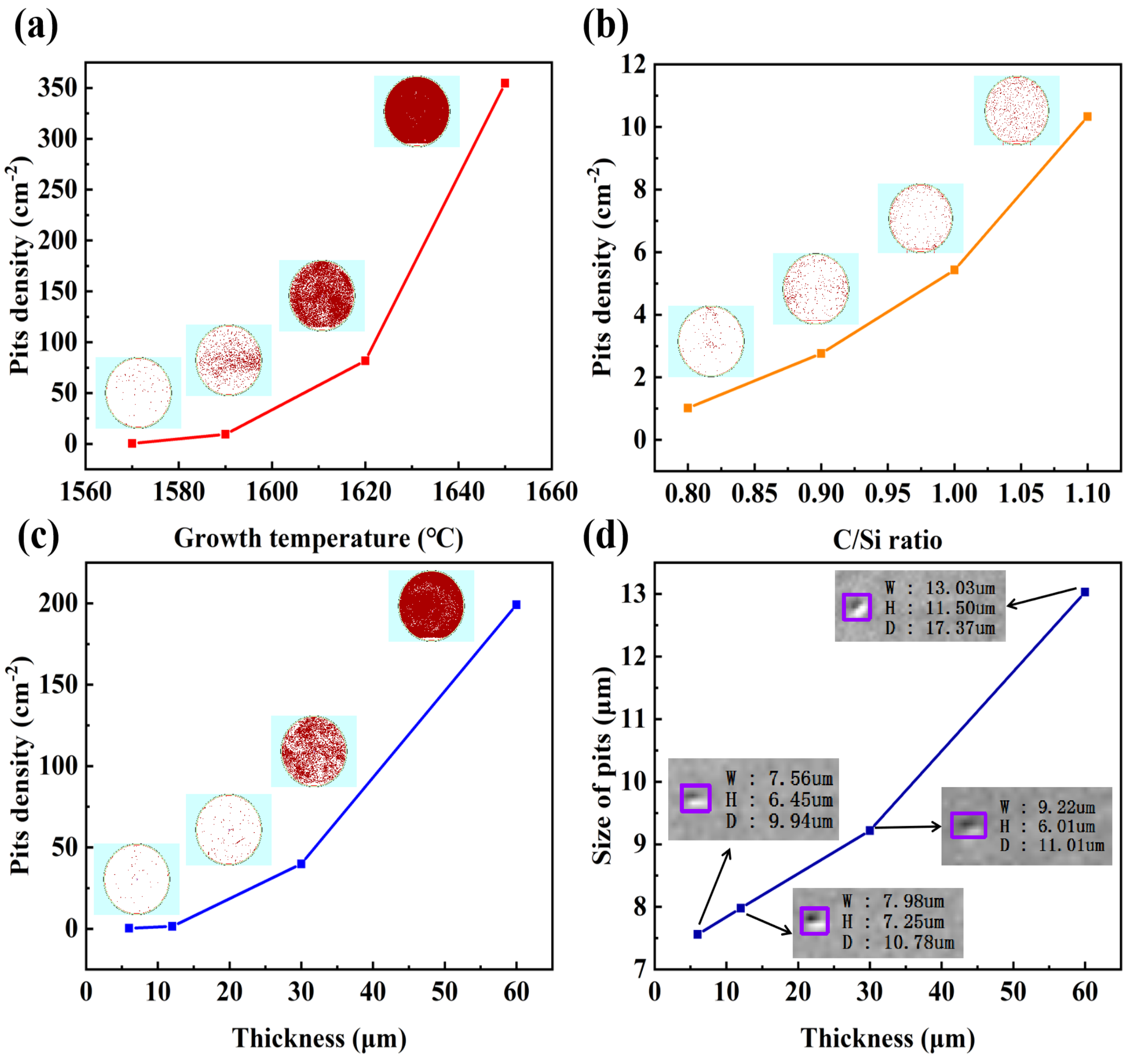

Fig. 2. Effect of different (a) growth temperature, (b) C/Si ratio and (c) growth thickness on the pit defect density; (d) Size of pit defects at different growth thicknesses.

Table 1. The number of pits versus their size on epitaxial layers with different thicknesses (by SICA88).

Thickness	Total number of pits	Number of pits (<100 μm^2)	Number of pits (100~250 μm^2)	Number of pits (250~1000 μm^2)
6 μm	53	42	11	0
12 μm	236	182	47	7
30 μm	6504	6237	241	26
60 μm	32477	24909	7505	63

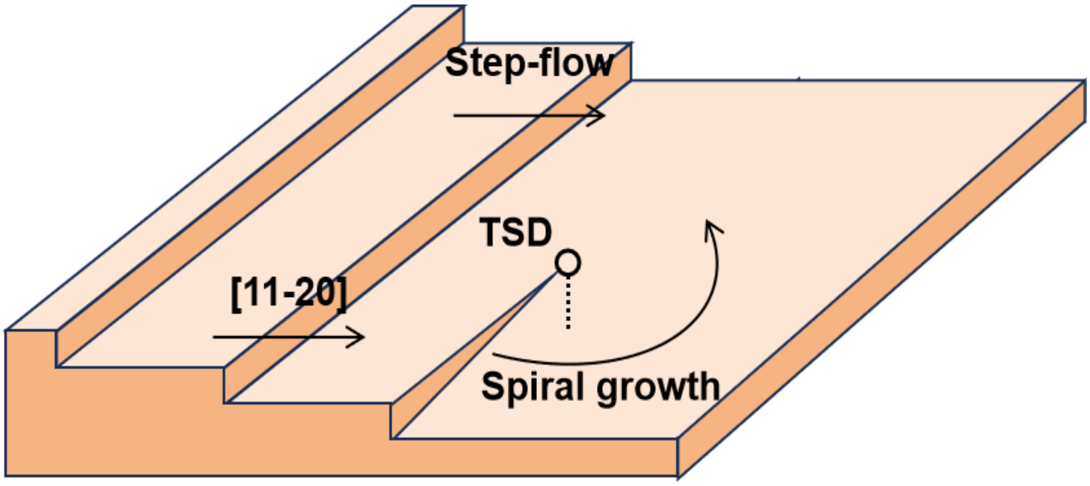

Fig. 3. Schematic illustration of the proposed model of the formation mechanism of surface pits.

Summary

This work systematically investigated the origin of surface pits in 4H-SiC epitaxial layers and their dependence on epitaxial growth parameters. Experimental results indicated that surface pits primarily originate from TSDs in the substrate. There was a spiral growth during the epitaxial process, leading to the formation of surface pits. By adjusting growth conditions (e.g., reducing temperature or the C/Si ratio), the formation and expansion of pits could be effectively suppressed. Furthermore, as the epitaxial layer thickness increased, both the density and size of the pits gradually increased, indicating that the pits undergo continuous evolution during growth. Based on these findings, a mechanistic model was proposed, showing the role of competition between step-flow growth and spiral growth of TSD in regulating pit morphology. This work provided a theoretical understanding and practical guidance for optimizing the SiC epitaxial processes, especially suppressing surface pits. It would offer a significant value for improving the performance of SiC devices.

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