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Unveiling the Role of Crystallographic Defects in SiC Device Reliability with Multi Modal Structural Analysis

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Abstract. The fabrication of high-quality 4H-SiC epitaxial layers for power semiconductor devices involves complex processes including bulk crystal growth, wafer slicing, polishing, and chemical vapor deposition (CVD) epitaxy with precise step-flow control on slightly off-cut Si-face substrates. Despite advances, intrinsic crystallographic defects such as threading dislocations, basal plane dislocations, and stacking faults remain significant challenges, propagating into epitaxial layers and degrading device performance and reliability. This study examines defect types and their impact on 4H-SiC wafers, emphasizing the transition from 150 mm to 200 mm substrates, which introduces increased defect densities and polytype inclusions. Comprehensive defect characterization using advanced microscopy, molten KOH etching, and electrical wafer sorting reveals strong correlations between physical defects-such as micropipes, carrot-like stacking faults, and triangular 3C-SiC inclusions-and device failures, particularly under reliability stress tests like High Temperature Reverse Bias (HTRB). The findings highlight the critical role of substrate quality, epitaxial growth conditions, and defect mapping in improving yield and device robustness. This work underscores the necessity of integrating multi-scale defect inspection and targeted reliability assessments to optimize 4H-SiC power device manufacturing and performance.

Introduction

The fabrication of standard 4H-SiC wafers typically involves multiple stages: initially growing a bulk SiC crystal, followed by slicing this crystal into individual wafers, polishing the wafer surfaces, and finally conducting epitaxial layer growth. At present, CVD remains the exclusive method for producing 4H-SiC epitaxial layers (epilayers) used in power semiconductor devices. Achieving high-quality homoepitaxial layers that preserve the 4H-SiC polytype relies on a technique known as "step-flow control." This method uses substrates cut at a slight angle—generally a few degrees off the {0001} basal plane—allowing the atomic stacking sequence to replicate along the advancing atomic steps [1]. Currently, wafers with a silicon-terminated (Si-face) surface and a 4° off-cut are predominantly utilized in the manufacture of 4H-SiC Schottky barrier diodes (SBDs) and metal-oxide-semiconductor field-effect transistors (MOSFETs). The standard CVD process employs hydrogen (H_2) as the carrier gas, silane (SiH_4) as the silicon precursor, and propane (C_3H_8) as the carbon source. Alternatively, chlorine-containing gas mixtures—either by supplementing the standard gases with hydrogen chloride (HCl) or by using chlorine-based precursors—are also employed to modify growth conditions [2-3-4-5]. To meet device design requirements, the epitaxial layers must exhibit tightly controlled thickness and doping profiles, with uniformity maintained both

across individual wafers and between different wafers. One of the current industrial challenges is to develop techniques capable of producing 200 mm diameter 4H-SiC epilayers that combine excellent uniformity with minimal defect densities. Additionally, increasing the epitaxial growth rate or shortening the overall production cycle is desirable to boost manufacturing throughput.

Despite improvements, commercially available 4H-SiC substrates still contain significant densities of crystallographic defects, including threading dislocations and basal plane dislocations (BPDs). Threading dislocations are classified by their Burgers vectors: threading screw dislocations (TSDs) have Burgers vectors of either c or c+a, while threading edge dislocations (TEDs) possess Burgers vectors of a/3. Basal plane dislocations share the Burgers vector a/3 [6-7-8]. Those threading dislocations with a c+a Burgers vector are often termed threading mixed dislocations (TMDs). During epitaxial growth, these dislocations propagate into the epilayer, with some altering their orientation or transforming into partial dislocations that generate Shockley Stacking Faults (SFs) [9] induce Frank-type stacking faults, prismatic defects, or complex stacking fault structures (commonly referred to as carrot-like defects) within the epitaxial layer, all of which impair electrical characteristics [10-11].

Historically, micropipe defects were a major concern in SiC wafers, but advances have reduced their density to below 0.1 cm^{-2}. Consequently, the focus has shifted toward dislocations and epitaxial growth-related defects, which now represent the primary obstacles to device reliability. While industrial inspection techniques efficiently detect most defects, dislocations remain challenging to identify comprehensively. Therefore, understanding the formation, propagation, and impact of these defects is vital, particularly regarding their role in device degradation after reliability stress.

Results and Discussion

The role of extended crystallographic defects as electrically active centers promoting leakage current, electric field crowding, and premature breakdown in 4H-SiC power devices is well established [12]. Threading dislocations, micropipes, basal plane dislocations, and stacking faults have been shown to directly trigger degradation and catastrophic failure under high-voltage and high-temperature stress conditions. In the following, we experimentally correlate specific defect types with device failure modes observed after electrical stress.

The ongoing transition from 150 mm to 200 mm diameter SiC substrates introduces new challenges. Unlike 150 mm wafers, 200 mm substrates exhibit slightly increased densities of propagated stacking faults (bar-shaped SFs) and polytype inclusions [13-14].

In typical 150 mm commercial substrates, the density of TSDs ranges from about 2×10^{2} cm^{-2}, TEDs $<1.5\times10^{3}$ cm^{-2}, and BPDs $< 3\times10^{2}$ cm^{-2}, while micropipe are nearly eliminated. In 8 inches the density of TSD is $<2.5\times10^{2}$ cm^{-2}, TED$<2.5\times10^{2}$ cm^{-2}, BPD $<6\times10^{2}$ cm^{-2} and micropipes <0.1 cm^{-2}.

Monocrystalline SiC substrates have been employed to investigate defect impacts on device performance. Reliability evaluations are indispensable in semiconductor manufacturing, designed to assess device robustness and longevity under various stress conditions. These tests are tailored to specific device technologies and anticipated failure modes. Among the standard reliability tests are High Temperature Reverse Bias (HTRB), High Temperature Gate Bias (HTGB), Dynamic Reverse Bias (DRB), and Body Diode Stress (BDS). These tests collectively inform lifetime and durability models.

Beyond process-induced electrical failures such as threshold voltage instability caused by suboptimal MOS interfaces [15], it is crucial to assess the influence of epitaxial defects on MOSFET device reliability. Failure analysis of 650 V MOSFETs post-reliability testing employs Emission Microscopy (Em.Mi.) to localize failure sites. Following localization, device layers are chemically stripped to expose the SiC surface, which is then subjected to molten KOH etching to reveal underlying defects. The etching process is conducted at 500°C for 10 minutes, followed by optical microscopy for defect classification and correlation with electrical failures. This approach, optimized for n-type epitaxial layers with doping levels near 1.6×10^{16} atoms/cm^{3}, provides reliable defect identification [16-17]. SiC wafers undergo comprehensive defect inspection using specialized inline metrology tools to identify defect-affected areas. These defects may be intrinsic to the material (e.g.,

carrots, comets, pits) or induced during processing. While process-related defects are linked to fabrication steps and screened accordingly, intrinsic defects require detailed classification to establish their correlation with device failure, quantified by the killer ratio.

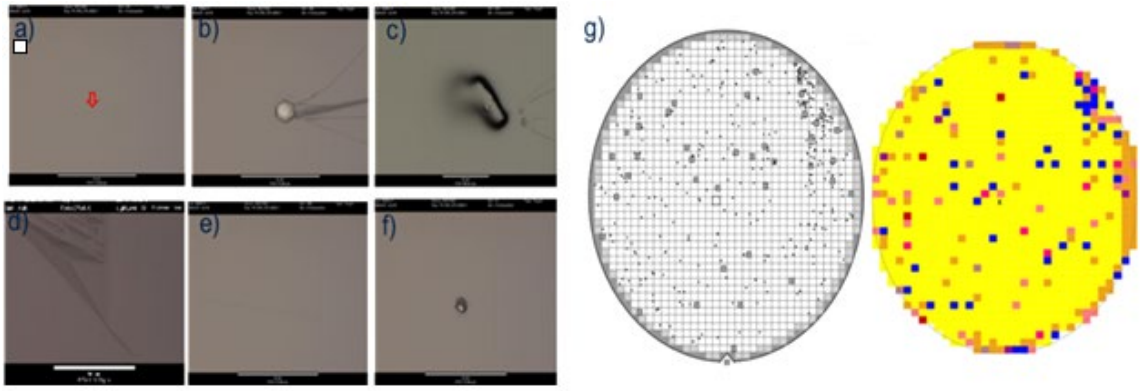

Fig. 1. (a-d) Altair images showing, a)micropipes, b-c-d) triangles, e) carrot, f) particle. g) Comparison demonstrating the overlap between the defect map output from Altair and the EWS map.

Key metrics such as Defective Die Percentage (DDP) and Total Usable Area (TUA) are employed to evaluate manufacturing yield and efficiency. Tools like Candela and Altair (KLA) utilize optical microscopy and scatter light methods, respectively, tailored for SiC inspection. Despite methodological differences, these tools generally show good agreement in defect detection, especially for surface and epitaxial defects including particles and micropipes. However, many buried substrate defects such as TSDs and BPDs evade detection by conventional methods, necessitating advanced techniques like X-Ray Topography (XRT), which is gaining recognition as a reliable, non-destructive tool for dislocation density measurement.

Material quality assessment often involves mapping device-sized grids to quantify defect impact via DDP after epitaxial growth. This metric predicts the expected failure rate per wafer. Testing wafers outside specification limits helps determine killer ratios for specific defect types.

Figure 1 reports many typical epitaxial defects detected through Altair inspection. Micropipes (Figure 1a), characterized as hollow-core screw dislocations, originate during ingot growth and extend through the wafer thickness, severely compromising device performance. Their evolution during Physical Vapor Transport (PVT) growth is intricate and not fully controlled. Attempts to mitigate micropipes via buffer layer optimization during epitaxial growth have not yielded significant reductions in device failure rates, especially concerning MOSFET blocking voltages. Consequently, micropipes remain a critical substrate-level issue. Triangular defects (TD) appear in three main morphological forms: TD-I, which features grains at its apex (Fig. 1b); TD-II, distinguished by micro-pits (Fig. 1c); and TD-III (Fig. 1d), characterized by a washboard-like surface texture. These defects arise from various causes, including foreign particles, micropipes within the substrate, and threading edge dislocations, all of which interfere with the epitaxial growth process. Comprehensive investigations employing techniques such as laser confocal microscopy, molten KOH etching, microwave plasma etching, Raman and photoluminescence spectroscopy, as well as high-resolution transmission electron microscopy, have shown that these defects consist of 3C-SiC polytype inclusions or Frank-type stacking faults. The interfaces between the 3C and 4H polytypes display both coherent and periodic arrangements, with twinning phenomena notably present in TD-III [18]. The development of these triangular defects is strongly associated with substrate flaws and irregularities in growth conditions, resulting in localized changes in polytype and stacking sequences. [19-20]. Complex stacking fault formations, historically termed carrot defects (Fig. 1e), mainly result from TSD propagation, though single or paired BPDs can also initiate such defects. This is supported by observations of BPD signatures following KOH etching of carrot defects. Fig. 1f reports the case of a particle embedded in the crystal at the end of epitaxial growth.

Aligning the Optical Microscopy (OM) map with Electrical Wafer Sorting (EWS) bins involves matching physical defects detected on the wafer surface, such as micropipes, stacking faults, and contamination, with the electrical test results assigned to each die. The colors on the EWS wafer map correspond to the different EWS bins, visually representing the electrical classification of each die. By ensuring both datasets share the same coordinate system and overlaying the OM defect map onto the colored EWS bin map, it becomes possible to identify correlations between defect locations and electrical performance variations or failures. This alignment facilitates effective root cause analysis, process improvements, and yield enhancement by directly linking specific physical defects to their electrical impact, thereby improving the quality and reliability of 4H-SiC power devices [21].

Both Candela and Altair (KLA) maps reveal elevated concentrations of epitaxial defects such as stacking fault complexes, topographic irregularities, and surface triangles adjacent to polytype regions. These defect clusters correlate strongly with EWS maps, where they cause catastrophic device failures as underlined by the superposition reported in Fig. 1g.

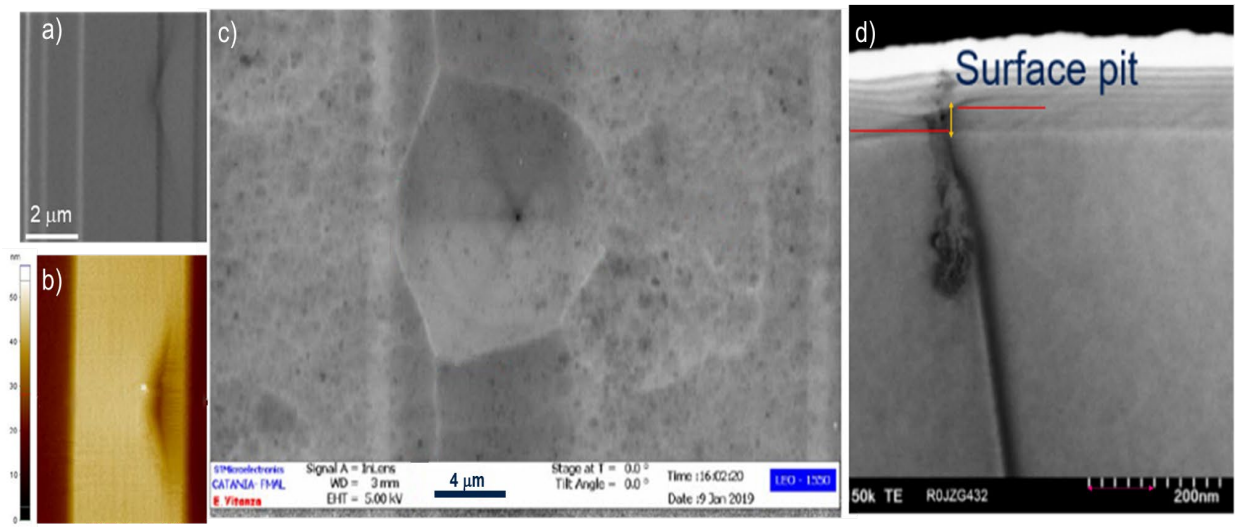

Fig. 2. a) SEM image displaying a V-shaped feature on the surface of the TSD. b) AFM image in the same region c) SEM image providing a detailed view of the pit formed by the TSD. d) Cross-sectional TEM image revealing the presence of the threading dislocation at the surface.

Reliability testing, particularly HTRB, is extensively used to probe failure mechanisms and improve device robustness. HTRB involves applying reverse bias near maximum rated voltages and currents under elevated temperatures to stress device junctions, following JEDEC standards for power devices. In this study, devices were subjected to 520 V reverse bias at 140°C for 30 hours. Devices failing this test underwent detailed failure analysis. Em.Mi. images highlighting failure locations post-HTRB, with emission spots indicating regions of high leakage current within various device areas depending on electrical configuration. Emissions detected in IDSS mode often correspond to epitaxial layer defects.

Following device delayering, surface morphology was examined via SEM and AFM (Fig. 2(a-b)). High magnification SEM images in Em.Mi. hot spots reveal the pit V-shape typical of TSDs arising from substrate [22]. AFM identifies surface pitting consistent with step flow irregularities caused by threading screw dislocations during growth. These shallow depressions evidenced by AFM analysis of about 20 nm depth vary with growth conditions and can cause localized electric field crowding, degrading device performance and potentially leading to failure. SEM analysis particularly elucidated the emergence of a cone shape formed by the TSD as large as 3 µm (Fig. 2c) and cross TEM analysis observations TSDs in 4H-SiC crystals reveal that TSDs propagate roughly along the c-axis but often exhibit non-straight, winding dislocation lines with occasional deflections generating confirming the presence of surface pit. KOH etching at the die level confirmed the association between device failure and TSDs (Fig. 2d).

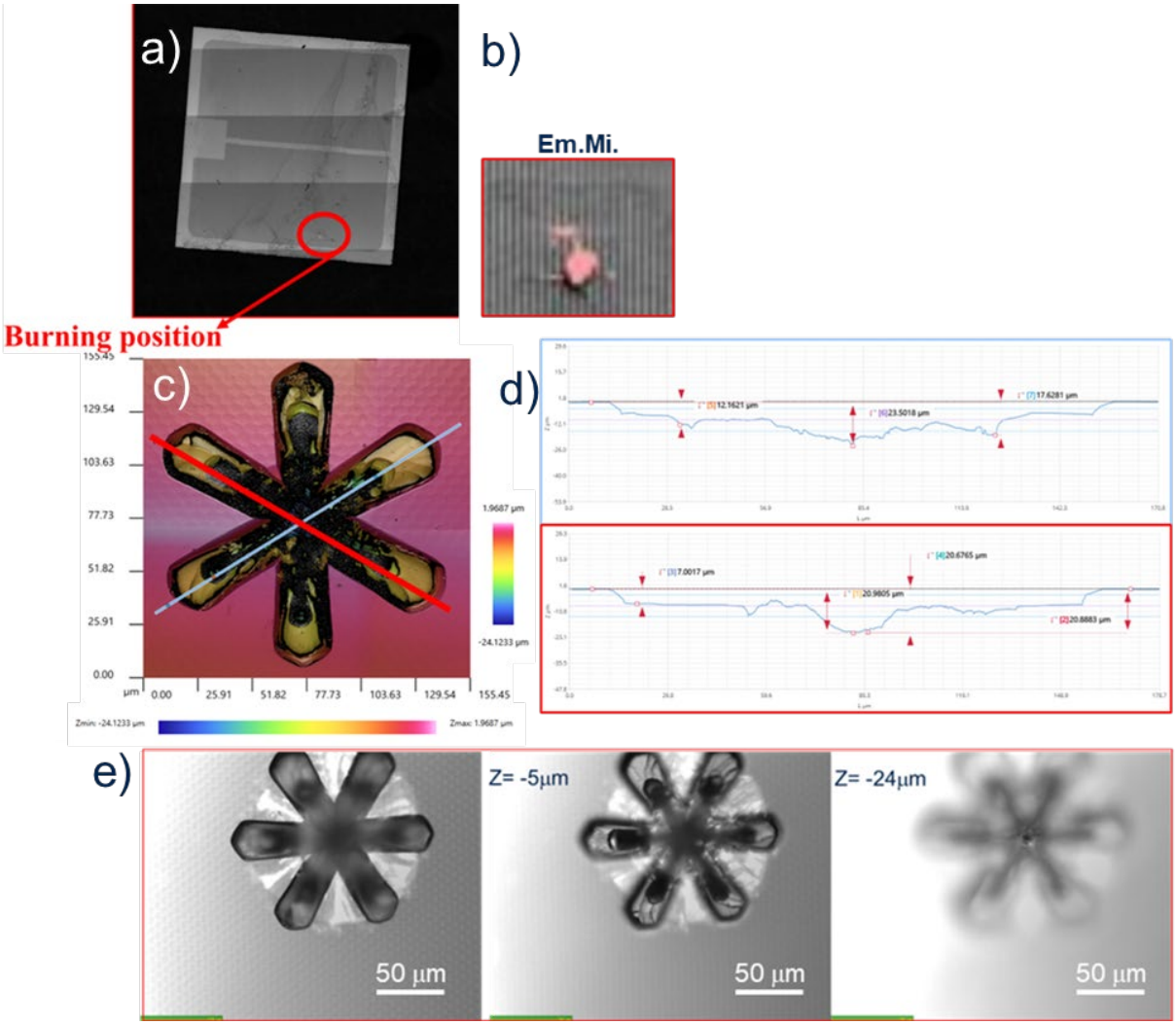

Fig. 3. a) shows a die with the burn location highlighted in red, as identified by Em.Mi analysis in b). The optical profilometer image (c) reveals the hexagonal shape of the burn spot after molten KOH etching. The blue and red profiles illustrate the burn's lateral extent and increasing depth toward the center (d). Optical microscopy (e) captures the defect at various focal planes, clearly indicating that the burn originates from a micropipe, evidenced by the defocus observed at -24 µm.

Molten KOH etching is a cost-effective, destructive method for dislocation density assessment. Conducted at 500°C in a nickel crucible, etching times are adjusted based on doping levels, differing between substrate and epitaxial layers. This technique effectively reveals dislocations that critically influence device reliability.

The detection of defects such as micropipes reveals that micropipe etch pits are significantly larger than those associated with threading screw dislocations (TSDs), primarily due to the larger Burgers vector of micropipes. Fig. 3 illustrates a hard device failure caused by a crystallographic defect. Leakage currents measured between drain-gate and gate-source terminals reveal short circuits. Em.Mi. pinpoints the emission site (Fig 3b), and subsequent chemical delayering exposes a hexagonal hole at the defect location. Optical profilometry analysis (Fig. 3c) further confirmed that these defects exhibit a hexagonal symmetrical structure aligned with the crystallographic axes. Profiling along marked lines (Fig. 3d) showed that the micropipe etch pits extend approximately 180 µm in diameter, with edge depths ranging from 2 to 7 µm, gradually tapering toward the center. In Fig. 3e Bright-field optical microscopy provided additional confirmation by revealing a distinct hole characteristic of micropipes when the focal plane was adjusted approximately 24 µm below the sample surface. Together, the hexagonal etch morphology and the observed subsurface hole definitively identify the defect as a micropipe determining localized high current density and thermal damage.

Conclusion

This comprehensive review underscores the critical importance of defect inspection in SiC wafer production, particularly focusing on the identification and characterization of killer defects that significantly impact device performance and yield. The article systematically categorizes the diverse crystallographic and surface defects inherent to SiC wafers, such as threading screw and edge dislocations, basal plane dislocations, micropipes, stacking faults, and polytype inclusions, detailing their origins, morphologies, and detrimental effects on various SiC power devices including MOSFETs, Schottky diodes, and p–n junctions. A broad spectrum of inspection techniques, ranging from destructive methods like KOH etching and transmission electron microscopy to advanced non-destructive optical and electron-based modalities such as photoluminescence, X-ray topography, Raman spectroscopy, and mirror projection electron microscopy are increasingly becoming essential in terms of their resolution, throughput, and applicability for in-line production environments. The review highlights the complementary nature of these methods and advocates for integrated inspection systems that combine high-resolution imaging with rapid scanning capabilities, enhanced by machine learning algorithms for automated defect classification and mapping.

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