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# Evaluation of Switching Performances and Short Circuit Capability of a 1.2 kV SiC GAA MOSFET through TCAD Simulations

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**Abstract.** Silicon Carbide (SiC) is a leading material for power electronics due to its high critical electric field, rapid switching, and high-temperature capabilities. This study delves into the dynamic and thermal performance of a novel SiC power MOSFET, utilizing an innovative vertical Gate All Around (GAA) design. Through detailed 2D TCAD simulations in cylindrical coordinates, the device's behavior is analyzed across various pillar radii and temperatures. Results indicate that while reducing the pillar radius does not improve the on-resistance ($R_{ON}$), a 500 nm radius is required to achieve $R_{ON} < 10$ mΩ·cm². Additionally, larger pillar radii significantly increase capacitance. The device exhibits strong switching performance comparable to commercial counterparts and benefits from the absence of a termination region. However, its short-circuit ruggedness is compromised, particularly in structures with smaller pillar radii, where delayed thermal runaway failure is observed. Notably, for a 20 nm radius, the temperature peak occurs on the Drain side, a deviation from typical behavior. Despite its advantages, the design's low short-circuit capability remains a limitation.

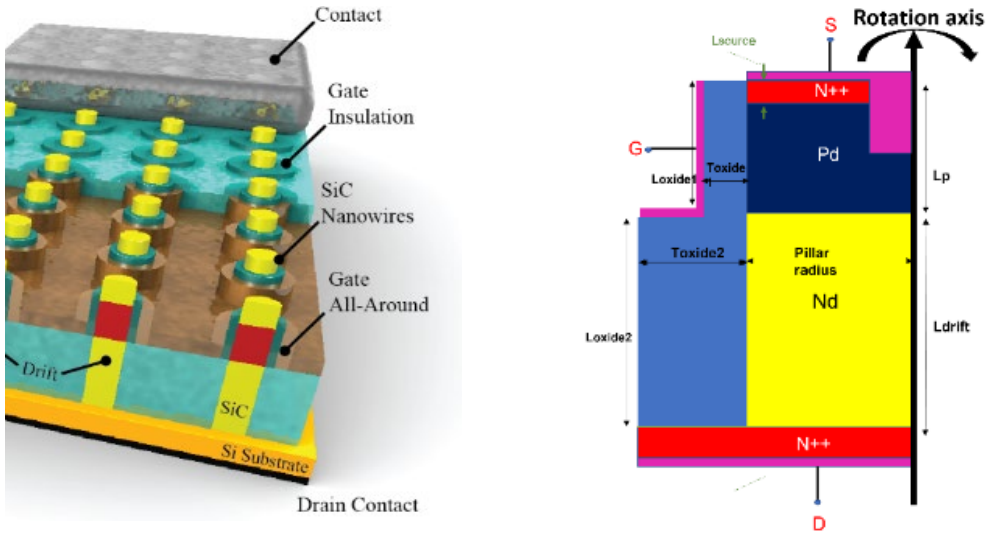
## Introduction

The next generation of power electronic devices must deliver high energy efficiency and power conversion density to accommodate the market requirements. Silicon Carbide (SiC) is emerging as the leading semiconductor for these applications due to its superior critical electric field, fast switching speeds, and ability to operate at high temperatures. SiC's impressive performance, compared to traditional silicon (Si), drives ongoing efforts to improve SiC device quality. With its wide bandgap, high electron mobility, and excellent thermal conductivity [1], SiC offers significant advantages, although several technological challenges remain to fully harness its potential. In terms of device design, literature presents various approaches for creating high-voltage SiC MOSFETs, primarily focusing on either planar or trench gate designs for the active section. The bulk section typically utilizes either a constant doping profile drift layer or super-junction and semi-super-junction methods. However, all these designs require a termination region, which is crucial in determining the device's breakdown voltage (BV) and occupies a significant portion of the device area, thus contributing substantially to the overall cost. Moreover, the termination region introduces challenging aspects related to the passivation layers that may affect the reliability of the device.

In this work, the recently introduced SiC power MOSFET [2], based on an innovative vertical Gate All Around (GAA) concept, is further explored with a focus on its dynamic and thermal performances. The study begins with a thorough evaluation of the device's thermal behavior, providing crucial insights into its operational stability under various conditions. Following this, an extensive series of TCAD simulations is conducted to examine the device's performance during switching operations and under short-circuit conditions. These simulations aim to assess the potential advantages and limitations of the GAA design, contributing valuable data for optimizing future SiC power MOSFET technologies.

## The Proposed Device

A sketch of the proposed device is reported in Fig. 1a. The overall device is composed by many N-type SiC cylindrical pillars surrounded by silicon dioxide (the single cell), in cellular parallel mode connection. The pillars are grown starting from a n+ Si substrate, connecting all pillars to the same Drain region. The available technology, the selective epitaxial growth of SiC on masked Si bulk (See [3]), allows the growth of the 3C-SiC. In this work it is assumed that the pillars are in 4H-SiC, to evaluate the best performances with this design. The top P-Body layer is surrounded by the Gate oxide layer, connected to the Gate contact. In this work the Gate oxide in made by Silicon Dioxide to evaluate the performances of the device with standard materials. To the active area of the device contributes both the pillar and the surrounded oxide. Therefore, in this work the ratio among the pillar area and oxide area will be calculated from the geometry reported in Fig. 1b, where $L_1 = 2(r + T_{OXIDE})$ and $T_{OXIDE} = Toxide1$. Further design details are reported in Table I. The geometry of the single pillar (See Fig. 1b) allows a suitable TCAD simulation by using cylindrical coordinates, therefore a 2D mesh is considered to evaluate the performance of the 3D structure. Standard physical models are adopted to run numerical simulations and only fixed charges are considered at the $SiC/SiO_2$ interface. When the radius of the proposed structure is lower than tens of nanometers, a very accurate description of the channel mobility is mandatory [1], therefore the MLDA model is used to model the channel electron density by quantum mechanical equations [5]. The length of the Drift region (L) is 7µm to allow a Breakdown Voltage (BV) of about 1300 V, *without the presence of a termination region*. Finally, all the numerical results reported in this work refer to a structure where the Source region is connected to the P-Body region through an ohmic contact, laying on the symmetry axes.




a) b)

**Fig. 1** a) A sketch of the overall SiC GAA MOSFET design concept. b) A sketch of the TCAD structure and geometrical parameters.

**Table 1.** Design parameters

| | |
|---|---|
| Toxide1 | 50 nm |
| Loxide1 | 0.7 μm |
| Toxide2 | 0.2 μm |
| Lch | 0.5 μm |
| Ldrift | 7 μm |
| Nd | $1.1*10^{16}$ $cm^{-3}$ |
| Pd | $4*10^{17}$ $cm^{-3}$ |

**Simulation Results and Discussion**

In Fig. 2 the sub-threshold slope and the threshold voltage, calculated starting from the $J_D$-$V_{GS}$, are reported for different radius at ambient temperature. A peculiar behavior of the Vth occurs: it decreases when the radius decreases until 25 nm, but it increases when the radius is lower than 25 nm. Therefore, the variation is not monotone. In the same way, the sub-threshold slope of the $J_D$-$V_{GS}$ curve is not monotone: for a radius higher than 75 nm the slope increases, while it quickly decreases for lower pillar radii.

Both the peculiar behaviors are due to the balance between the oxide capacitance and the depletion capacitance in the channel region [1]. Simulations for a pillar radius of 2 μm for T = 300 K and T = 450 K, show a weak dependence on the temperature.

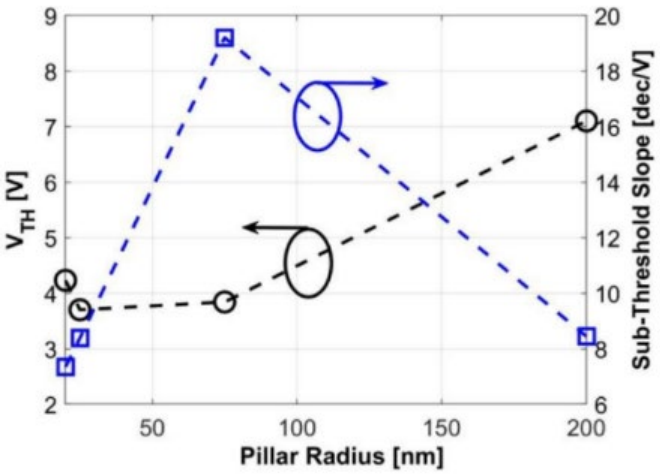



**Fig. 2** Sub-threshold slope and threshold voltage dependence on the pillar radius.

In Fig. 3 the output curves are reported up to 500V and it is visible as the reduction of the pillar radius does not improve the $R_{ON}$. It is visible as even if the saturation current increases for high $V_{DS}$ > 300V for a 20 nm pillar radius, this does not lead to the improvement of the $R_{ON}$, since the Drain current is negligible compared to the Drain current for $V_{DS}$<100V. The main reason comes from the fact that the more the pillar radius decreases, the more the section oxide area percentage increases (See Fig. 4). This leads to the reduction of the SiC section useful for the conduction. This leads to the increase of the resistance, that is inversely proportional to the section of the pillar.

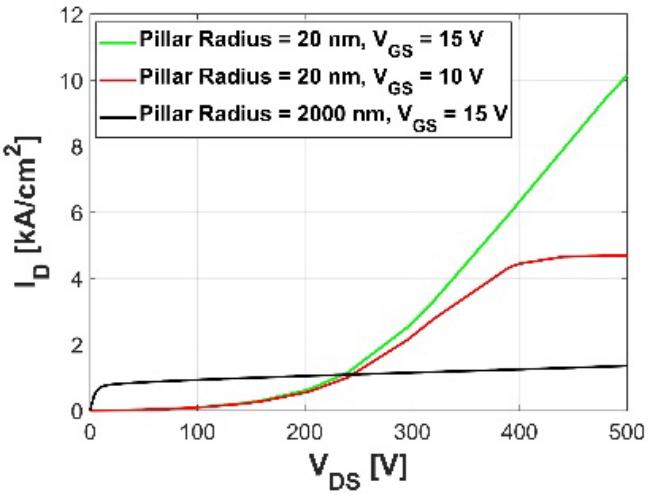



**Fig. 3** Output curves for pillar radius equal to 20 nm ($V_{GS}$= 15 V and $V_{GS}$ = 10 V) and 2 μm ($V_{GS}$ = 15 V).

The Ron dependence on pillar radius and temperature is detailed in Fig. 4, where in the inset the geometrical features of the device are reported. A pillar radius of 500 nm is mandatory to have $R_{ON}$ < 2 mΩ·cm$^2$. As reported above, it is clear as the geometrical distribution of the pillars modifies the $R_{ON}$ dependence on the pillar radius. As an example, the more the oxide thickness is reduced, the more the $R_{ON}$ decreases, by keeping constant the area of the device.

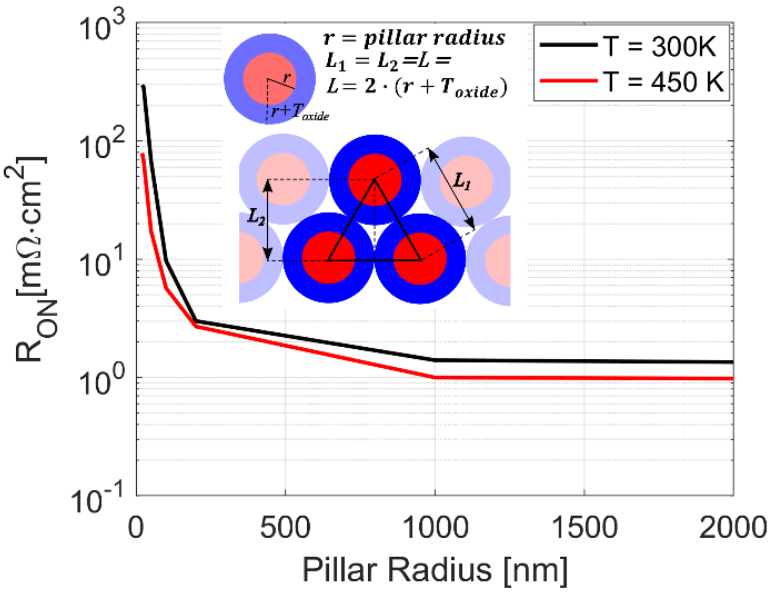



**Fig. 4** On-resistance value for different pillar radius for two temperatures. In the inset the geometrical distribution of the pillars to evaluate the $R_{ON}$.

In Fig. 5 the capacitances of the structure with 20 nm and 2 μm are reported. It is visible as the capacitance strongly increases for a larger pillar radius. The active area is 1cm$^2$ and $I_{ON}$ = 60 A. The reduction of the pillar radius leads to an abrupt decrease of the overall capacitance.

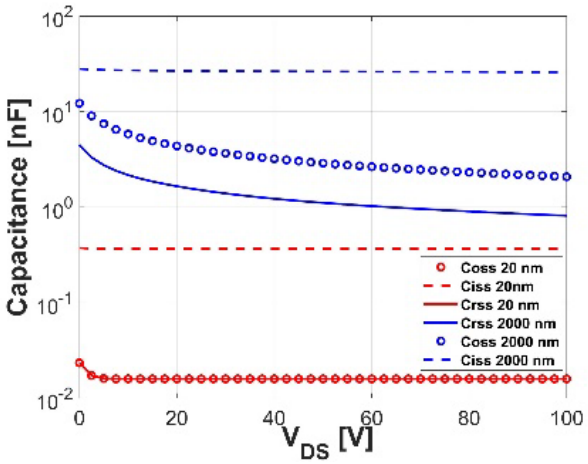



**Fig. 5** Ciss, Coss, and Crss values for pillar radius of 20 nm and 2 μm.

On the other hand, for a pillar radius of 20 nm, the Miller plateau is much higher compared to one of 2 μm. A complete overview of this effect is reported in Fig. 6. It is visible as for a very low pillar radius, both $E_{OFF}$ and $E_{ON}$ arise. For higher pillar radius values, the performances are comparable to the structure in [6]. This happens even if the static capacitances in Fig. 5 show higher values for higher radius.

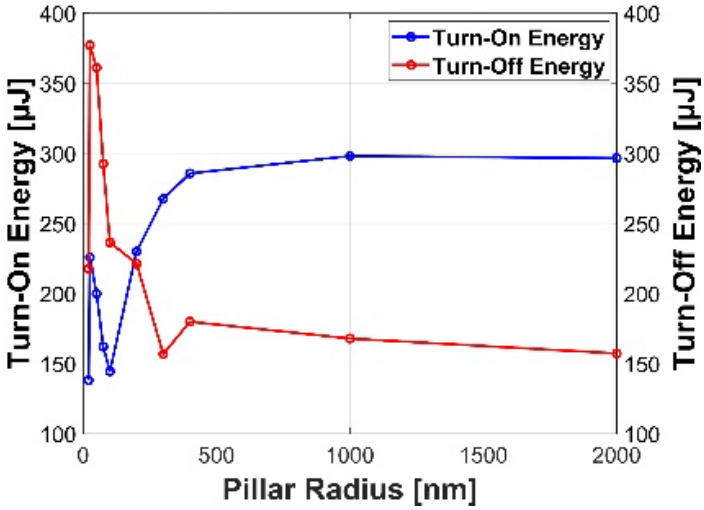



**Fig. 6** Turn-off and turn-on energy dependence on the pillar radius. T=300K, $I_D$ = 20A.

Finally, the short circuit capability was evaluated through electro-thermal simulations. In Fig. 7 both the Drain current and the maximum temperature are reported for a pillar radius of 20 nm and 2 μm. As expected, the structure does not show a short-circuit ruggedness, since the great portion of silicon oxide. For 1 μm, even if the current turns off, the temperature does go to zero, leading to delayed thermal runaway failure. Both structures do not withstand a short circuit pulse with a duration of 1 μs. For the pillar radius of 50 nm, the temperature abruptly arises to very high values.

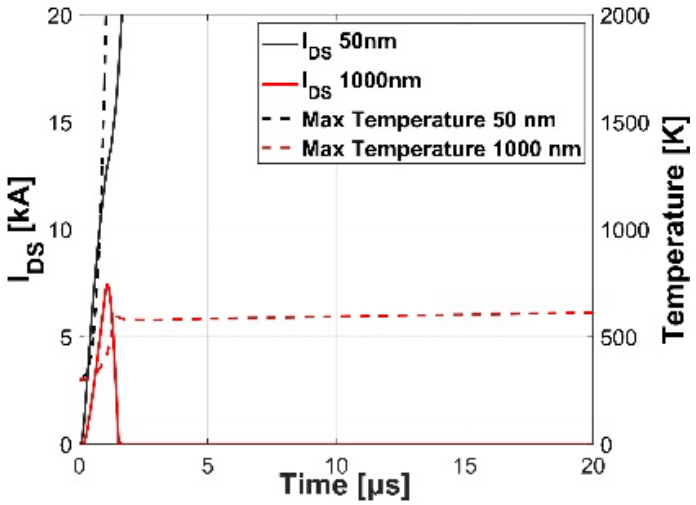
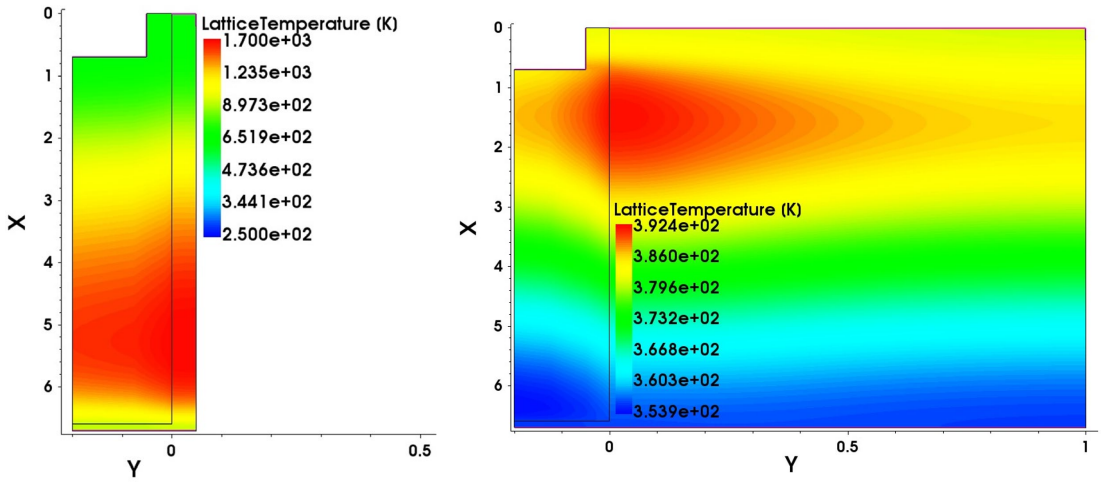



**Fig. 7** Short circuit waveforms for two pillar radius values.

An interesting effect occurs during the short circuit for the 20 nm pillar radius structure, where the temperature peak occurs on the Drain side instead of the P-Body side (See Fig. 8). The peak temperature for the small radius device occurs on the Drain side, while for the larger structure the temperature peak occurs below the P-Body region, as expected. Therefore, the proposed structure has switching performances comparable to commercial devices with similar rates and has the advantage of the absence of a termination region. On the other hand, the structure shows a very low short circuit capability.




a) b)

**Fig. 8** Temperature distribution at the end of the 1 ms pulse into the a) 50 nm structure and the b) 1 µm.

## Summary

In conclusion, the SiC power MOSFET with a vertical Gate All Around (GAA) design shows strong switching performance and removes the need for a termination region. However, TCAD simulations highlight challenges, particularly with the device's on-resistance ($R_{ON}$), which is highly dependent on the pillar radius, with a 500 nm radius necessary for $R_{ON} < 10$ mΩ·cm². Additionally, larger pillar radii lead to increased capacitance, affecting performance. The device also shows limited short-circuit ruggedness, especially in designs with smaller pillar radii, where delayed thermal runaway failure is observed. Notably, for a 20 nm pillar radius, the temperature peak occurs on the Drain side.'

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