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Impact of Positive and Negative High Voltage Gate Stress on Channel Degradation in SiC MOSFETs

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Abstract. The effects of positive and negative high voltage gate stress on the interface trap density and channel conductivity of lateral, Si-face 4H-SiC MOSFETs is studied, and the possible physical mechanisms for interface trap generation are discussed. Charge pumping and I_D-V_{GS} measurements are used to measure the trap density and field-effect mobility, respectively. The time dependence of the channel degradation is evaluated for different stress voltages with oxide electric field exceeding 8 MV/cm. Positive stress is shown to generate acceptor traps which degrade the field-effect mobility, and the density of traps follows a universal dependence on the injected electron fluence into the gate oxide. In contrast, negative stress resulted in no degradation of the field-effect mobility even as interface trap density increased, indicating that only donor interface traps are created. Furthermore, the trap density during negative stress does not follow a universal dependence on the injected hole fluence, indicating that other mechanisms are responsible for the trap creation.

Introduction

To ensure long-term reliable operation of SiC power MOSFETs, it is critical to understand safe operating conditions and the effects of gate voltage stress on device performance and defectivity, during both operation and testing. Recently, the evolution of the threshold voltage (V_T) of SiC MOSFETs during positive high voltage gate stress (HVGS), wherein the oxide electric field exceeds the threshold field for impact ionization, has been evaluated. It has been routinely observed that a large negative V_T shift occurs when the gate is stressed at oxide fields over ~8 MV/cm [1]–[3], which is attributed to the trapping of holes in the bulk of the SiO_2 gate oxide after being generated by impact ionization and/or anode hole injection [3]–[6]. More recently, the charge pumping (CP) technique [7], [8] was used to show that the interface trap density (N_{it}) also increases during HVGS, thereby degrading the MOS interface [9]. In this work, we continue these investigations by studying the evolution of both N_{it} and field-effect mobility (μ_{FE}) during positive as well as negative HVGS on lateral test MOSFETs using I_D-V_{GS} and CP measurements, revealing the practical impact of HVGS on device performance and providing insight into the possible physical mechanisms responsible for the interface degradation.

Experimental Details

The devices used for this study were lateral test MOSFETs fabricated on 4° off-axis 4H-SiC epitaxial wafers. The implanted acceptor concentration (N_A) in the channel is 2×10^{17} cm^{-3} and the MOS interface is formed on the Si face by thermal oxidation followed by NO annealing. The MOSFET channel length and width are 8 μm and 200 μm, respectively. This channel length was long enough to ensure the channel resistance was the dominant resistance during I_D-V_{GS} measurements to allow extraction of an accurate value for μ_{FE}, but also short enough to avoid significant geometric current during CP measurements [7], [8]. A schematic cross section of the test MOSFET is shown in Fig. 1(a), along with an illustration of the gate voltage stress and measurements sequence in Fig. 1(b). Each MOSFET was stressed at a certain gate voltage sufficiently high to induce impact ionization in the oxide, which is well beyond the recommended operating conditions of the device (oxide field >

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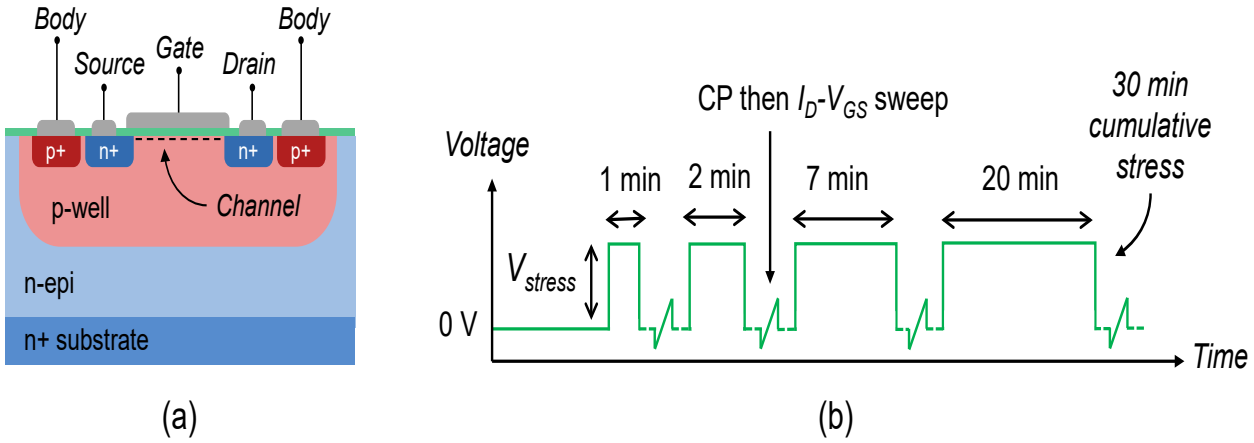

Fig. 1. (a) Schematic cross-section of the lateral test MOSFETs used in this work. (b) Diagram of the gate voltage sequence during the HVGS experiment.

~8 MV/cm) for a cumulative stress time of 30 minutes, which was interrupted periodically by a CP voltage level sweep with a pulse amplitude of 15 V followed by an I_D-V_{GS} sweep.

The field-effect mobility was calculated from the I_D-V_{GS} data by

$$\mu_{FE} = \frac{L}{W}\frac{1}{C_{ox}V_{DS}}\frac{dI_D}{dV_{GS}}, \quad (1)$$

where L and W are the MOSFET channel length and width, respectively, C_{ox} is the specific oxide capacitance, and V_{DS} is the drain-source voltage, which was 0.1 V during the measurements. Due to the high density of interface traps in SiC MOSFETs, the calculated μ_{FE} is not the real mobility of the free electrons in the channel, but is a fraction of the real mobility determined by the fraction of electrons in the channel that are not trapped. This parameter thus represents the combined effects of electron immobilization and Coulombic scattering caused by interface traps, which determine the channel resistance.

The peak CP current (I_{CP}) is related to the interface trap density according to

$$N_{CP} = I_{CP,max}/qfWL = \int_{E_{em,h}}^{E_{em,e}} D_{it}(E)dE, \quad (2)$$

where N_{CP} is the number of traps pumped per cycle, q is the elementary charge, f is the gate pulse frequency, D_{it} is the interface trap energy distribution, and $E_{em,h/e}$ are the lower/upper energy bound of the energy range of interface traps measured which is determined by the rise/fall time and amplitude of the gate pulse waveform [7]. N_{CP} is therefore a fraction of the total N_{it} which in our measurements includes interface traps within an energy range of about 2.9 eV across the middle of the bandgap.

Results and Discussion

Positive High-Voltage Gate Stress. The CP I-V curves during positive HVGS for a stress voltage of +36 V are shown in Fig. 2(a). The corresponding μ_{FE}-V_{GS} curves are shown in Fig. 2(b). The peak I_{CP} increases significantly with stress time, indicating that new interface traps are being generated during the stress. This is accompanied by a decrease in the peak μ_{FE}, which allows us to conclude that the generated interface traps include acceptor traps in the upper half of the bandgap which become negatively charged upon capturing electrons, reducing the free electron density in the channel and increasing the Coulombic scattering rate of the remaining free electrons. The CP curves also show a negative shift in the flatband voltage (V_{FB}) after the first stress interval which becomes nearly constant after the subsequent stress intervals. The same behavior is observed for V_T in the μ_{FE} curves as well.

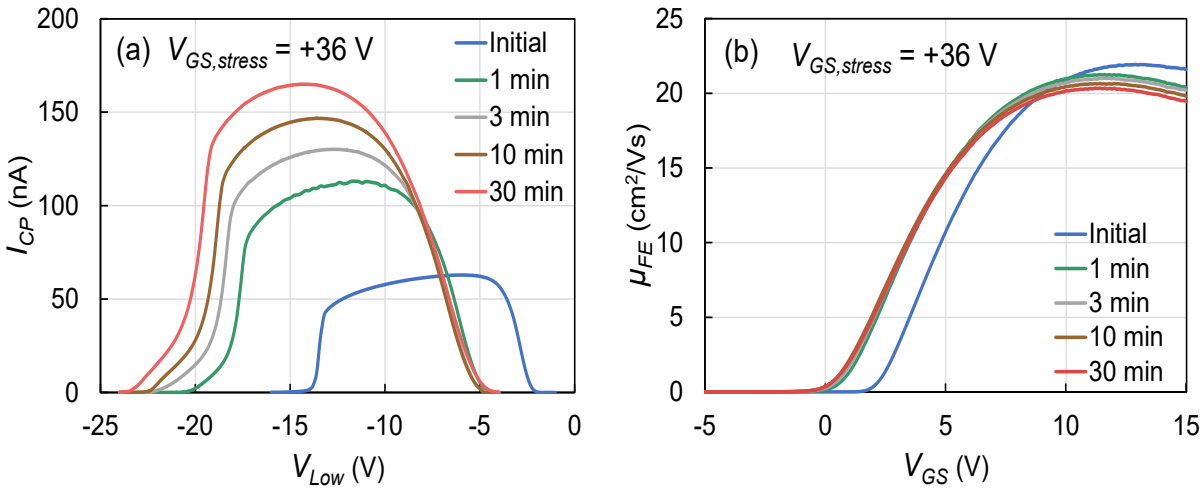

Fig. 2. (a) CP *I-V* curves taken after several time intervals during positive HVGS for a stress voltage of +36 V. (b) The corresponding field-effect mobility curves calculated from the I_D-V_{GS} sweeps.

This quickly saturating negative shift in V_{FB} and V_T is attributed to a rapid accumulation of positive charge in the bulk of the gate oxide as holes generated by impact ionization and/or anode hole injection become trapped in the SiO_2 [3]–[6]. The apparent V_T from the CP curves shows a continuous negative shift with additional stress time, in contrast to V_{FB} and the V_T from the μ_{FE} curves, which may result from an increase in donor interface traps [10]. The left side of the CP curves after stress also show an early rise in I_{CP} with a shallower initial slope, which can result from parallel recombination current [10], indicating the presence of nonuniform interface degradation during positive HVGS. The behavior of the CP curves after positive HVGS observed here are consistent with our previous observations [9].

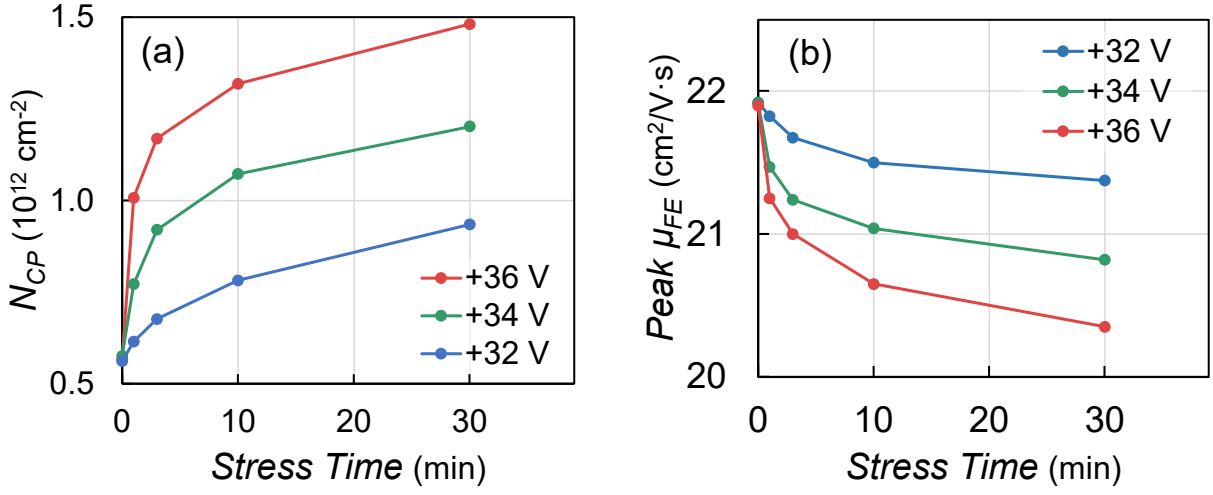

Fig. 3. (a) The measured N_{CP} versus stress time during positive HVGS for different stress voltages and (b) the corresponding peak μ_{FE}.

Fig. 3(a) and 3(b) show the measured N_{CP} and peak μ_{FE}, respectively, as a function of time during positive HVGS for three different gate stress voltages. The interface degradation measured by both parameters increases with both stress voltage and time. The time dependence obeys a power law with an exponent less than unity, similar to V_T shift during bias temperature instability (BTI) [11], [12].

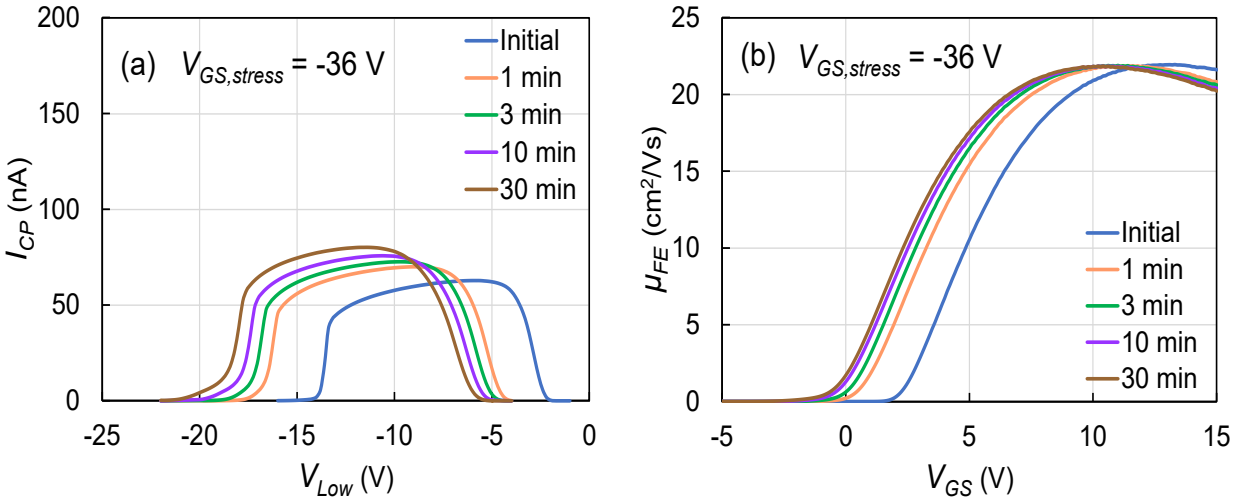

Fig. 4. (a) CP *I-V* curves taken after several time intervals during negative HVGS for a stress voltage of -36 V. (b) The corresponding field-effect mobility curves calculated from the I_D-V_{GS} sweeps.

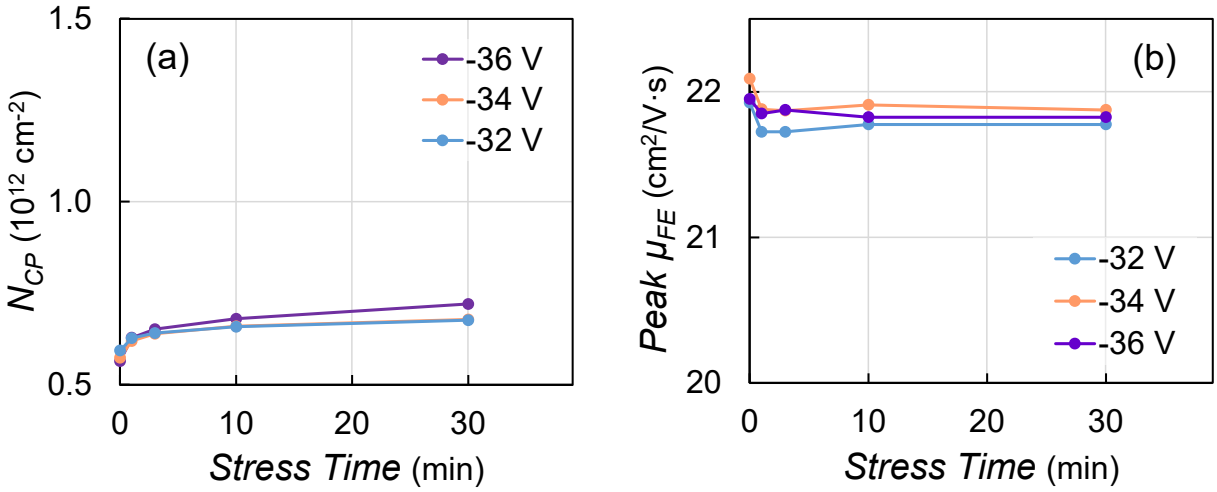

Fig. 5. (a) The measured N_{CP} versus stress time during negative HVGS for different stress voltages and (b) the corresponding peak μ_{FE}.

Negative High-Voltage Gate Stress. Fig. 4(a) and 4(b) show the CP and μ_{FE} characteristics, respectively, during negative HVGS for a stress voltage of -36 V. I_{CP} increases much less than during positive HVGS, and no μ_{FE} degradation is observed. Both V_{FB} and V_T exhibit a continuous negative shift with increasing stress time, which can be attributed to holes becoming captured by border traps as well as Fowler-Nordheim (F-N) injection and subsequent trapping in the SiO_2 bulk.

Fig. 5(a) and 5(b) show the measured N_{CP} and peak μ_{FE}, respectively, as a function of time during negative HVGS for three different gate stress voltages. N_{CP} again shows a sublinear time dependence, but it increases much less compared to positive HVGS, and μ_{FE} shows no degradation for any of the stress voltages apart from an initial decrease after the first stress interval.

To better visualize the stress voltage and time dependence of N_{CP}, the change in N_{CP} during positive and negative HVGS for each stress voltage are plotted versus stress time in logarithmic scale in Fig. 6. From these plots the time exponent of the power law can be readily extracted. During positive HVGS, the exponent decreases with higher stress voltage, in contrast to what would be expected for BTI effects. During negative HVGS, a voltage-independent time exponent of ~0.25 is obtained, which is close to what is commonly found for V_T shift during BTI for both SiC and silicon MOSFETs [11]–[13]. This observation suggests that normal BTI mechanisms may be operating during negative HVGS. The stress voltage dependence of ΔN_{CP} during negative HVGS can also be more clearly seen in the logarithmic scale of this plot.

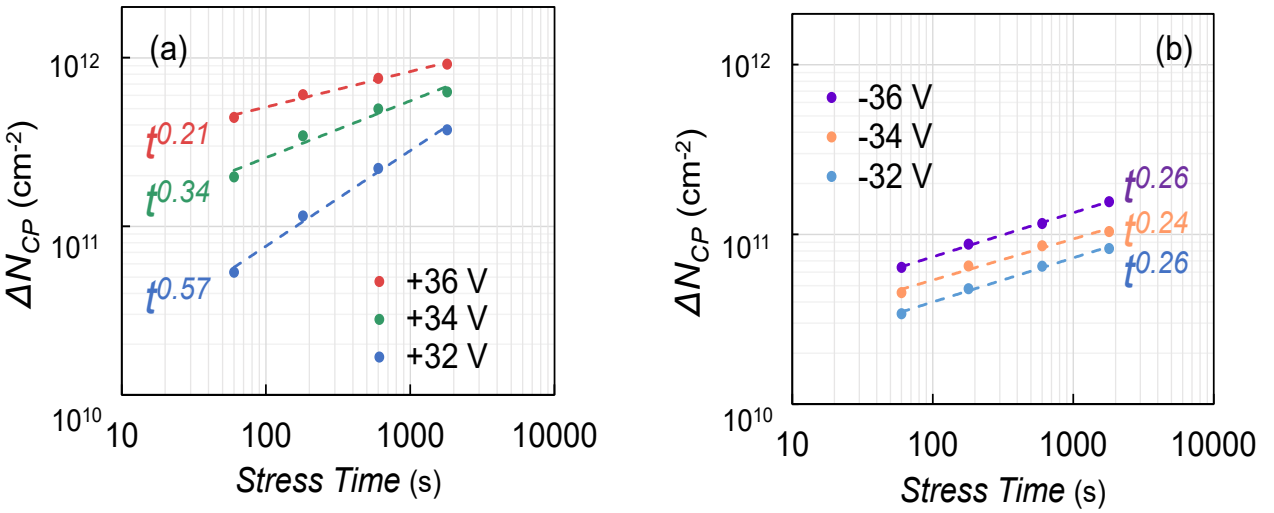

Fig. 6. The change in N_{CP} versus stress time in logarithmic scale for (a) positive HVGS and (b) negative HVGS. N_{CP} increases as a power law in time with the shown exponents.

Correlation of Trap Density and Mobility. In Fig. 3, N_{CP} and μ_{FE} appear to be inversely correlated, inversely following the same voltage and time dependence during positive stress. In Fig. 5, on the other hand, N_{CP} and μ_{FE} do not appear to be correlated during negative stress. It is of interest to evaluate the correlation of N_{CP} and μ_{FE} for each stress condition. This is shown in Fig. 7, where $\Delta\mu_{FE}$ is plotted versus ΔN_{CP} (normalized to the values before any stress) for each stress voltage for both positive and negative HVGS. For positive stress, $\Delta\mu_{FE}$ follows a universal linear dependence on ΔN_{CP}, irrespective of the stress voltage magnitude. The μ_{FE} degradation during positive HVGS therefore seems to be caused directly by increased Coulomb scattering and trapping of channel electrons at newly created interface defects.

In Fig. 7(b), the relatively small changes in both N_{CP} and μ_{FE} during negative HVGS make it difficult to conclude whether the same trend is followed as during positive HVGS. As can be seen in Fig. 7(c), when the scale is magnified $\Delta\mu_{FE}$ shows no decrease after the initial stress interval and thus exhibits no correlation with N_{CP}. This observation indicates that the generated interface traps during negative HVGS must be donor traps, which are neutral of charge when the channel is in inversion and thus have no effect on free electron density or mobility in the channel.

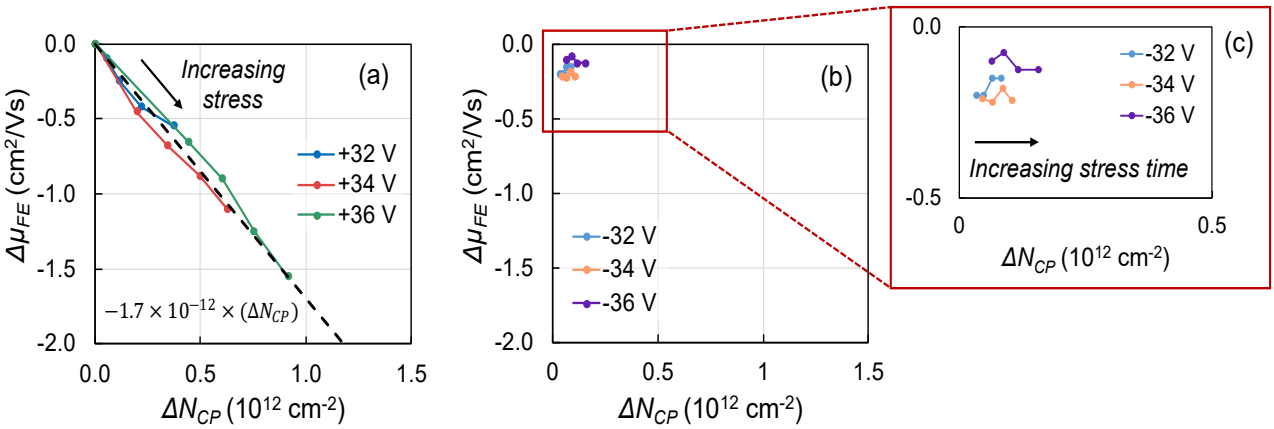

Fig. 7. The change in peak μ_{FE} plotted versus the change in N_{CP} for the different stress voltage magnitudes during (a) positive HVGS and (b) negative HVGS. The universal linear correlation for positive HVGS indicates that the μ_{FE} degradation is a direct result of interface trap generation. (c) A magnified view of the negative HVGS data showing the lack of correlation between $\Delta\mu_{FE}$ and ΔN_{CP}.

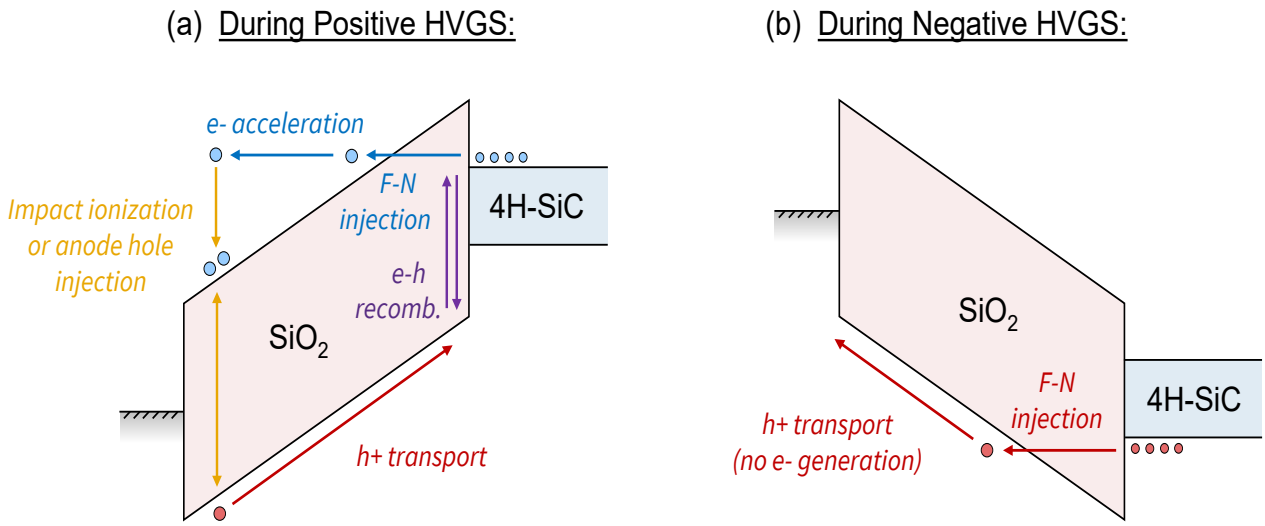

Fig. 8. Energy band diagram of the MOS structure and the various carrier transport and generation/recombination processes occuring during (a) positive HVGS and (b) negative HVGS.

Discussion of Possible Degradation Mechanisms. To understand the possible mechanisms for interface trap generation during HVGS that can be deduced from the above observations, it is helpful to review the physical processes electrons and holes undergo in the MOS structure during HVGS. These are illustrated in Fig. 8(a) for positive HVGS and 8(b) for negative HVGS.

During positive HVGS, (i) electrons are injected from the channel into the SiO_2 by F-N tunneling, (ii) the injected electrons are accelerated toward the gate electrode by the high oxide field, gaining kinetic energy, (iii) a small fraction of the accelerating electrons, which increases with oxide field, are able to reach an energy over 9 eV to cause impact ionization within the SiO_2 [5], generating electron-hole pairs, (iv) the generated holes transport back toward the SiC/SiO_2 interface, though some become trapped within the SiO_2, and (v) recombination may take place near the interface or in the channel between the generated holes and the injected or channel electrons. Therefore, processes happening near the interface which could be responsible for trap generation during positive HVGS include electron F-N injection, hole transport, and electron-hole recombination.

During negative HVGS, holes are injected into the SiO_2 by F-N tunneling, then accelerate toward the gate electrode. However, in SiO_2 hole transport is believed to be much more dispersive and possibly even proceed via a hopping mechanism [5], [6], [14], such that the holes cannot obtain significant kinetic energy to generate electrons by impact ionization or anode electron injection. Therefore, during negative HVGS, hole F-N injection is the only physical mechanism taking place near the interface and the only apparent candidate for interface trap generation, other than the high electric field itself and the presence of accumulated holes in the channel.

To further deduce the responsible mechanisms for trap generation, the dependence of the measured ΔN_{CP} on the calculated fluence of injected carriers due to F-N tunneling was evaluated. The F-N current is given by

$$I_{inj} = \frac{q^2 E_{ox}^2}{16\pi^2 \hbar \phi_B} \exp\left[-\frac{4\sqrt{2m^*(q\phi_B)^3}}{3q\hbar E_{ox}}\right], \tag{3}$$

where E_{ox} is the oxide electric field, $\hbar$ is the reduced Planck's constant, Φ_B is the injection barrier height for the carrier due to the SiC/SiO_2 band offsets (in volts), and m^* is the tunneling effective mass of the carrier. For the calculation, a Φ_B value of 2.75 V was used for electrons and 2.9 V for holes [13], and an m^* value of $0.42m_0$ was used for electrons and $0.58m_0$ for holes [15], where m_0 is the electron rest mass. The fluence was then calculated by

$$N_{inj} = I_{inj} \cdot t_{stress}/q. \quad (4)$$

It should be noted that the change in V_{FB} after each stress interval was also accounted for in the calculation of E_{ox}, though it did not significantly affect the qualitative features of the results.

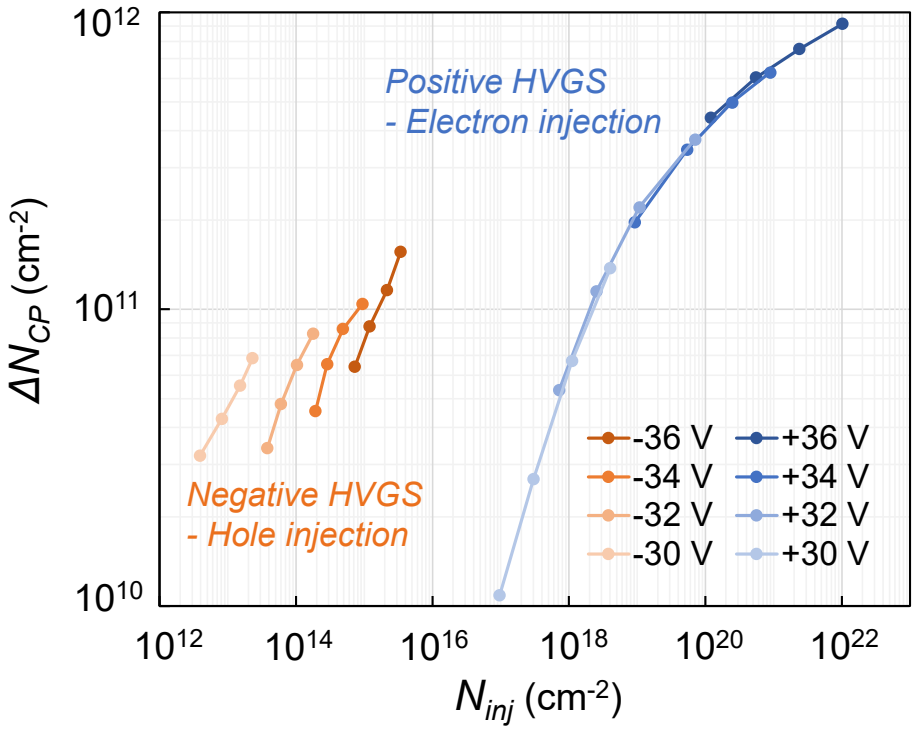

Fig. 9. The measured change in N_{CP} versus the calculated fluence of carriers injected by Fowler-Nordheim tunneling into the SiO_2 from the channel during positive or negative HVGS for several stress voltage magnitudes. The generated trap density follows a universal dependence on the injected fluence for positive HVGS, but not for negative HVGS.

Fig. 9 shows the measured ΔN_{CP} plotted versus the calculated fluence for positive and negative HVGS for several stress voltage magnitudes. The ΔN_{CP} during positive HVGS shows a universal dependence on the electron fluence, irrespective of the stress voltage used. The lack of a separate voltage dependence makes it unlikely for hot holes and electron-hole recombination to be the source of trap generation, since the density of holes arriving at the interface would depend not only on the number of injected electrons, but also on the avalanche multiplication rate (per injected electron), which would also depend on the gate voltage. Thus, the arriving hole density would not be directly proportional to N_{inj}. In addition, the recombination rate would be hole-limited because the hole density arriving at the interface must be lower than the injected electron density since only a small fraction of the electrons generate holes. The trap generation during positive HVGS therefore appears to be caused by the F-N electron injection itself.

In contrast, ΔN_{CP} during negative HVGS does not appear to follow a universal dependence on the hole fluence. In particular, the dependence of ΔN_{CP} on the stress voltage magnitude is too weak. It is also noteworthy that for a given fluence, the ΔN_{CP} is much higher for negative HVGS than for positive HVGS. The defect generation during negative HVGS is therefore likely field-induced, as that seems to be the only remaining candidate.

Summary

In summary, positive and negative HVGS was applied to lateral SiC test MOSFETs using several stress voltages and times, and the impact of each on N_{CP} and μ_{FE} was studied. Positive HVGS was found to cause significantly more interface trap generation than negative HVGS, which was linearly correlated with the degradation in μ_{FE}. No mobility degradation occurred during negative HVGS despite some increase in N_{CP}, indicating that the newly created traps were donors. When the change in N_{CP} is plotted versus the injected carrier fluence into the oxide via F-N tunneling, the generated trap density follows a universal dependence on the injected electron fluence during positive HVGS, irrespective of the stress voltage, but during negative HVGS the generated trap density did not follow a universal dependence on the injected hole fluence, indicating that other mechanisms are responsible for the trap creation. Lastly, CP was shown to be a valuable technique for characterizing interface trap density, as evidenced by the ability to directly correlate N_{CP} and μ_{FE} during positive HVGS.

References

[1] J. Berens and T. Aichinger, "A straightforward electrical method to determine screening capability of GOX extrinsics in arbitrary, commercially available SiC MOSFETs," in *2021 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, USA: IEEE, Mar. 2021, pp. 1–5. doi: 10.1109/IRPS46558.2021.9405152.

[2] A. K. Biswas *et al.*, "Hole-Induced Threshold Voltage Instability Under High Positive and Negative Gate Stress in SiC MOSFETs," in *2024 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2024, pp. 1–5. doi: 10.1109/IRPS48228.2024.10529422.

[3] F. Masin *et al.*, "Non-monotonic threshold voltage variation in 4H-SiC metal–oxide–semiconductor field-effect transistor: Investigation and modeling," *Journal of Applied Physics*, vol. 130, no. 14, p. 145702, Oct. 2021, doi: 10.1063/5.0057285.

[4] D. J. DiMaria, E. Cartier, and D. Arnold, "Impact ionization, trap creation, degradation, and breakdown in silicon dioxide films on silicon," *Journal of Applied Physics*, vol. 73, no. 7, Art. no. 7, Apr. 1993, doi: 10.1063/1.352936.

[5] D. Arnold, E. Cartier, and D. J. DiMaria, "Theory of high-field electron transport and impact ionization in silicon dioxide," *Phys. Rev. B*, vol. 49, no. 15, pp. 10278–10297, Apr. 1994, doi: 10.1103/PhysRevB.49.10278.

[6] D. J. DiMaria and J. W. Stasiak, "Trap creation in silicon dioxide produced by hot electrons," *Journal of Applied Physics*, vol. 65, no. 6, Art. no. 6, Mar. 1989, doi: 10.1063/1.342824.

[7] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Trans. Electron Devices*, vol. 31, no. 1, Art. no. 1, Jan. 1984, doi: 10.1109/T-ED.1984.21472.

[8] A. Salinaro *et al.*, "Charge Pumping Measurements on Differently Passivated Lateral 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 1, Art. no. 1, Jan. 2015, doi: 10.1109/TED.2014.2372874.

[9] S. R. Stein, J. Kim, S. Das, D. J. Lichtenwalner, and S. Ryu, "Characterization of Interface Trap Density in SiC MOSFETs Subjected to High Voltage Gate Stress," in *2024 IEEE International Reliability Physics Symposium (IRPS)*, Grapevine, TX, USA: IEEE, Apr. 2024, pp. 1–5. doi: 10.1109/IRPS48228.2024.10529394.

[10] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, "Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation," *IEEE Trans. Electron Devices*, vol. 36, no. 7, Art. no. 7, Jul. 1989, doi: 10.1109/16.30938.

[11] D.K. Schroder, “Negative bias temperature instability: What do we understand?,” *Microelectronics Reliability*, vol. 47, no. 6, Art. no. 6, Jun. 2007, doi: 10.1016/j.microrel. 2006.10.006.

[12] J. H. Stathis, “The physics of NBTI: What do we really know?,” in *2018 IEEE International Reliability Physics Symposium (IRPS)*, Burlingame, CA: IEEE, Mar. 2018, p. 2A.1-1-2A.1-4. doi: 10.1109/IRPS.2018.8353539.

[13] D. J. Lichtenwalner *et al.*, “Reliability studies of SiC vertical power MOSFETs,” in *2018 IEEE International Reliability Physics Symposium (IRPS)*, Burlingame, CA: IEEE, Mar. 2018, p. 2B.2-1-2B.2-6. doi: 10.1109/IRPS.2018.8353544.

[14] R. C. Hughes, “Time-resolved hole transport in a-SiO2,” *Phys. Rev. B*, vol. 15, no. 4, pp. 2012–2020, Feb. 1977, doi: 10.1103/PhysRevB.15.2012.

[15] R. K. Chanana, “Determination of hole effective mass in SiO2 and SiC conduction band offset using Fowler–Nordheim tunneling characteristics across metal-oxide-semiconductor structures after applying oxide field corrections,” *Journal of Applied Physics*, vol. 109, no. 10, p. 104508, May 2011, doi: 10.1063/1.3587185.