Key Engineering Materials
ISSN: 1662-9795, Vol. 1021, pp 35-39
doi:10.4028/p-4QkAFT

Submitted: 2024-09-20
Revised: 2025-08-07
Accepted: 2025-08-08
Online: 2025-09-05

Impact of Single-Step Deep P-Body Implant on 1.2 kV 4H-SiC MOSFET

Pavan Vudumula[1,a], Yu-Chieh Chien[1,b], Abdul Hannan Yeo[1,c*], Lakshmi Kanta Bera[1,d], Umesh Chand[1,e], Voo Qin Gui Roth[1,f], Surasit Chung[1,g], Navab Singh[1,h], Yee-Chia Yeo[1,i]

[1]Institute of Microelectronics (IME), Agency for Science, Technology, and Research (A*STAR), Singapore 138634.

*E-mail: [a]Vudumula_pavan_kumar@a-star.edu.sg, [b]Chien_Yu_Chieh@a-star.edu.sg, [c]hannan_yeo@a-star.edu.sg, [d]Lakshmi_kanta_bera@a-star.edu.sg, [e]Chand_Umesh@a-star.edu.sg, [f]Roth_Voo@a-star.edu.sg, [g]Surasit_chung@a-star.edu.sg, [h]navab@a-star.edu.sg, [i]Yeo_Yee_Chia@a-star.edu.sg,

Keywords: Channeling implant, Deep p-body, Single step implant

Abstract: In this work, TCAD simulation of SiC MOSFETs design with deep (2 μm) p-base using single step aluminum channeling implant along [0001] direction and JFET design using phosphorus implant is presented. The threshold voltage (V_{th}) was around 3 V for both the devices. Improvements to the specific on-resistance ($R_{on,sp}$) reduction by ~ 30 %, breakdown voltage (BV) enhancement by ~ 40 %, miller plateau (Q_{GD}) reduction by ~ 30% is reported. Furthermore, both the Baliga figure-of-merit (BFOM) ($BV^2/R_{on,sp}$) and high-frequency figure-of-merit (HFOM) ($R_{on,sp} \times Q_{GD}$) with 2 μm deep p-base /JFET implant are enhanced as compared to shallow 0.7 μm p-base/JFET implant. This paper provides valuable insights into the advantages of a single-step channeling implant at room temperature, without the need for a hard mask. This approach offers a high throughput with a low-cost process for fabricating high-performance SiC MOSFETs.

Introduction

4H-SiC MOSFETs are well-suited for hybrid electric vehicles (HEV) and pure electric vehicles (EV) with a voltage rating of 1.2 kV. This is attributed to their impressive BV, low $R_{on,sp}$, and fast switching speeds [1]. These devices consist of box-shaped implantation profiles formed through multi-step processes, including the p-base, JFET, n^+ and p^+ regions. Aluminum is used for both the p-base and p^+ implantation, while phosphorus is used for the JFET and n^+ implantation [2]. The multi-step implantation for box profiles is commonly conducted utilizing SiO_2 hard masks at high temperatures (> 400 °C). Undoubtedly, this process entails several steps that inherently impede manufacturing throughput. Few studies have investigated the impact of deep p-body and deep JFET on $R_{on,sp}$, BV and short circuit withstand time [3,4]. A recent study has shown that a well-defined box-type profile can be achieved through a single-step implantation with significant depth along the [0001] and [11$\bar{2}$3] crystal orientations [5]. However, the box shape profile is more effective in the [0001] direction. The channeling implantation process performed at room temperature, allows the use of photoresists which eliminates the need for hard mask processes. This helps to streamline fabrication by eliminating several steps involved in hard mask patterning which could lead to significant cost reductions. This channeling implant has potential applications in SiC super junction devices too. However, there are little reports on the characteristics of deep p-body standard SiC MOSFETs using single-step implant. This study investigates the impact of a deep p-body using a single-step implant profile along [0001] and the corresponding JFET implant design using phosphorous channeling implant along [0001] in 1.2 kV MOSFETs in terms of its static and dynamic characteristics.

Results and Discussion

Experimental data on aluminum channeled implantation with an energy of 300 keV and a dose of 1.2×10^{13} cm^{-2} along the [0001] crystal direction show a nearly box-shaped profile up to a depth of 2 µm [4]. This profile has been used for the p-body. To achieve a uniform JFET design, phosphorus implantation with optimized parameters (energy: 300/500/700 keV, dose: $3\times10^{12}/3\times10^{12}/1.2\times10^{13}$ cm^{-2}) is necessary. The implant profile is illustrated in Fig. 1.

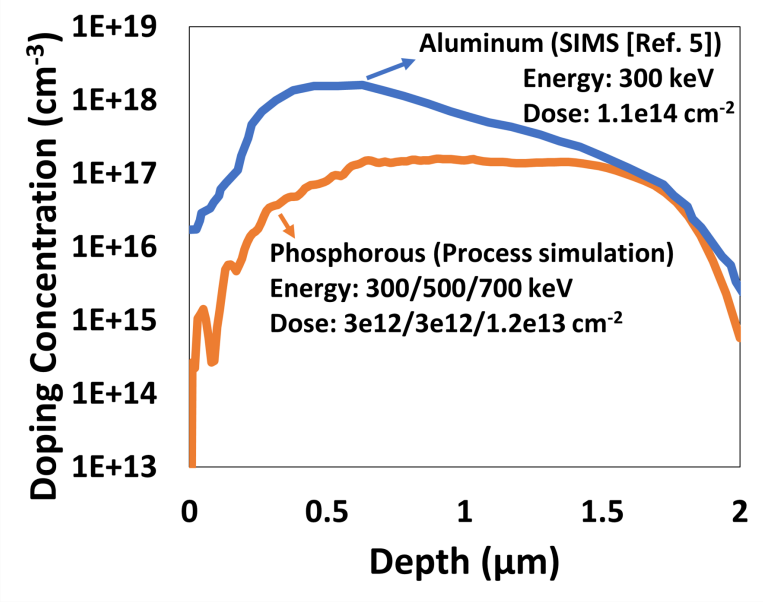

Fig. 1 Simulated doping profile for deep (2.0 µm) channeling implantation along [0001] orientation with optimized JFET profile.

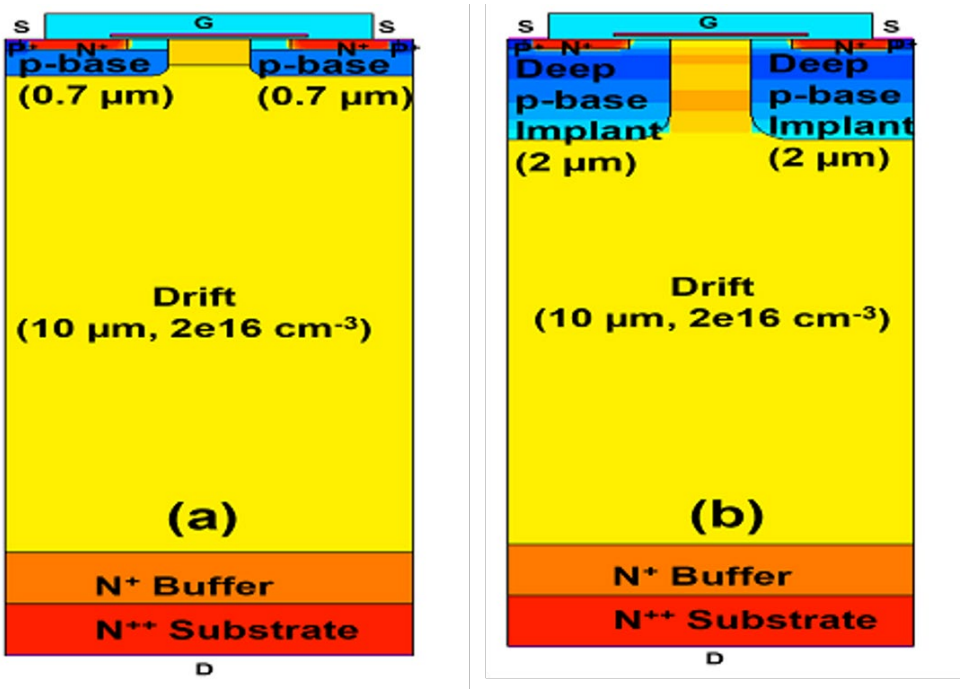

Fig. 2 Schematic of (a) non-channeled 0.7 µm p-base and (b) channeled single-step implanted 2 µm p-base from TCAD simulation.

The device cross-section of a 1.2 kV MOSFET with a non-channeled implant for a p-body depth of 0.7 µm and a p-body depth of 2 µm using channeling implant is depicted in Fig. 2 (a) and (b), respectively. These devices are simulated using TCAD with W_{JFET} = 1 µm, L_{ch} = 0.5 µm, L_{drift} =

10 µm, and a uniform epitaxy doping profile of 2 x 10^{16} cm^{-3}. The extracted threshold voltage (V_{th}) is approximately 3 V for both devices, and specific on-resistance ($R_{on,sp}$) from I_d-V_d characteristics (Fig. 3 (a)) is 30% lower with a JFET implant depth of 2 µm compared to a shallow JFET implant depth of 0.7 µm. This reduction is due to 2 µm charge sustaining layer (CSL) with deep JFET implant, resulting in increased electron flow and thus a lower $R_{on,sp}$. Fig. 3 (b) demonstrates a 40% improvement in blocking voltage for the p-body device with a depth of 2 µm compared to the device with a depth of 0.7 µm. Enhanced two-dimensional electric field distribution with deeper p-body compared to shallow p-base allows the device to sustain higher blocking voltages. Deep p-base better shields the channel and gate oxide from high drain bias due to the depletion in JFET.

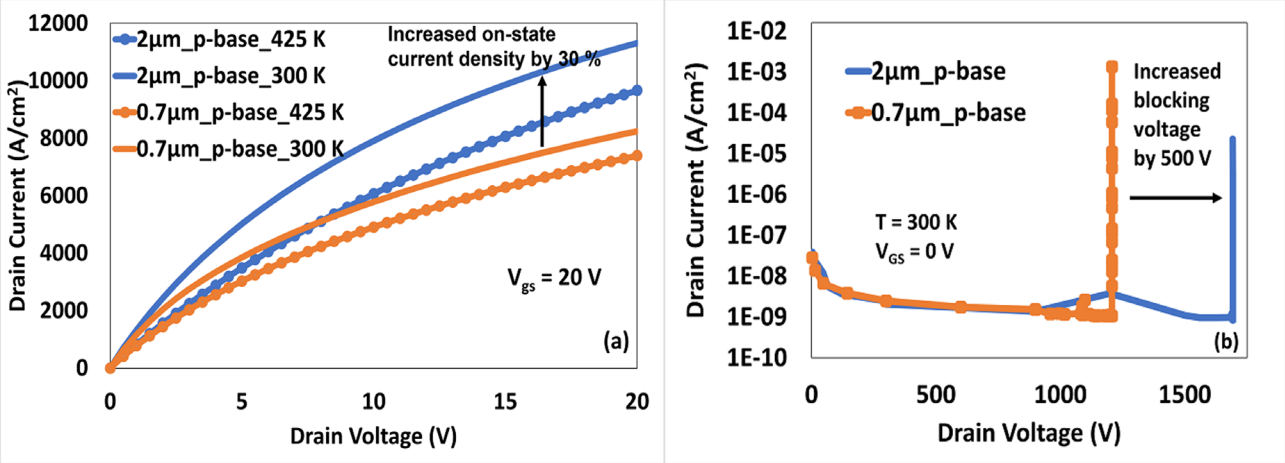

Fig. 3 Simulated (a) output and (b) blocking voltage characteristics for SiC MOSFETs with non-channeling (orange) and channeling (blue) implantation.

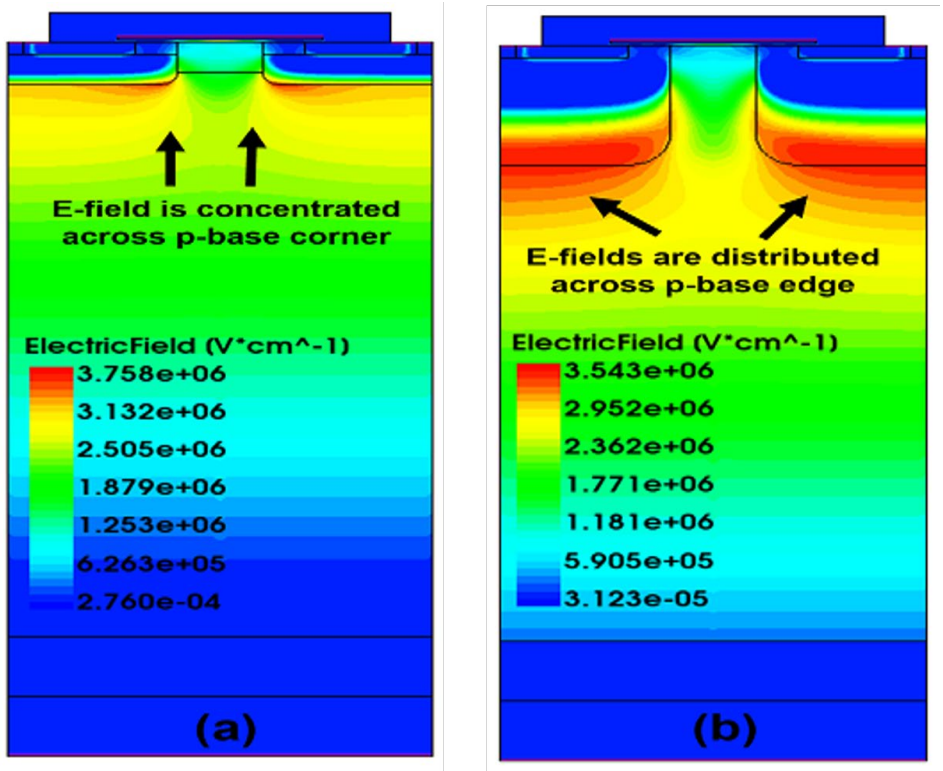

Fig. 4 Blocking-state electric field distribution near breakdown for (a) non-channeling 0.7 µm and (b) channeling 2.0 µm p-base region in SiC MOSFETs.

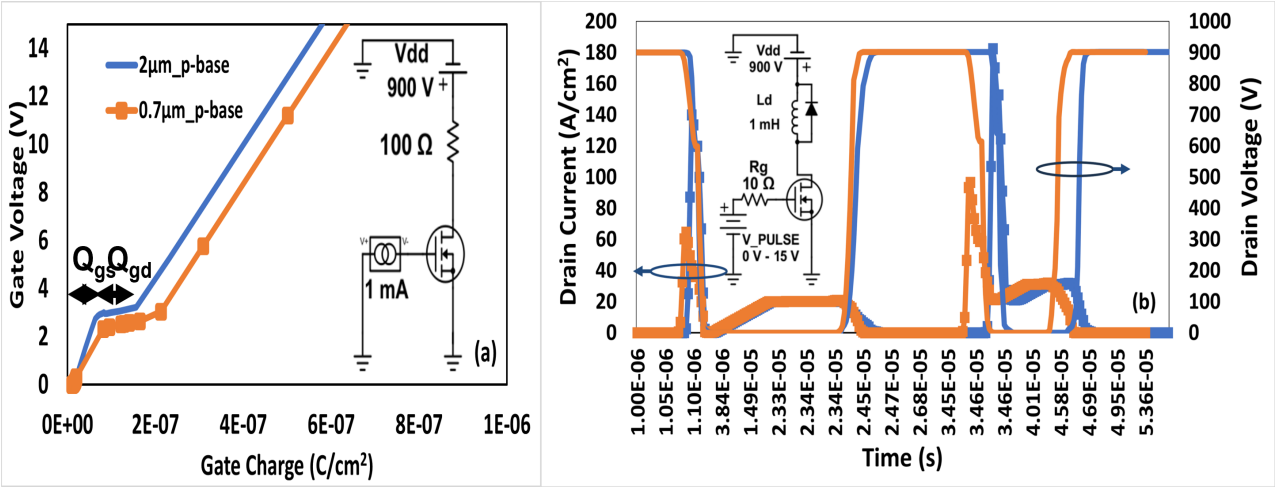

Fig. 5 Simulated (a) gate charge and (b) switching characteristics with non-channeling 0.7 µm and channeling 2.0 µm p-base region in SiC MOSFETs.

The off-state electric field distributions near the breakdown regime for 0.7 µm and for 2 µm p-base are shown in Fig. 4 (a) and 4 (b). Additionally, gate charge (Fig. 5(a)) and clamped inductive load switching simulations (Fig. 5 (b)) are performed using a mixed-mode SPICE environment to analyze the miller plateau (Q_{gd}) and switching losses. The non-linear capacitance simulations with variations in drain bias, including input (C_{iss}), output (C_{oss}), and reverse transfer (C_{gd}/C_{rss}) capacitances are shown in Fig. 6. An 80% improvement in C_{rss} corresponds to the reduced gate-to-drain coupling with the deep p-base design, which induces an increased depletion width along the JFET region during the switching regime. C_{iss} and C_{oss} remain the same for both devices as the remaining regions remain unaltered with a 5 µm cell pitch. Table 1 lists the performance metrics (BFOM, HF-FOM) and switching losses for both devices along with benchmarking results.

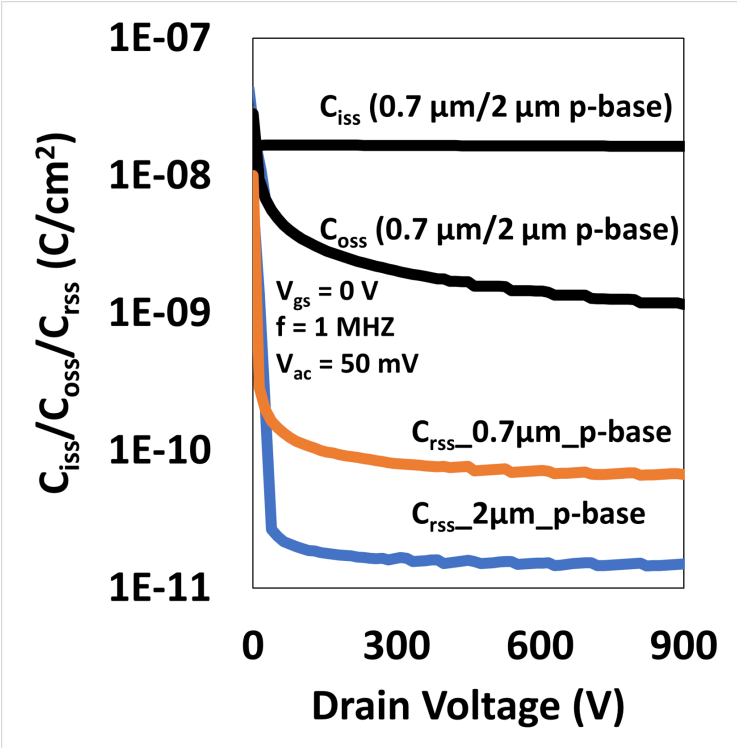

Fig. 6 Simulated non-linear input, output, and miller capacitances with drain bias with non-channeling 0.7 µm and channeling 2.0 µm p-base region in SiC MOSFETs.

Table 1 Simulated electrical performance metrics (BFOM and HF-FOM) at 27 ºC and 150 ºC.

0.7 μm p-base 1.2 kV 4H-SiC MOSFET				**2.0 μm p-base 1.7 kV 4H-SiC MOSFET**				**Benchmark [Ref. 3]**
T **(ºC)**	BV (V)	$R_{on,sp}$ (mΩ-cm^2)	BFOM (MV/cm^2)	***T*** **(ºC)**	BV (V)	$R_{on,sp}$ (mΩ-cm^2)	BFOM (MV/cm^2)	Design parameters: W_{JFET} = 0.9 μm L_{ch} = 0.5 μm L_{drift} = 10 μm N_{drift} = 8×10^{15} cm^{-3}
27	1208	2.4	608	**27**	1693	1.7	1686	
150	1220	2.7	551	**150**	1700	2.0	1445	
	Q_{gd} (nC/cm^2)	$R_{on,sp}$ (mΩ-cm^2)	HF-FOM (nC-mΩ)		Q_{gd} (nC/cm^2)	$R_{on,sp}$ (mΩ-cm^2)	HF-FOM (nC-mΩ)	
27	117	2.4	281	**27**	82	1.7	140	
150	117	2.7	433	**150**	82	2.0	164	Electrical parameters: $R_{on,sp}$ = 4 mΩ-cm^2 BV = 1560 V
	E_{on} (mJ)	E_{off} (mJ)			E_{on} (mJ)	E_{off} (mJ)		
27	2.1	0.8		**27**	1.7	0.8		

Conclusion

In this study, we showed that the single-step channeling implantation is a highly promising method for realizing high BFOM and low HF-FOM in 4H-SiC MOSFETs. In addition, the implementation of channeling implantation ensured a superior process throughput at a much lower cost than the standard multi-step implant process.

Acknowledgement

This work was supported by the Science and Engineering Research Council of A*STAR (Agency for Science, Technology and Research) Singapore, under Grant No. A20H9A0242.

References

[1] B. J. Baliga, Silicon Carbide Power Devices, World scientific (2006).

[2] T. Kimoto and J. A. Cooper, Fundamentals of Silicon Carbide Technology, John Wiley & Sons (2014).

[3] D. Kim, N. Yun, A. J. Morgan, and W. Sung, “The effect of deep JFET and P-Well Implant of 1.2kV 4H-SiC MOSFETs,” IEEE J. Electron Devices Soc., vol. 10, 989-99 (2022).

[4] D. Kim and W. Sung, “Improved short-circuit ruggedness for 1.2kV 4H-SiC MOSFET using a deep p-well implemented by channeling implantation,” IEEE Electron Device Letters, vol. 42, no. 12, 1822-1825 (2021).

[5] M. K. Linnarsson, L. Vines, and A. Hallén, “Influence from the electronic shell structure on the range distribution during channeling of 40-300 keV ions in 4H-SiC,” J. Appl. Phys., 130, 075701 (2021).