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Temperature Dependence of 1200V-10A SiC Power Diodes: Impact of Design and Substrate on Electrical Performance

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Abstract. In this work, we investigate the static electrical parameters of 1200 V 4H-SiC power diodes with various designs and architectures (Schottky, PiN, and JBS with hexagonal or stripes anode), fabricated on two types of 150 mm substrates (single crystal 4H-SiC reference and 3C-poly silicon carbide based substrates: SmartSiC^{TM}). I(V) measurements are carried out in both reverse and forward modes to assess the impact of designs and substrates. Non-destructive avalanche mode is reached with similar performance (leakage, V_{AV}) observed for both substrates (due to identical drift layers and device structures). All diode designs on SmartSiC^{TM} exhibit a larger current conduction and less resistance in the ohmic regime (compared to bulk), whatever the temperature (up to 200°C). Partitioning model is also proposed for evaluating the substrate contribution on the measured specific resistance and on the observed SmartSiC gains.

Introduction

Bulk 4H-SiC substrates growth requires a long, energy-intensive and costly process, which limits the availability of SiC substrates for devices production today. Consequently, 3C-poly silicon carbide based substrates (pSiC) are currently being considered as an alternative substrate for SiC power devices fabrication. By utilizing the SmartCut^{TM} technology, a high-quality 4H-SiC layer can be bonded (conductive bonding) on top of a thick (350µm) polycrystalline SiC handle wafer [1]. The resulting SmartSiC^{TM} substrates are engineered to achieve better device yield and to optimise conduction losses [2] because of the low resistivity poly-SiC layer, thanks to one order of magnitude lower resistivity values compared to mono-SiC. SmartSiC™ not only enhances electrical performance but also reduces manufacturing costs and environmental impact. It enables the reuse of donor wafers, yielding around 500 wafers per SiC boule, ten times more than standard methods [3]. In this work, we study the impact of temperature on the static electrical parameters of 1200 V power 4H-SiC diodes with various designs and architectures (Schottky, PiN, JBS with hexagonal cells or stripes) fabricated on 150 mm bulk 4H-SiC and 3C-pSiC based substrates (SmartSiC^{TM}).

Devices Fabrication

Three power diodes architectures (Schottky, PiN, and JBS: Fig. 1a-b) have been fabricated through a process flow designed for 1200 V blocking voltage capability [4], with Al implanted p+ guard rings and a junction termination extension (JTE) annealed at 1700 ºC to achieve the breakdown voltage target (Fig. 1c). Various anode and edge terminations have been designed and fabricated on both 4H-SiC bulk and SmartSiC™ substrates (Fig. 1d). The substrates have not been thinned and backside contact formation was performed using laser annealing [5].
I(V) measurements, conducted in both reverse and forward modes, are aimed at evaluating the impact of different designs and substrates.

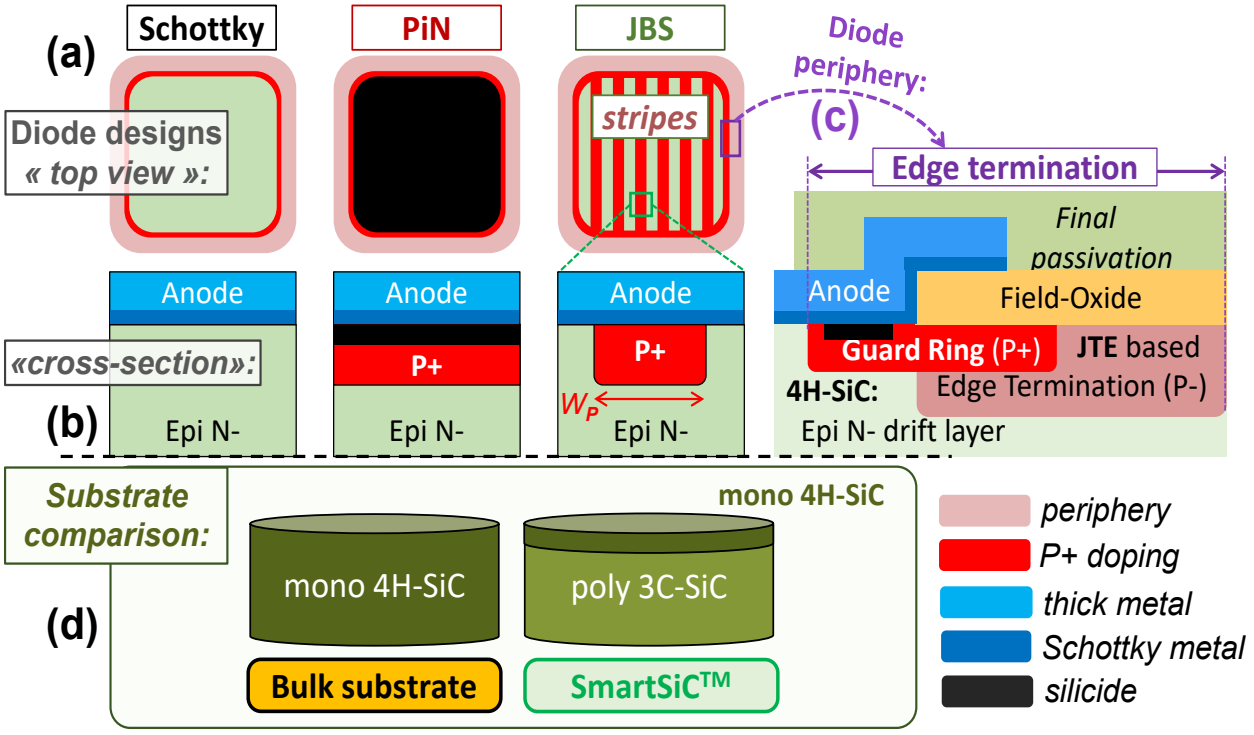

Fig. 1. Description of the tested diodes samples (device designs: Schottky, PiN, and JBS). **a**) Top view, **b**) anode cross-section with **c**) edge termination cross-section at the diode periphery, **d**) Additionally, standard 4H-SiC bulk and new SmartSiC™ substrates have been considered for building the diodes samples on these two types of epiwafers (with identical epi process, designed for 1200 V rating).

Electrical Characteristics: Off-State

Off-state characteristics, shown in Fig. 2a, highlight various reference diode types that are reverse biased on single crystal 4H-SiC (bulk) and SmartSiC™ epiwafers. Diodes on both epiwafers achieved non-destructive avalanche mode with similar leakage currents and avalanche voltages (V_{AV}), attributed to the identical drift layers and device structures.

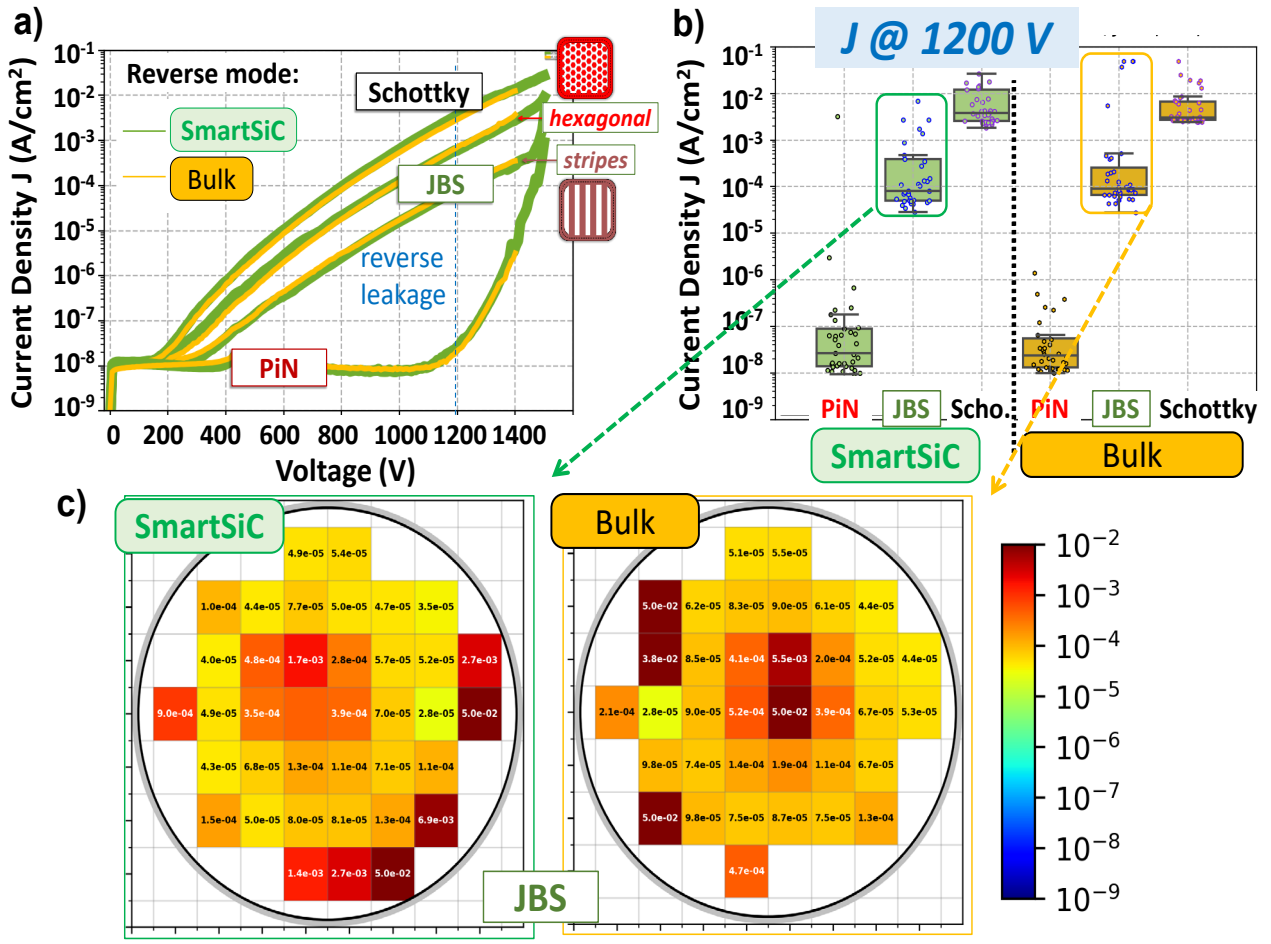

Fig. 2. **a**) Reverse I(V) curves (wafer median for bulk and SmartSiC™) for Schottky, JBS (hexagonal and stripes) and PiN. Anode surface is 2.01mm². **b**) Corresponding box plots of reverse leakage current densities J extracted at 1200V (for PiN, JBS with stripes, and Schottky diodes on SmartSiC™ and bulk), **c)** examples of wafermaps for J @ 1200V.

In Fig. 2b, the leakage current density is extracted at 1200 V (before avalanche). We observe similar leakage current distributions for both substrates (for PiN, JBS and Schottky diodes). Fig. 2c shows the wafer mapping of this leakage current level extracted for JBS (with stripes) on both bulk and SmartSiC™ substrates. Both substrate types reveal similar leakage current profile, with an increased leakage for a limited number of sites situated around the center and edges of the wafer, due to the presence of defects in these areas. It is also worth noting that the levels of reverse leakage current around the centre are slightly reduced for SmartSiC™ substrates. Wafer mapping and yield analysis indicated that defects contributing to off-state performance degradation, such as BPDs or TEDs, were minimally influenced by the substrate material [6].

Electrical Characteristics: On-State

Following the off-state study, forward mode measurements are carried out. I(V) characteristics of SmartSiC™ and bulk devices are compared. JBS diodes on SmartSiC™ exhibited superior current conduction and reduced resistance in the ohmic regime (Fig. 3a), demonstrating the impact of substrate resistivity. The specific differential resistance (R_{DIF}) was extracted as illustrated in Fig. 3a. In Fig. 3b, R_{DIF} decreases as the Schottky surface ratio increased for both bulk and SmartSiC™, with a notable reduction in resistance observed in hexagonal configurations. All diodes fabricated on SmartSiC™ exhibited less resistance than their bulk counterparts.

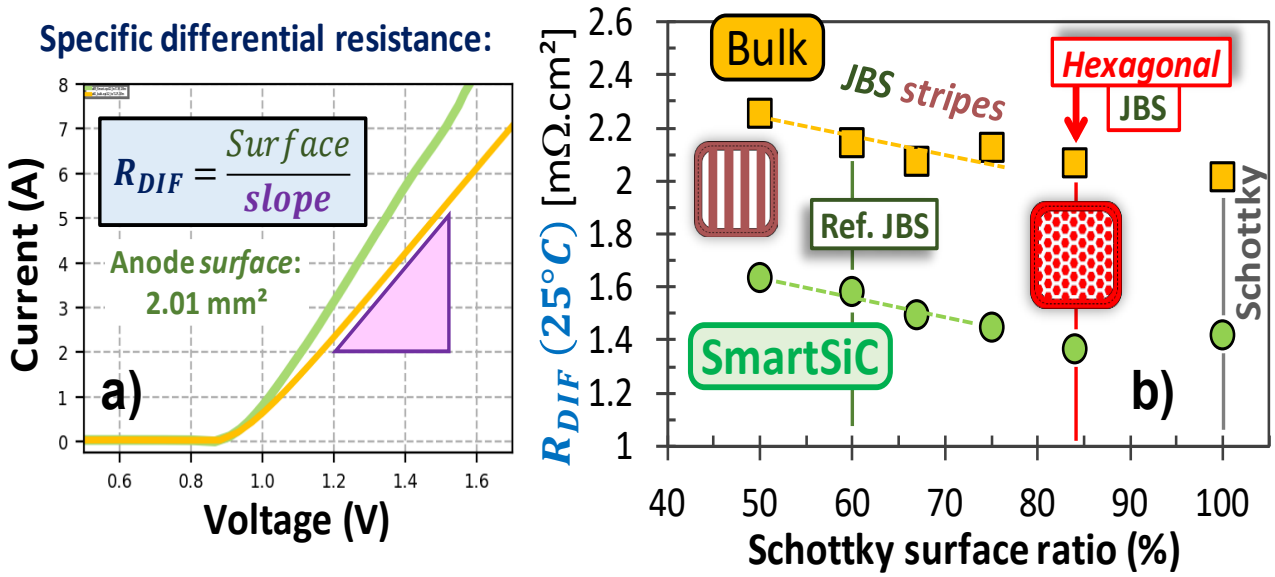

Fig. 3. **a)** Example of JBS diodes I(V) measurements for bulk and SmartSiC (with specific differential resistance R_{DIF} definition). **b)** Extracted R_{DIF} for different JBS diode designs (+Schottky) as function of the Schottky surface ratio.

Fig. 4 shows the JBS R_{ON}-BV figure of merit for the studied JBS samples with a comparison to state-of-the-art diodes [7]. For breakdown voltage (BV) ratings between 1400 and 1600 V, we observe that the specific on-resistance (similarly extracted as R_{DIF}) is reduced and is closer to the theoretical limit of 4H-SiC for the SmartSiC™ JBS compared to the bulk reference and also to state-of-the-art JBS devices (including commercial devices with thinned substrates) [7].

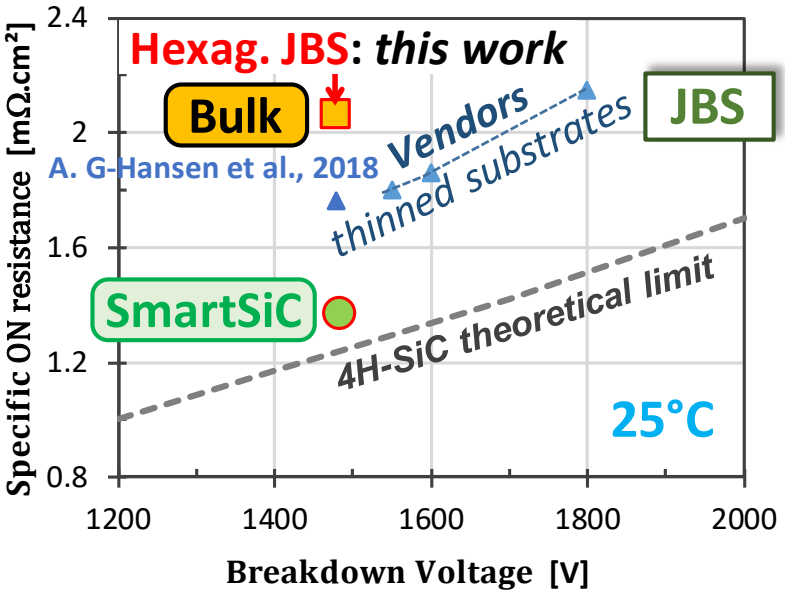

Fig. 4. JBS specific ON resistance versus breakdown voltage (for the investigated bulk and SmartSiC™ hexagonal JBS diodes, compared to state-of-the-art JBS diodes, including commercial products) [7].

On-state resistance behaviour with temperature

The forward characteristics were further studied as a function of temperature. The observed conduction gain for the SmartSiC™ samples (compared to bulk) was investigated from 25°C to 200°C in Fig. 5 and Fig. 6.

Fig. 5 shows $R_{DIF}(T)$ measurements for JBS diodes (with stripes) on bulk and SmartSiC™ epiwafers, with an observed exponential behaviour. The absolute R_{DIF} difference between bulk and SmartSiC™ is 0.7 mΩ.cm² (respectively 1.5 mΩ.cm²) at 25 °C (resp. 200 °C).

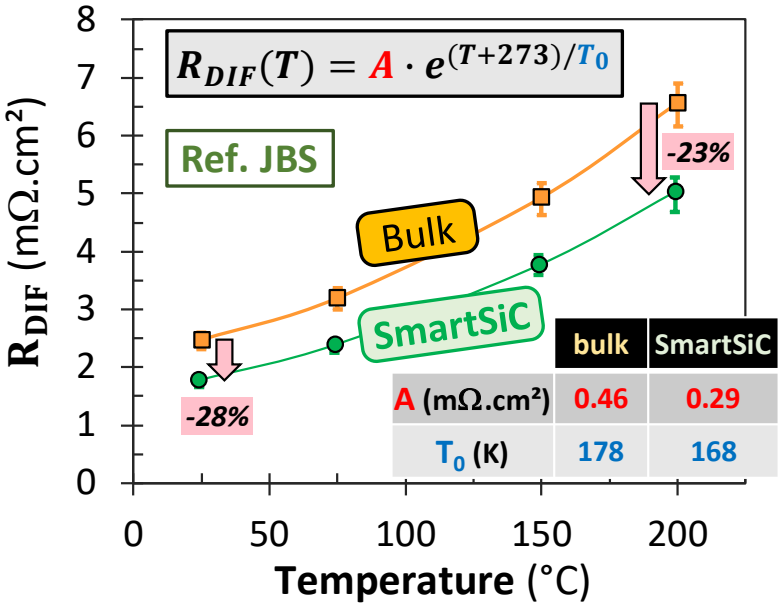

Fig. 5. Impact of temperature (25-200°C) on measured specific differential resistance (R_{DIF}) for JBS diode (reference design with stripes). For both samples, the data can be fitted using an exponential model (as observed for results in [8], cf. Fig. 7).

In order to check if this R_{DIF} advantage offered by SmartSiC exist also for the other diodes types, we perform similar comparison for the following designs:

- JBS with stripes: three designs with various Schottky ratios
- JBS with hexagonal cells
- Reference Schottky diode

The following figures show extracted R_{DIF} versus temperature for these five different diode designs on SmartSiC™ epiwafer (Fig. 6a) and on bulk epiwafer (Fig. 6b): again, an increasing trend with temperature can be observed for all samples. Besides a minor dispersion between the designs is also highlighted (<1 mΩ.cm²). In Fig. 6c, the differential resistance gain, ΔR_{DIF}, between the two epiwafers is calculated and plotted against temperature. The gain offered by SmartSiC™ epiwafer compared to bulk counterpart is found to be independent on the diode design: ~0.7 mΩ.cm² (respectively ~1.4 mΩ.cm²) at 25 °C (resp. 200 °C).

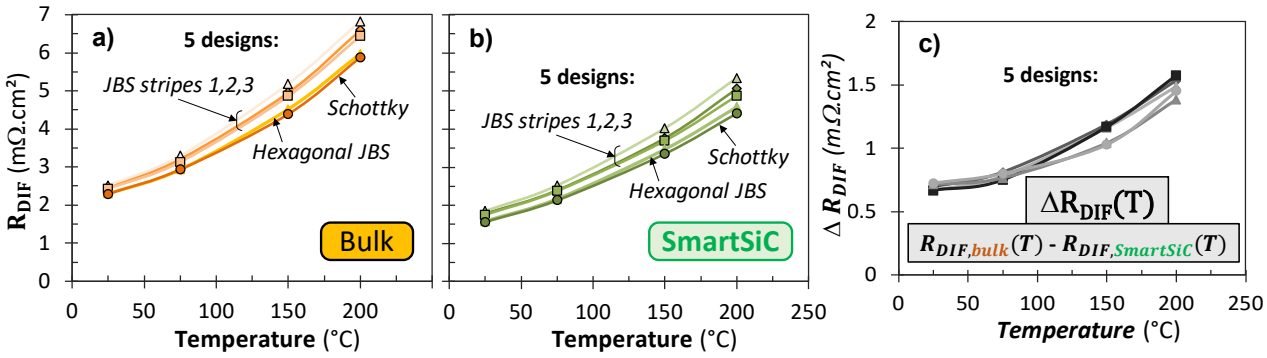

Fig. 6. **a-b**) Comparison of $R_{DIF}(T)$ for different diodes (JBS with three stripes designs; hexagonal cells JBS, and Schottky) for bulk and SmartSiC epiwafers, **c**) and corresponding differential resistance gain (bulk-SmartSiC) versus temperature showing identical trend for all diode designs.

Fig. 7 reveals that all device designs, regardless of epi or substrate (including additional 1700 V epiwafer with the same diode process [4], and literature reference [8]), follow the same predictive behaviour: R_{DIF} values at 25 °C exactly reflect R_{DIF} at 200°C. This indicates that the $R_{DIF}(T)$ model from Fig. 5 can be applied to all these various device/substrate/epi configurations (with very similar T_0 parameter).

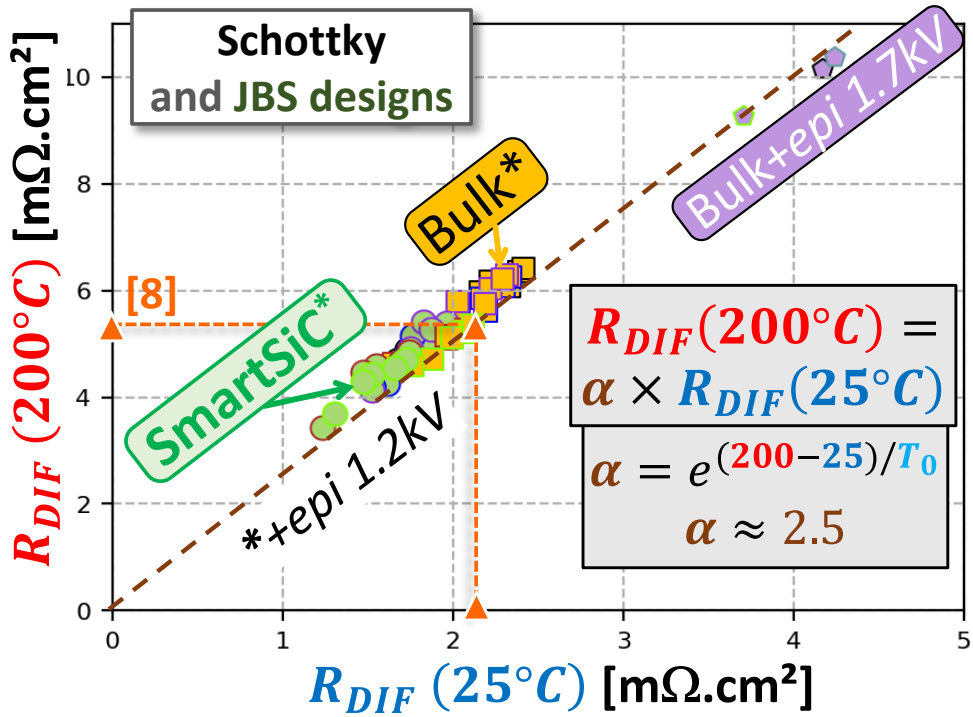

Fig. 7. Measured differential resistance at 200 °C versus 25 °C for various JBS designs (+Schottky) on different sites (for two wafers with same 1200 V epi, +1700 V bulk epiwafer). Ref [8] bulk data are in agreement with the observed trend.

Discussion

The focus on this paper is to highlight on-resistance difference in the forward operation mode of unipolar 1200 V diodes fabricated on bulk and SmartSiC™ epiwafers. For the off-state characteristics depicted in Fig. 2, the findings suggest that for the same diode device and epi designs on bulk and SmartSiC™, the off-state performance ought to be similar in terms of reverse leakage current levels and non-destructive avalanche breakdown. This also suggests that SmartSiC™ in the reverse mode

behaves similarly to bulk wafers, which also implies that the engineered substrate does not exhibit additional defects.

In the on-state, differential resistance (R_{DIF}) has been comprehensively studied between Schottky and several JBS diode designs. The overall forward conduction current in Fig. 3 illustrates the advantage of using SmartSiC™ to reduce conduction losses with a less resistive handle substrate as reported in [9]. This confirms the influence of substrate resistivity on the on-state performance of power devices. The exponential temperature dependence of R_{DIF} demonstrated in Fig. 5 to 7, coupled with the increased absolute R_{DIF} difference at 200°C further highlight the SmartSiC™ substrate's stability at high-temperature, which is reported here for the first time.

Further calculations are performed to anticipate and compare the performance of SmartSiC™ against thinned bulk epiwafers. This requires a decomposition of the different resistance contributions of the diode. Fig. 8 presents the differential resistance partitioning model used, cf. Eq. 1. To avoid additional calculation terms that may emerge from the current spreading in JBS devices, Schottky diodes is preferred here. The three main contributors to the total differential resistance are the epilayer (drift + buffer), substrate, and contacts (anode and cathode) resistances. The resistivity of each layer (Eq. 2, Eq. 3, Eq. 4) is calculated according to Eq. 5 (sheet resistivity) and Eq. 6 (electron mobility). For the electron mobility, Arora model [10] was used with parameters calibrated from [11] for 4H-SiC and from [12] for 3C-poly SiC. The contribution of the contacts is calculated as the resistance contributions deducted from the extracted measured differential resistance.

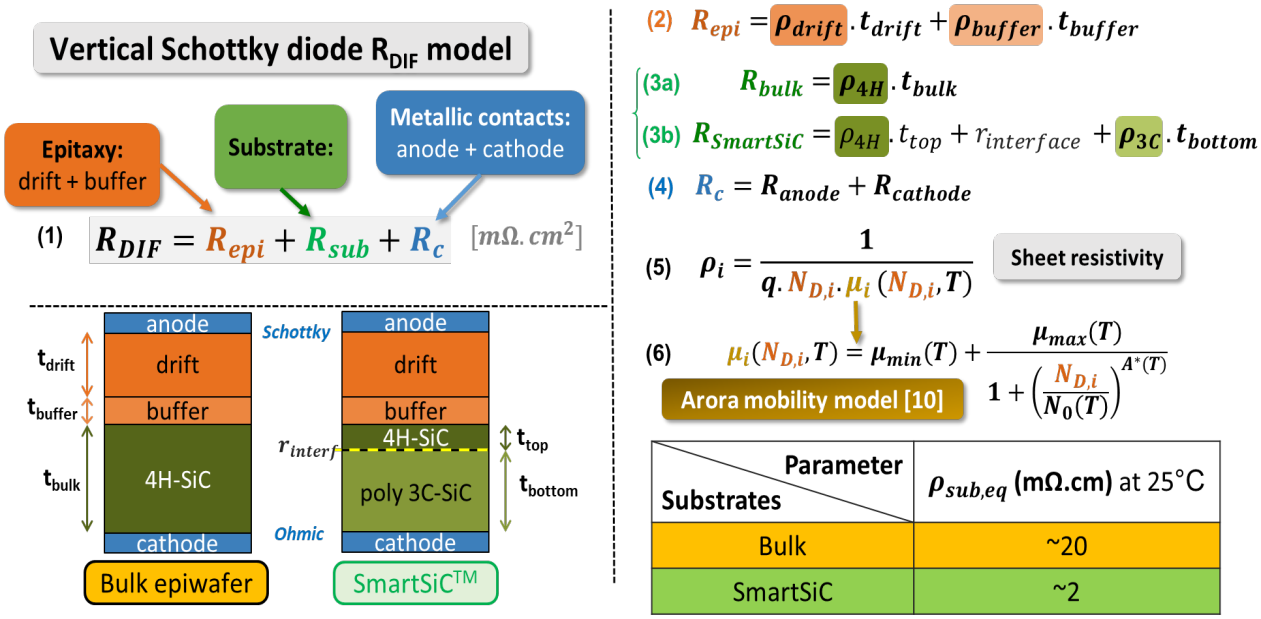

Fig. 8. Vertical SiC diode differential resistance partitioning model is composed of three primary contributors: epilayer (comprises drift and buffer layers), contacts (anode and cathode), and substrates (bulk vs. SmartSiC™). Arora model [10] for electron mobility is used to calculate the resistivity of each layer and construct the final partition.

R_{DIF} partitioning is calculated for both SmartSiC™ and bulk epiwafers in addition to a thinned down version of the bulk substrate at 25 ºC and 200 ºC temperatures as shown in Fig. 9. It is observed that SmartSiC™ substrate (350 µm, without thinning) exhibited lower resistance even compared to thinned (110µm) bulk epiwafer. Furthermore, these calculations bring new insights on the extracted $\Delta R_{DIF}(T)$ shown in Fig. 6c: the R_{DIF} gain can be attributed to the substrate (ΔR_{sub}) and partially to the back side contact ($\Delta R_{cathode}$), as the anode and epi components are identical for both samples.

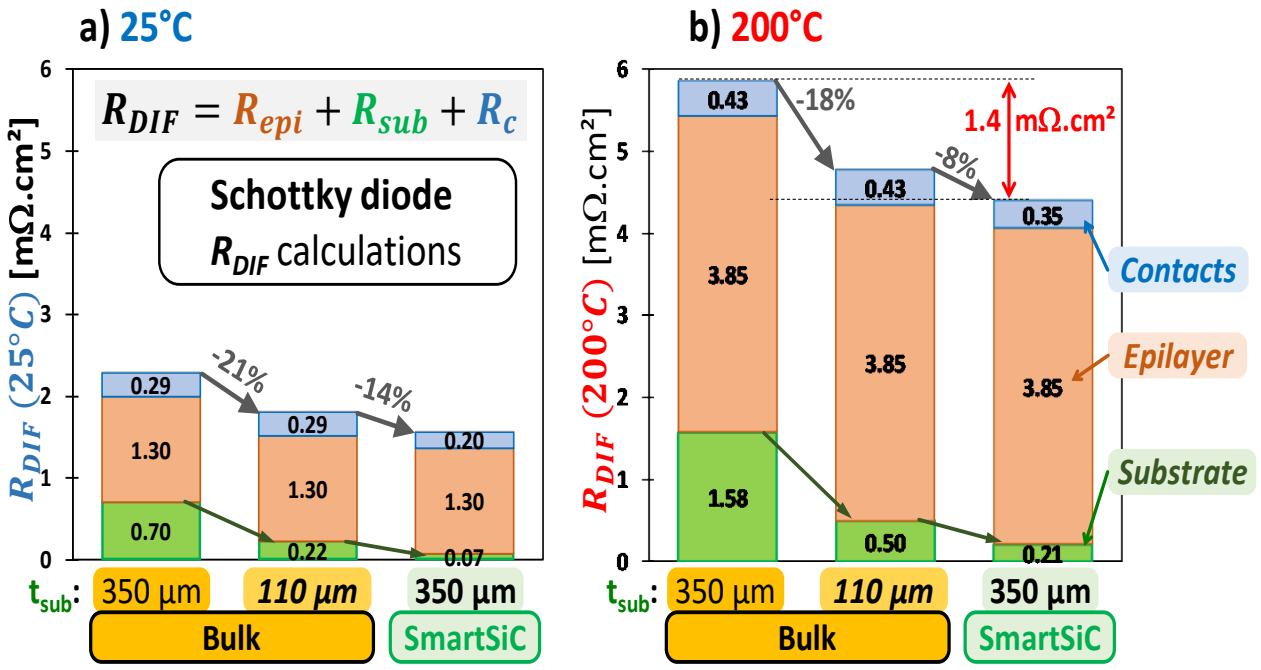

Fig. 9. R_{DIF} partitioning calculations at **a)** 25°C and **b)** 200°C for Schottky diodes with same epi. For bulk epiwafer, R_{DIF} is reduced with substrate thinning. SmartSiC™ substrate enables further R_{DIF} reduction without thinning.

Summary

This study compares 1200 V 4H-SiC power diodes on two different substrate technologies (single crystal 4H-SiC reference bulk and 3C-poly silicon carbide based substrates: SmartSiC™). The reverse mode measurements demonstrate that substrate material has a minimal impact on defect propagation affecting off-state performance, as both bulk and SmartSiC™ exhibit similar non-destructive avalanche characteristics due to identical drift layers and device structures. The specific differential resistance (R_{DIF}) decreases with an increase in Schottky surface ratio, with hexagonal configurations yielding the lowest resistance, particularly in SmartSiC™ samples. JBS diodes fabricated on SmartSiC™ showed superior current conduction and lower resistance in the ohmic regime, highlighting the significance of substrate resistivity. The results also reveal an exponential temperature dependence of R_{DIF}, indicating that substrate properties, including thickness, play a crucial role in high-temperature device performance.

Overall, introducing SmartSiC™ enables to optimize device performance (reducing specific on-resistance even at high temperature) while sustaining similar off-state behaviour compared to standard bulk. This study paves the way for further investigations related to dynamic performance and reliability/ruggedness to consolidate the SmartSiC™ position in power electronics.

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References

[1] E. Guiot, F. Allibert, J. Leib, T. Becker, W. Schwarzenbach, C. Hellinger, T. Erlbacher, and S. Rouchier, "Proven Power Cycling Reliability of Ohmic Annealing Free SiC Power Device through the Use of SmartSiC™ Substrate", MSF 1092, 201–207 (2023). https://doi.org/10.4028/p-777hqg

[2] S. Rouchier, G. Gaudin, J. Widiez, F. Allibert, E. Rolland, K. Vladimirova, G. Gelineau, N. Troutot, C. Navone, G. Berre, D. Bosch, Y.L. Leow, A. Duboust, A. Drouin, J.M. Bethoux, R. Boulet, A. Chapelle, E. Cela, G. Lavaitte, A. Bouville-Lallart, L. Viravaux, F. Servant, S. Bhargava, S. Thomas, I. Radu, C. Maleville, and W. Schwarzenbach, "150 mm SiC Engineered Substrates for High-Voltage Power Devices," MSF 1062, 131–135 (2022). https://doi.org/10.4028/p-mxxdef

[3] O. Bonnin, "SmartSiC™: A Greener, Faster and Better Technology for SiC," Semicon Europa Conference, 2023. https://www.semi.org/sites/semi.org/files/2023-12/5 Olivier%20Bonnin.pdf

[4] D. Clark et al., "CPD1 Clas-SiC Planar MPS/JBS diode Process Design kit", Clas-SiC Wafer Fab, 2021. https://clas-sic.com/

[5] G. Gelineau, J. Widiez, E. Rolland, K. Vladimirova, A. Moulin, V.S. Prudkovskiy, N. Troutot, P. Gergaud, D. Mariolle, S. Barbet, V. Amalbert, G. Lapertot, K. Mony, S. Rouchier, R. Boulet, G. Berre, W. Schwarzenbach, and Y. Bogumilowicz, "Evaluation of Crystal Quality and Dopant Activation of Smart Cut™ - Transferred 4H-SiC Thin Film," MSF 1089, 71–79 (2023). https://doi.org/10.4028/p-026sj4

[6] T. Kimoto, and H. Watanabe, "Defect engineering in SiC technology for high-voltage power devices," Appl. Phys. Express 13(12), 120101 (2020). https://doi.org/10.35848/1882-0786/abc787

[7] A. Gendron-Hansen, D. Sdrulla, B. Odekirk, A.S. Kashyap, and L. Starr, "4H-SiC 1200 V Junction Barrier Schottky Diodes with High Avalanche Ruggedness," MSF 924, 585–588 (2018). https://doi.org/10.4028/www.scientific.net/MSF.924.585

[8] J. Millan, V. Banu, P. Brosselard, X. Jorda, A. Perez-Tomas, and P. Godignon, "Electrical performance at high temperature and surge current of 1.2 kV power rectifiers: Comparison between Si PiN, 4H-SiC Schottky and JBS diodes," in 2008 International Semiconductor Conference, (IEEE, Sinaia, Romania, 2008), pp. 53-59. https://doi.org/10.1109/SMICND.2008.4703326

[9] W. Schwarzenbach, S. Rouchier, G. Berre, R. Boulet, O. Ledoux, E. Cela, A. Drouin, A. Chapelle, S. Monnoye, H. Biard, K. Alassaad, L. Viravaux, N.B. Mohamed, D. Radisson, G. Picun, G. Lavaitte, A. Bouville-Lallart, J. Roi, J. Widiez, K. Abadie, E. Rolland, F. Fournel, G. Gelineau, F. Mazen, A. Moulin, C. Moulin, D. Delprat, N. Daval, S. Odoul, P. Sandri, and C. Maleville, "Engineered SiC materials for power technologies," in 2022 International Conference on IC Design and Technology (ICICDT), (IEEE, Hanoi, Vietnam, 2022), pp. 55–56. https://doi.org/10.1109/ICICDT56182.2022.9933092

[10] N.D. Arora, J.R. Hauser, and D.J. Roulston, “Electron and hole mobilities in silicon as a function of concentration and temperature,” IEEE Trans. Electron Devices 29(2), 292–295 (1982). https://doi.org/10.1109/T-ED.1982.20698

[11] K. Tian, J. Xia, K. Elgammal, A. Schöner, W. Kaplan, R. Karhu, J. Ul-Hassan, and A. Hallén, “Modelling the static on-state current voltage characteristics for a 10 kV 4H–SiC PiN diode,” Materials Science in Semiconductor Processing 115, 105097 (2020). https://doi.org/10.1016/j.mssp.2020.105097

[12] A. Arvanitopoulos, N. Lophitis, K.N. Gyftakis, S. Perkins, and M. Antoniou, “Validated physical models and parameters of bulk 3C–SiC aiming for credible technology computer aided design (TCAD) simulation,” Semicond. Sci. Technol. 32(10), 104009 (2017). https://doi.org/10.1088/1361-6641/aa856b