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Designs of 1.2 kV Rated Semi-Superjunction MOSFET on the 2D and 3D Planes for Practical Realization

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Abstract. This paper investigates the charge balancing and performance optimization of two 1.2 kV rated Semi-Superjunction (SSJ) MOSFETs. Beginning with a conventional double trench MOSFET, SJ trenches are imposed in 2D (within the X-Y plane unit cell) and in 3D (trenches in Z-Y plane, perpendicular to the gate trench). The optimization of these structures focuses on the effects of p-pillar doping, tilt angle, and z-plane pillar width and the trade-off between specific on-resistance $R_{on,sp}$, breakdown voltage (BV), implantation window, and gate reliability is assessed for each configuration. The 2D SSJ MOSFET, is the device that offers the highest breakdown voltage of those assessed (1781 V) and the widest implantation window (±25.4%), when implemented with a vertical trench sidewall, while this is a trade-off against achieving the lowest $R_{on,sp}$, (1.15 mΩ.cm^2) with a 12.5° side wall angle. In the 3D SSJ MOSFET, a reduced p-pillar depth in the z-dimension, and hence a higher doping density, leads to a significant improvement in $R_{on,sp}$. The Z-plane p-pillars in the 3D device efficiently deplete its JFET region, causing the $R_{on,sp}$ of the 3D devices to be higher than the 2D devices, and the breakdown voltage lower. However, this also results in very low electric field (<0.5 MV/cm), in the gate oxide, offering a safe alternative to the 2D devices (1.69 MV/cm). Differences between the devices could be narrowed in the future with optimal JFET design.

Introduction

4H-silicon carbide (SiC) metal-oxide-semiconductor-field-effect-transistors (MOSFETs) are an efficient, fast-switching alternative to Silicon (Si) IGBTs in the 650-1700 V class. This is primarily due to SiC's 9 times larger critical electric field and relatively high thermal conductivity [1] compared to Si. Recently, double trench MOSFET architectures [2] have come to the fore that deliver a narrow cell pitch, thereby reducing, in turn, specific on resistance, die size and switching losses, while this structure also protects the gate oxide from high electric fields in the off state and in fault states such as short circuit.

Until now, the fast-paced advancement of SiC production methods is yet to result in a commercialized superjunction (SJ) MOSFET. While a SiC SJ could further improve the trade-off between breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$), from $R_{on,sp} \propto BV^{2.293}$ to $R_{on,sp} \propto BV^{1.007}$ [2], the multi-epitaxial SJ fabrication process used is not commercially feasible in SiC processing. This is due to the high cost, growth complexity, defect sensitivity, and low yield of fabrication [4]. However, demonstrator SJ devices produced via a trench etch and epitaxy refill method [5] or a trench etch and sidewall implant [5, 6], may offer a practical alternative. This is due to the more simplistic approach of reducing the number of epitaxial steps, providing better control over doping profiles and minimizing defect introduction. This leads to higher yields and lower production costs compared to multi-epitaxial methods.

To realize high-performing SJ structures in SiC devices, a high aspect ratio (trench depth divided by trench width) is required to uniformly distribute the electric field across the device. Achieving an optimal BV also depends on a precise dopant diffusion process that introduces a uniform P-doping layer, ensuring accurate charge balance between the alternating P- and N-doped regions. This enhances BV significantly without increasing device size or on-resistance, optimizing both performance and efficiency. However, in practice, this ideal case is difficult to achieve. The SJ structure faces implantation challenges as maintaining an exact doping concentration along the entire depth of a deep trench is technically complex. More critically, the sidewall plays a vital role in the performance of the SJ structure, as it is crucial to maintaining a constant doping concentration along the entire depth of a deep trench. This ensures effective charge balancing and electric field distribution. Typically, the doping variation can range between 5% to 10% depending on several factors, which leads to charge imbalance, reducing the maximum achievable BV and potentially degrading the device's overall performance and reliability [7]. In a prior study, the reduction of the strict SJ requirements of optimal trench aspect ratio and doping implantation window was explored on 1.7 kV SiC Schottky diodes [6]. This was done through a combination of varying sidewall tilt angles to expand the implantation window, and semi-Superjunction (SSJ) implementations to reduce the trench depth and fabrication costs.

In this study, the implementation of two practical SSJ topologies are compared in Sentaurus TCAD simulations. The starting point of the investigation is a 650 V rated double trench MOSFET benchmarked elsewhere [8], from which two SSJ MOSFET implementations are developed in the same thickness of epitaxy. A conventional, 2D SSJ implementation is produced entirely within the X-Y plane by extending the existing source trenches throughout the epitaxial region, implantations into the sidewalls resulting in a charge balanced SSJ. This is compared with a 3D implementation, in which a trench is etched in the X-Z plane, behind the active gate trench.

SJ technology is usually implemented at relatively high voltages. However, even at 650-1200V, a SSJ will be shown to facilitate lower drift region resistance contributions compared to the double trench MOSFET, while supporting a higher voltage rating. Were this to be paired with innovations that reduce the channel resistance [9], and the substrate resistance [10], this could lead to a highly efficient, low resistance MOSFET.

Simulated Structure

The location of the SSJ p-pillar is explored in planes both parallel (X-Y, "2D device") and perpendicular (Z-Y, "3D Device") to the device active area, as seen in Fig.1. The SSJ SiC MOSFETs are developed using a trench etch and sidewall implantation. The device substrate consists of a n+ substrate with a doping concentration of 1×10^{19} cm^{-3} , that is assumed to have been thinned to 140 μm. The drift region has been split into three vertical sections; a 1 μm N-bottom assist layer (NBAL) with a doping concentration of 1.5×10^{16} cm^{-3}, a charge balanced, low resistance n-drift region, and finally then a low doped Junction Field Effect Transistor (JFET) region designed to fully deplete to protect the gate oxide. In prior literature, the NBAL structure has been shown to support the higher electric field spread at the base of the SJ by providing a gradual transition from the high-resistance substrate to the low resistance drift region [11].

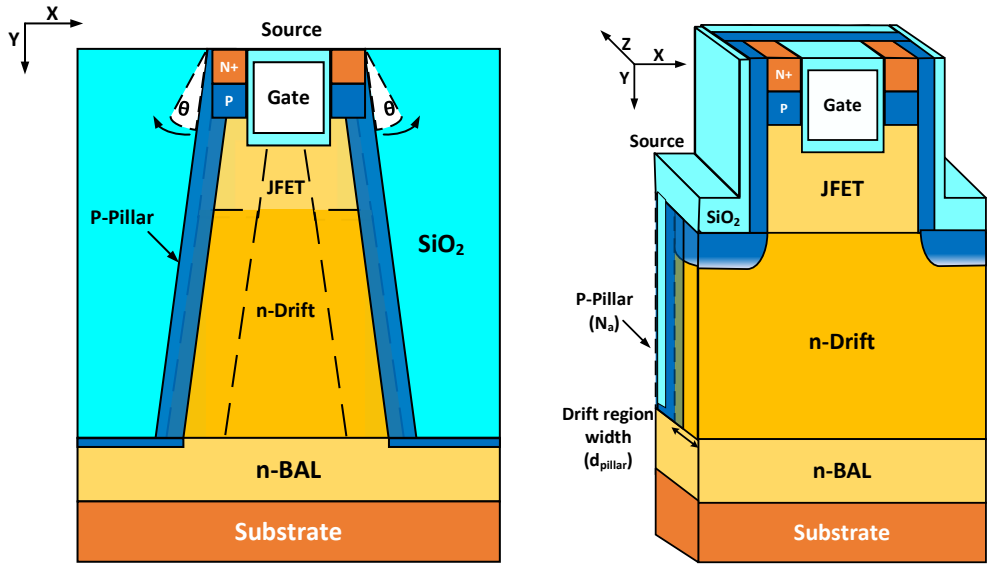

Fig.1.a. A 2D (2D plane, parallel trench) SiC SSJ with varying P-pillar tilt (θ). **Fig.1.b.** A 3D (Z-Y plane, perpendicular trench) SiC SSJ with varying drift region width (d_{pillar}).

For the 2D SSJ MOSFET, a 6.8 µm n-Drift region with a fixed doping concentration of N_D=1×10^{17} cm^{-3} is grown. For the 3D SSJ MOSFET, a 6.8 µm n-drift region is also grown, however N_D is varied from 2×10^{17},1×10^{17}, and 5×10^{16} cm^{-3} for a drift region width (d_{pillar}) of 0.5, 1, and 2 µm half-cell, respectively. Above the drift region, a 1.8 µm thick JFET region is grown with a fixed doping concentration of 1.5×10^{16} cm^{-3}. Above this, a 0.4 µm 3.8×10^{18} cm^{-3} P channel region and a 0.2 µm 1×10^{19} cm^{-3} N+ contact region. A trench of 0.8 µm is created to create the gate. For the 2D SSJ MOSFET, a trench of 6.8 µm is created on the sides of the active region to implant a thin P-doped layer of 5 nm for the SSJ. The trenches are wide enough to ensure a tilted implantation (20° from vertical) can reach the entire trench sidewall. Where implemented, a sidewall angle of up to 12.5° pivots from the device surface, effectively widening the lower drift region, but ensuring minimal impact on the gate structure. For the 3D SSJ MOSFET, 1.8 µm deep source trenches are formed for the P-doping implantation of the source P-wells. Perpendicular, in the X-Z plane, a 6.8 µm deep trench allows for the implant of a thin P-doped layer of 5 nm for the SSJ. The SSJ trench width is fixed at 1 µm for both 2D and 3D SSJ MOSFETs. All trenches are passivated with Silicon Dioxide (SiO_2). All P-doped regions are formed using Aluminum ion implantation. The selection of the N_D doping concentration is calculated through Gauss's Law based on a critical electric field of 2.0 MV/cm for 4H-SiC [12].

The devices are simulated at room temperature using the "Sentaurus" module from the TCAD package Synopsys.

Table 1. Summary of key device design geometry and parameters.

Symbol	Definition	2D P-pillar tilt (°)	3D half-cell thickness (µm)	Units
		0, 2.5, 5, 7.5 10,12.5	0.5, 1, 2	
t_{depth}	Drift region depth	8.6	8.6	
t_{cell}	Cell pitch	2	1, 2, 4 (z-axis) 2 (x-axis)	
t_{sub}	Substrate thickness	140	140	µm
d_{pillar}	Drift region width	1	1, 2, 4	
t_{pdop}	P-pillar thickness	5	5	nm
N_D	Drift region doping	1×10^{17}	2×10^{17}, 1×10^{17}, 5×10^{16}	cm^3
N_{BAL}	n-Bottom Assist Layer doping	1.5×10^{16}	1.5×10^{16}	
N_{sub}	Substrate doping	1×10^{19}	1×10^{19}	
V_{th}	Threshold Voltage	~6.33	6.55, 7.04, 7.08	V
$R_{on,sp}$	Specific on-resistance	1.61, 1.51, 1.46, 1.34, 1.23, 1.15	1.52, 1.63, 2.36	$m\Omega.cm^2$
BV_{max}	Max. Breakdown Voltage	1781, 1728, 1668,1591, 1520, 1431	1539, 1540, 1338	V

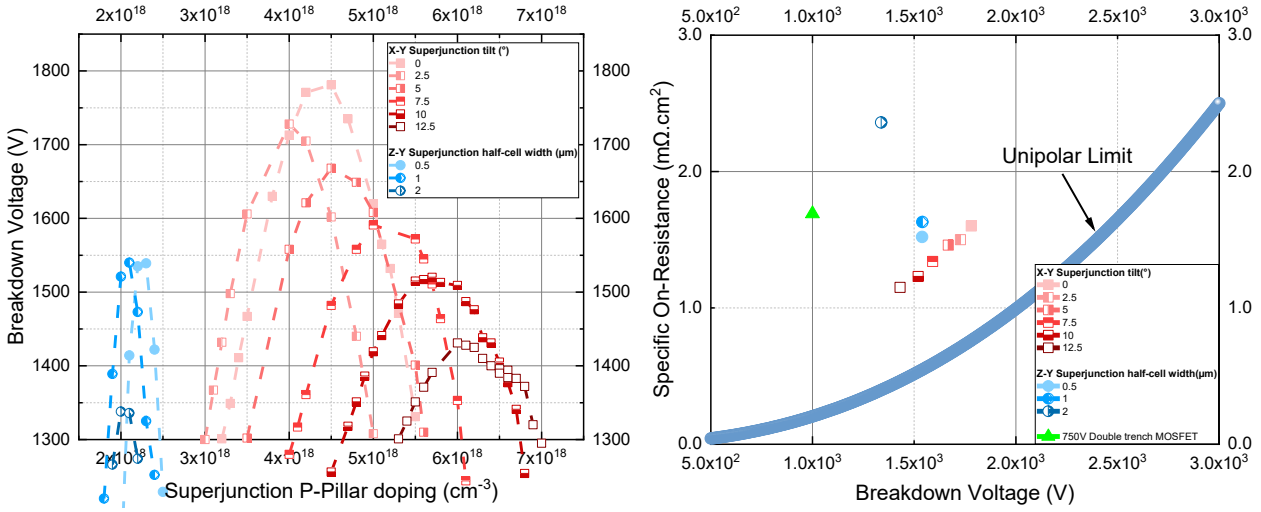

Fig.2. (left) Comparison of the 2D SiC SSJ with varying θ and 3D SiC SSJ with varying drift region width (d_{pillar}) on the optimal SJ p-pillar doping required for charge balancing. **Fig.3**. (right) Trade-off between the BV and $R_{on,sp}$ for the 2D plane SiC SSJ with varying θ and 3D SiC SSJ with varying drift region width (d_{pillar}).

Results and Discussion

Charge balancing simulations, shown in Fig. 2a, are carried out to analyze the effect that SJ p-pillar doping has on the implantation window, the allowable discrepancy from the optimum doping. The implantation window is defined in this study as the percentage difference between the optimal SJ P-pillar doping for maximum breakdown voltage and the minimum doping required to achieve a 1300 V breakdown voltage. For the 2D SSJ MOSFET, this shows a clear decreasing trend with increasing tilt angle, with a ±26.9% implantation window at 0°, ±25.4% at 2.5°, ±23.0% at 5°, ±21.1% at 7.5°, ±18.1% at 10°, and ±13.9% at 12.5°. This implies that increasing the tilt angle reduces the processing window, making it more difficult to precisely control the implantation process to avoid breakdown voltage degradation. This could present challenges in manufacturing, particularly for devices

requiring higher tilt angles for other design constraints. For the 3D SSJ MOSFET, there is a slight increase in implantation window with d_{pillar} by ±11.1% at 1 µm to ±12.1% at 2 µm. However, there is massive drop in implantation window to ±5.0% at 4 µm. This suggests that a smaller d_{pillar} offers a wider processing window, making the device more robust to doping variations, while larger widths significantly constrain the window, suggesting that larger structures require stricter control over the doping process to prevent performance loss. These implantation window changes are visualized in Fig.2.

In addition, each SSJ MOSFET is compared to the theoretical unipolar limit of 4H-SiC, shown in Fig.3, to quantify the BV vs $R_{on,sp}$ performance. The no tilt (0°) 2D SSJ MOSFET achieves a $R_{on,sp}$ of 1.6 mΩ.cm^2, 5.9% lower than the original benchmarked double trench MOSFET. With increasing tilt angle, this improves further, a tilt angle of 2.5, 5, 7.5, 10, 12.5°, reducing the $R_{on,sp}$ by a further 6.3, 8.8, 16.3, 23.1, 28.1% compared to no-tilt (0°). This is potentially due to reduction in JFET resistance as a larger JFET area is required for increasing tilt angle. As a result, these designs could offer significant advantages for applications at a 1.2 kV rating requiring lower conduction losses and higher efficiency while still maintaining a balance between BV and $R_{on,sp}$.

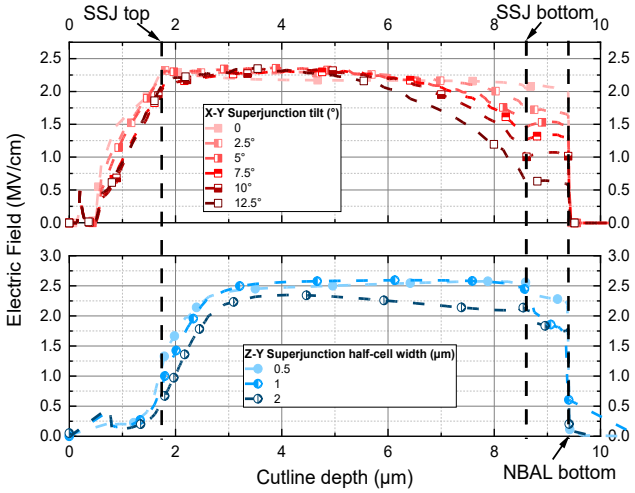

Fig.4. Electric field profiles along active region of devices (seen in fig.1) for the 2D (top) and 3D (bottom) SSJ MOSFET at breakdown voltage.

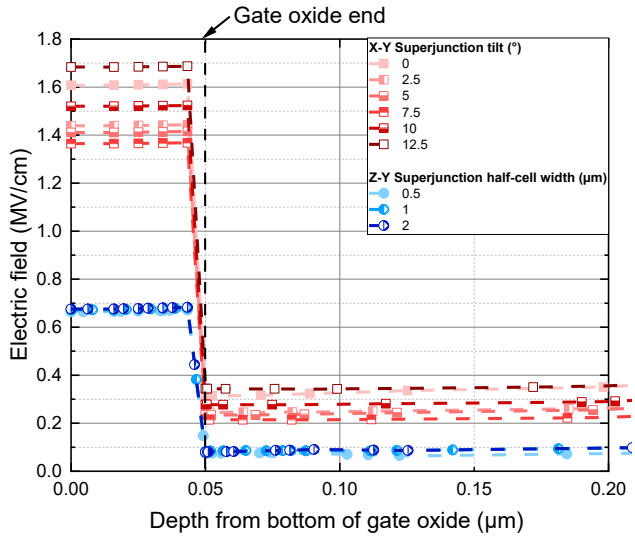

Fig.5. Electric field profiles along the gate oxide to 0.2 µm below gate oxide depth (seen in fig.1) for the 2D (top) and 3D (bottom) SSJ MOSFET at 800V voltage.

The 3D SSJ MOSFET shows an improvement in $R_{on,sp}$ with reducing d_{pillar}. At d_{pillar}=1 μm, the resistance is 1.5 mΩ.cm^2, 10.6% lower than the original benchmarked double trench MOSFET. This is 37.5% lower compared to a d_{pillar} of 2 μm, due to the impact of a higher N_D of 2×10^{17} at 1 μm, compared to 5×10^{16} at a 4 μm d_{pillar}. This contributes to the reduction of the JFET resistance, which results in a total net decrease in $R_{on,sp}$ for the 3D SSJ MOSFET. It can be noted that the 2D SSJ MOSFET with a 12° tilt angle has the lowest $R_{on,sp}$ due to the minimized JFET resistance. These results can be visualized in Fig.3.

The effect of the SSJ on both 2D and 3D MOSFETs on BV can be further analyzed through the electric field profile at the point of breakdown, shown in Fig.4. For the 2D device with a vertical sidewalls (0° tilt), a flat electric field profile can be seen between the top (1.8 μm) and the bottom (8.6 μm) of the drift region, which is symbolic of a balanced SJ. As the tilt angle increases, three effects combine to reduce the total voltage supported. First, the increasing tilt angle causes the SJ region to become increasingly unbalanced, the charge imbalance becoming more pronounced in the centre, bottom of the drift region. With a tilt angle of 0, 2.5, 5, 7.5, 10 and 12.5° the electric field at the bottom of the SJ region, drops from 2.1 MV/cm to 1.7, 1.4, 1.3, 1.0 and 0.6 MV/cm, respectively. Second, a reduction in electric field at the bottom of the SJ region reduces the field supported within the NBAL region, so the field supported in the NBAL also reduces with increasing tilt angle. Thirdly. the electric field at the top of SJ region also reduces from 2.1 MV/cm for a tilt angle of 0 - 5°, to 1.8 MV/cm for a tilt angle of 7.5 – 12.5°. These results explain the breakdown results seen, the maximum BV reducing with increasing tilt angle.

The electric field at the bottom of the 3D SSJ MOSFET decreases with d_{pillar}, at 2.5, 2.4, 2.1 MV/cm at a d_{pillar} of 0.5, 1, and 2 μm, respectively. There is also a similar decrease in electric field seen at the SSJ start, of 1.0, 0.9, and 0.6 MV/cm for a d_{pillar} of 0.5, 1, and 2 μm, respectively. There is also an impact of reducing electric field held within the NBAL region during breakdown with increasing d_{pillar}, seen in Fig.4. These results also correspond with the breakdown results seen, with the charge balance effect weakening, causing the BV to reduce as d_{pillar} increases.

The 2D SJ devices support a greater BV than the 3D SJ devices, as seen in Fig.2. This can be explained by comparing their electric field profiles in the JFET region, seen in Fig.4. The electric field profile in the JFET region of the 3D device is kept at a very low level, below 0.5 MV/cm. This occurs because the additional SJ pillars in the Z-X plane, result in the JFET region being surrounded on all four sides by P+ regions. This results in a lateral depletion effect that is stronger than the vertical one, fully depleting this region. In contrast the JFET region of the conventional 2D device is confined on only two planes and a vertical field is allowed to penetrate this region.

This difference in electric field within the JFET region has an impact on gate reliability, which is a significant factor to consider for device design performance. The electric field held within the gate oxide at the operating voltage (assumed to be 800V for these devices as they block >1300V) significantly impacts the reliability, efficiency, and long-term stability of MOSFETs. Seen in Fig.5, the electric field in the gate oxide of the 3D device is much lower than the 2D device, due to the strong lateral depletion effect in the 3D JFET. The very low gate oxide electric field of 0.67 MV/cm is present for all the 3D SSJ MOSFET devices. For the 2D devices, a tilt angle of 7.5° results in the minimum gate oxide electric field of 1.38 MV/cm for. The 12.5° tilted device performs the worst in the dataset, with an electric field of 1.69 MV/cm.

Through all the devices in this investigation, the JFET doping was held constant at 1.5×10^{16} cm^{-3}, as per the original benchmark device. This value proved to be relative low for the 3D device, its full lateral depletion offering maximum protection to the gate and preventing any electric field increase that would contribute to the total blocking voltage. Conversely, in the 2D device, the JFET doping appears too high, as the field was allowed to penetrate this region, adding a significant

contribution to the total voltage, while jeopardizing the oxide reliability. It is clear that in future studies the relative gap between these structures could be narrowed through JFET doping optimization.

Conclusion

The paper presents an extensive analysis of charge balancing in SSJ MOSFETs, exploring the effects of a 2D vs 3D implementation, P-pillar doping and geometrical factors such as tilt angle on performance parameters $R_{on,sp}$, BV and gate oxide electric field, and implantation window. For the 2D implementation, increasing the tilt angle up to 12.5° reduces $R_{on,sp}$ by effectively widening the JFET region. However, the increased tilt angle also narrows the implantation window and reduces the breakdown voltage as greater charge imbalance occurs. For the 3D SSJ MOSFET reducing the pillar depth allows for higher doping concentrations, significantly improving the $R_{on,sp}$,. However, a narrow implantation windows reduce the practically of implementing such a design. The importance of the JFET region on gate oxide reliability and breakdown voltage was revealed as a key trade off in the two device implementations. In the 2D MOSFETs, a relatively weak lateral depletion from its two sides allowed field to penetrate to the gate, adding blocking voltage but increasing the field in the gate oxide. This could be optimised, using a tilt angle of 7.5° but this remained 2.5 times higher than the 3D implementation, where a strong depletion on four sides of the JFET region fully prevented a vertical field building up and lowering BV. The findings provide an insight into optimizing SJ device design for better efficiency and reliability, highlighting the trade-offs between doping, geometrical structure, and performance metrics in SSJ MOSFETs.

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