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Superior Characteristics of Body Diode in DMOSFET Fabricated on 4H-SiC Bonded Substrate

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Abstract. A novel substrate of 4H-SiC bonded substrate is expected to solve issues such as decreasing the on-resistance, which has attracted much attention. Therefore, several studies have been conducted on the use of bonded substrates. In this study, we fabricated a DMOSFET on a bonded substrate and compared its static and dynamic characteristics with those on a single-crystal substrate. Consequently, the on-resistance of the DMOSFET fabricated on a bonded substrate was lower than that on a single-crystal substrate owing to the low resistivity of the polycrystalline substrate. Also, reverse recovery loss of the DMOSFET fabricated on a bonded substrate was lower than that on single-crystal substrate at high temperature due to low carrier lifetime in a drift layer. Additionally, we observed that the DMOSFET fabricated on a bonded substrate did not generate bipolar degradation despite the application of a forward-current stress of over 1500 A cm^{-2}. According to these results, we expected that the carrier lifetime in both drift layer and transfer layer was decreased on a bonded substrate.

Introduction

Power devices based on silicon carbide (SiC) are being increasingly developed. However, these devices still have issues such as on-resistance and long-term reliability. Recently, a novel substrate comprising an extremely thin (submicron) monocrystalline 4H-SiC layer bonded to a polycrystalline 3C-SiC substrate, we called bonded substrate, was developed [1] [2]. However, there have been few studies on devices fabricated using bonded substrates, especially MOSFETs. This bonded substrate is expected to reduce the on-resistance of the vertical device and simplify the formation of the backside ohmic contact [3]. In addition, suppression of forward-bias degradation has been reported for PiN diodes [4], that is, the bonded substrate is expected to be effective as a body diode in MOSFET. Therefore, the purpose of this study was to verify the properties of a Double-implanted MOSFET (DMOSFET) fabricated on a bonded substrate. In this study, we fabricated a DMOSFET on a bonded substrate and compared its static and dynamic characteristics, suppression of forward bias degradation, and high-temperature reliability with those for monocrystalline substrate.

Experiment

1. Fabrication of bonded substrate

Figure 1 shows a flowchart of the 4H-SiC bonded substrate (SiCkrest^{TM}) manufactured by SICOXS. A polished monocrystalline substrate was implanted with proton and phosphorus ions. Subsequently, the monocrystalline substrate was directly bonded with the polished polycrystalline substrate, and the bonded one was thermally split into two. In these processes, the bonded substrate forms a thin monocrystalline layer, called the transfer layer, on top of the polycrystalline substrate. The transfer layer thickness is approximately 0.5 μm and its doping concentration is the same as that of a conventional monocrystalline substrate. However, the doping concentration of the polycrystalline substrate is higher than that of the monocrystalline substrate. Thus, the bonded substrate has lower resistivity than the conventional monocrystalline substrate.

2. Fabrication of DMOSFETs

Figure 2 shows the cross-sectional schematics of 1.2 kV-class DMOSFETs fabricated on a 4H-SiC single-crystal substrate (mono-MOS) and a SICOXS's 4H-SiC bonded substrate (bonded-MOS). The resistivity of the bonded substrate is approximately 8 mΩ·cm, which is approximately one-third of that of the single-crystal substrate. The fabrication conditions and device structures, including the drift layer, were identical. The drift layer thickness and concentration were 10 μm and 1.0×10^{16} cm^{-3}. The drift layers on both substrates were grown under the same conditions, such as temperature and gas flow. The DMOSFET structure was formed by conventional double-implantation technique in which the p-base and p^+-contact region were implanted with aluminum ions, and the n^+-source was implanted with phosphorus ions. The gate oxide film thickness was 50 nm, which was formed by high-temperature chemical vapor deposition and nitric oxide (NO) annealing, and phosphorus doped gate polysilicon was formed on the gate oxide film. The ohmic metals for the source and drain electrodes were Ni and Ti/Ni, respectively. The chip size of the fabricated DMOSFET was 3×3 mm^2, and its chip thickness was approximately 350 μm; without thinning process.

3. Measurement

The fabricated DMOSFETs were characterized by static current–voltage measurements and reverse recovery of the body diode. Furthermore, the forward voltage shift caused by the forward current stress and high temperature reliability were tested. Each testing conditions were shown in each experiment summary.

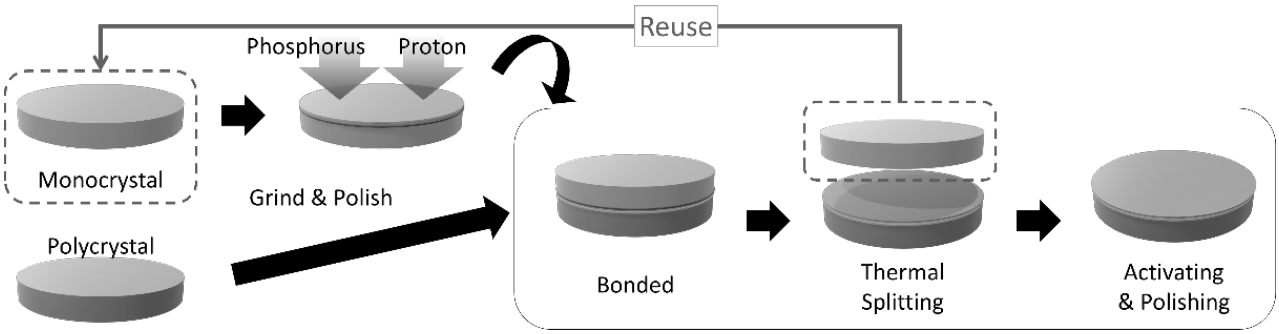

Fig.1 Brief flowchart the 4H-SiC bonded substrate[8]

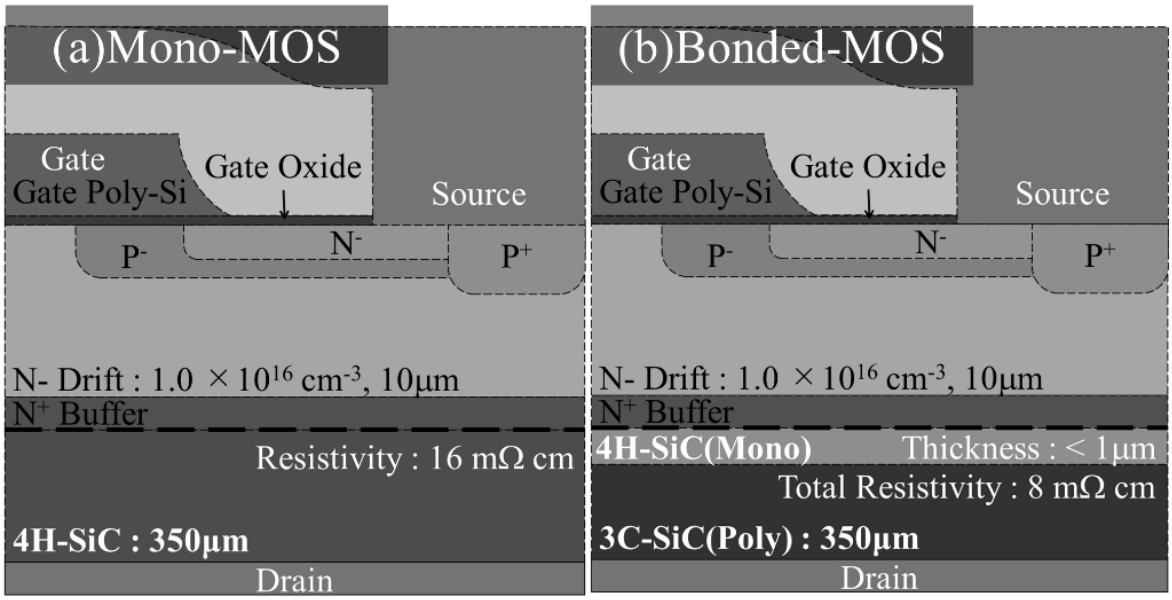

Fig.2 Schematic cross-section of a DMOSFET

Results and Discussions

1. Static characteristics of DMOSFETs

First, we evaluated the static characteristics of the MOSFET part in the fabricated DMOSFET at room temperature (RT) and 175 ℃. Fig. 3 shows the blocking characteristics. Both the mono-MOS and bonded-MOS exhibited similar blocking voltage (V_B) over 1500V at each temperature. On the other hand, the drain current (I_D)–drain voltage (V_D) characteristics exhibited clear differences between mono-MOS and bonded-MOS, as shown in Fig. 4. At a drain current of 20A, the bonded-MOS had 0.4% and 2.1% higher current than the mono-MOS at RT and 175 ℃, respectively. The suppressed on-resistance is primarily caused by low-resistivity polycrystals in the bonded substrates.

2. Static and dynamic characteristics of body diodes

Second, we evaluated the static characteristics of the body diodes in the fabricated DMOSFET on each substrate at RT and 175 ℃. Fig. 5 shows the forward current (I_F)–forward voltage (V_F) characteristics of the body diode inside the fabricated DMOSFETs. At RT, almost no differences were observed between the two devices, despite the bonded substrate having a lower resistance. This means the low lifetime of minority carrier in the bonded-MOS. Furthermore, at high temperature, although V_F decreases by the lifetime increasing, the bonded-MOS exhibited a higher V_F than the mono-MOS. However, considering the dead time of inverter operation, the increase in conduction loss is negligible. This trend was similar to that of a PiN diode fabricated on a bonded substrate [4]. We believe that the lifetime of minority carriers in the drift layer is suppressed even at high temperatures compering to on a single-crystal substrate when the drift layer is grown on a bonded substrate.

Next, we examined the reverse-recovery characteristics because it was also influenced by the lifetime of minority carrier. Fig. 6 shows the reverse-recovery waveform of the body diode. The reverse recovery current (I_{RR}) exhibited almost no difference between mono-MOS and bonded-MOS at RT, which might be due to the dominant junction charge. In contrast, the I_{RR} of the bonded-MOS was lower than that of mono-MOS at high temperature. These reverse-recovery charge (Q_{RR}) values calculated by the integral of I_{RR} along time was 30% less than that of mono-MOS. In other words, the recovery loss of bonded-MOS is less than that of mono-MOS at high temperature. This result also indicates that carrier lifetime of bonded-MOS is lower than that of mono-MOS.

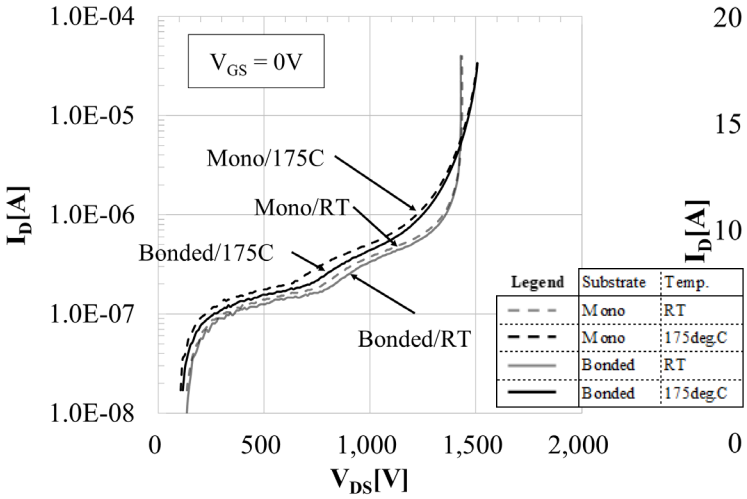

Fig. 3 Dependence of the blocking characteristics of DMOSFETs on temperature

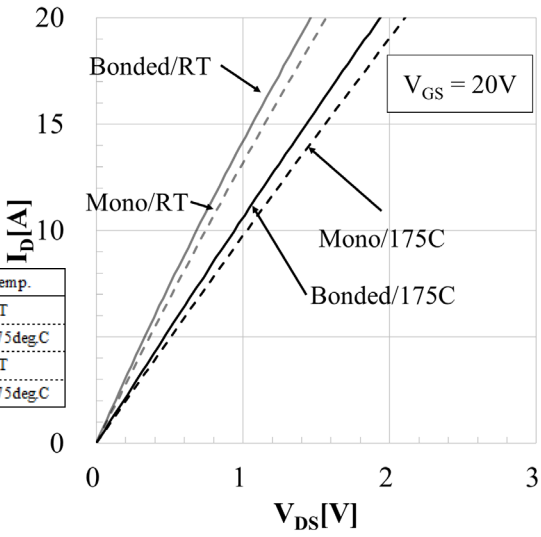

Fig. 4 Dependence of the I_D–V_D characteristics of DMOSFETs on temperature

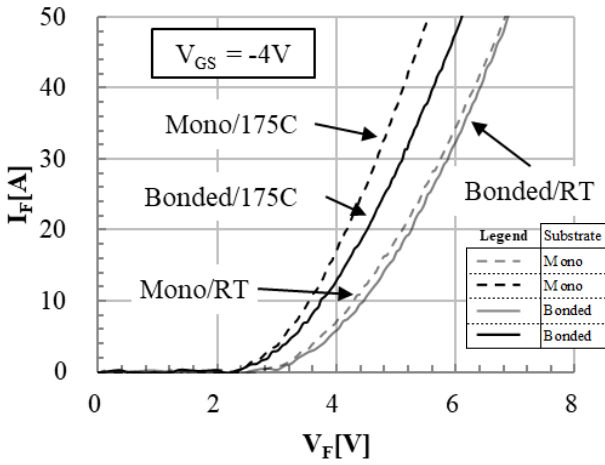

Fig. 5 Dependence of the I_F–V_F characteristics of DMOSFETs on temperature

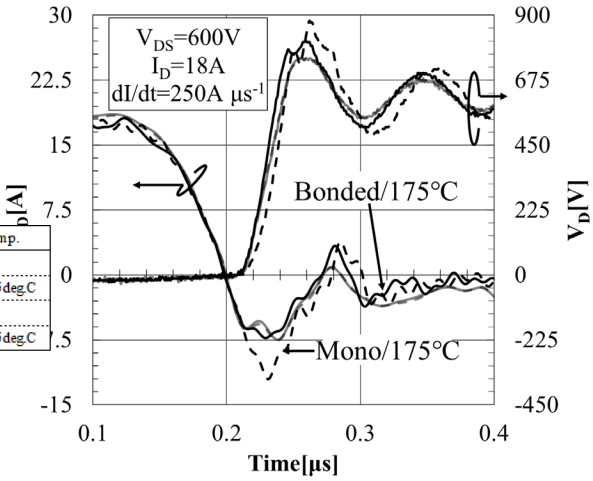

Fig. 6 Reverse-recovery waveforms of the body diode

3. Forward current stress testing

Previous studies have demonstrated that forward-bias degradation was suppressed in a PiN diode fabricated on bonded substrate [4]. Therefore, we examined forward voltage shift (ΔV_F) of body diode. Forward current stresses of 100, 500, 1000, and 1500 A cm^{-2} were applied on the body diodes using direct (DC) or alternating current (AC) and their ΔV_F were evaluated after the test. Fig. 7 shows the flowchart diagram of the forward current stress test and the definition of the forward voltage shift. Increased current stress was applied in four steps at 175 °C. The degree of forward bias degradation was quantitatively defined as ΔV_F at a forward current (I_F) of 60 A, as shown in right graph in fig. 7. Fig. 8 shows the I_F-V_F characteristics before and after the forward current stress test. Almost no differences were observed between the MOSFETs before the stress testing; however, the mono-MOS had a clearly lower current than the bonded-MOS at the end of the testing. The summary of the ΔV_F changes by the forward current stress test is shown in Fig. 9. The ΔV_F increases with increased current stress in the mono-MOS, whereas it remained unchanged in the bonded-MOS even after testing at 1500 A cm^{-2}.

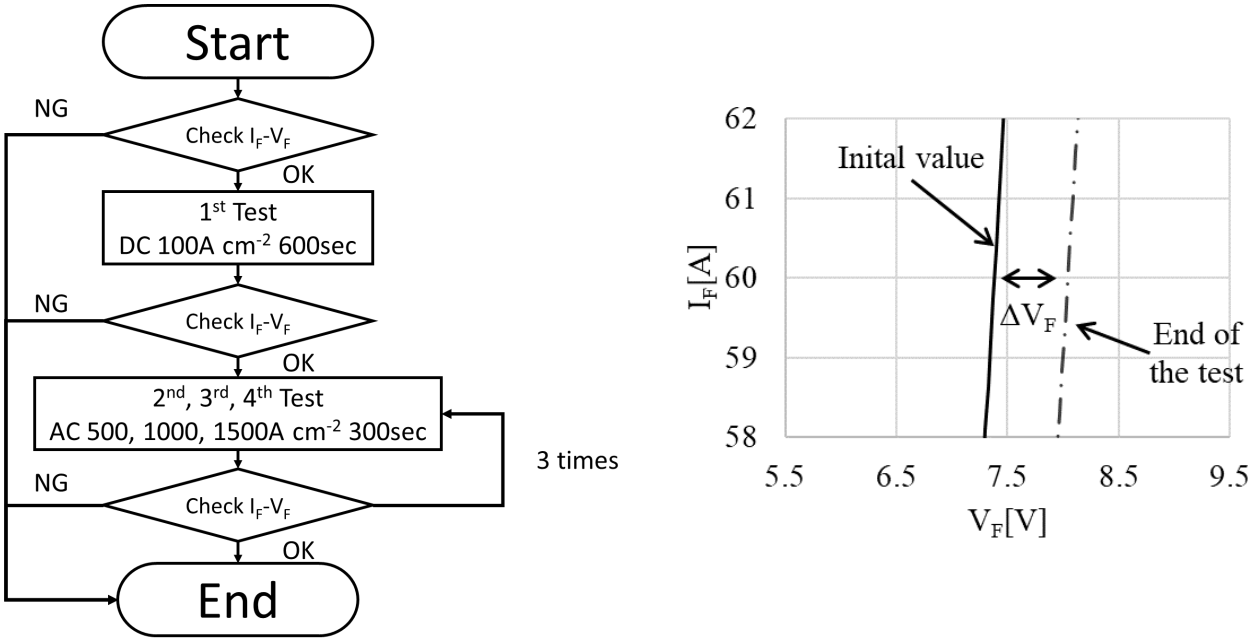

Fig. 7 Flowchart diagram of the forward-current stress test and definition of ΔV_F

The increase in ΔV_F is generally caused by the expansion of Shockley stacking faults (SSFs). Thus, after the test, all materials constituting the device on the drift layer were removed, and SSFs were observed using photoluminescence (PL) imaging. Fig. 10 shows the PL imaging results with a 420 nm band-pass filter obtained for each sample. Numerous SSF expansions were observed over the entire area of the mono-MOS. However, SSFs were not observed in the bonded-MOS. These tendencies were the same as those of a PiN diode fabricated on a bonded substrate [5]. They confirmed that the SSFs expanded in the epitaxial layer and stopped above the transfer layer by TEM observation. It was suggested that proton implantation for the wafer splitting process might generate a large number of trap centers such as $Z_{1/2}$ which decreased the lifetime and suppressed the SFF expansion in the transfer layer. On the other hand, decreasing of I_F and I_{RR} were originated from the low carrier lifetime in the drift layer of the bonded-MOS. Therefore, we expect that the low carrier lifetime in the drift layer is caused by trap centers including the $Z_{1/2}$ diffused from the transfer layer. Actually, increased $Z_{1/2}$ with shortened carrier lifetime were measured by DLTS and μ-PCD in the drift layer on bonded substrate [6].

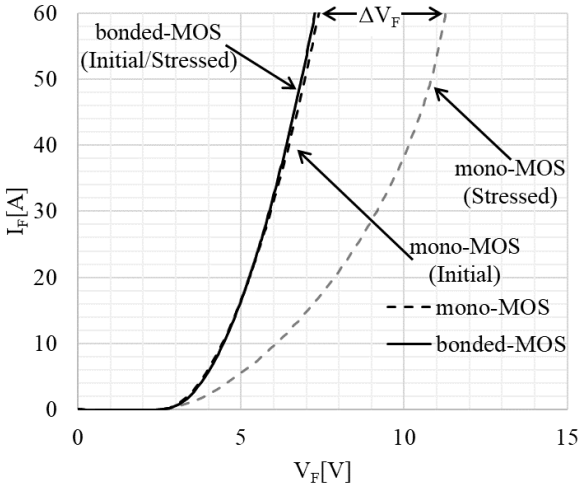

Fig. 8 I_F–V_F waveforms at the start and end of testing

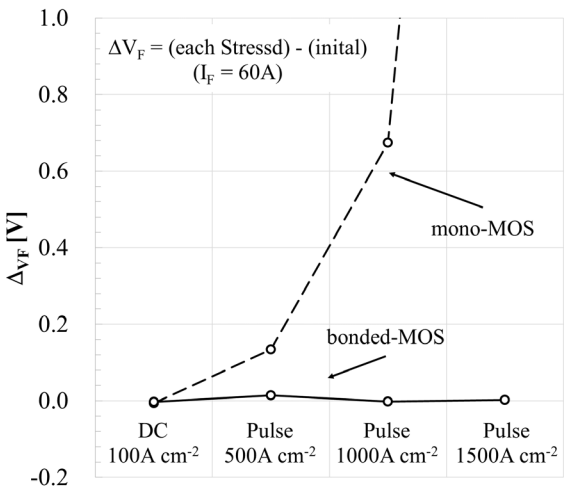

Fig. 9 Changes in the ΔV_F caused by forward-current stress of the body diode

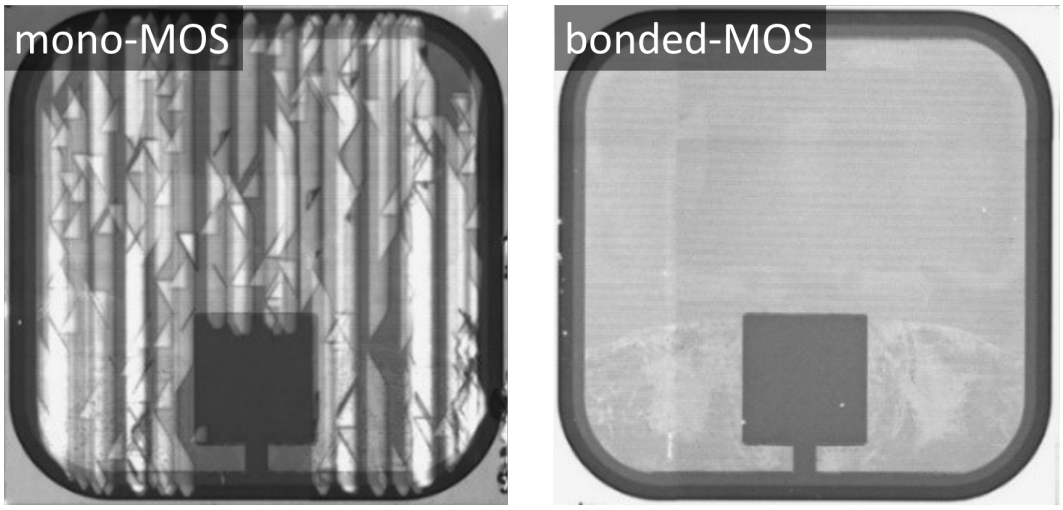

Fig. 10 PL imaging results after the stress testing (a band-pass filter of 420 nm is applied)

Table 1 Test conditions for HTRB and burn-in

Test item	Test Condition	Duration	Number of samples
HTRB	T_a= 175˚C V_R = 1200V	1000hr	8(each 4)
Burn-in	T_a = 175˚C V_{GS} = +20/-10V	1000hr	6(each 3)
	T_a = 175˚C V_{GS} = +22/-12V	1000hr	6(each 3)

4. High Temperature Reliability

High temperature reliability was compared between the fabricated bonded-MOS and mono-MOS to confirm the long-term reliability characteristics. We conducted high-temperature reverse bias (HTRB) and burn-in tests for each fabricated device. Table 1 lists the test conditions. Before and after the tests, reverse leakage-current (I_{DSS}) at a V_{DS} of 1.2 kV, breakdown voltage (BV) at I_D of 0.2 A, gate leakage-current (I_{GSS}) at V_{GS} of 22 V, and threshold voltage (V_{th}) at V_D of 10 V and I_D of 18 mA were evaluated. In addition to the standard condition, severe gate voltages (V_{GS}) were applied for burn-in test to confirm under more severe conditions. Figs. 11 and 12 shows the current–voltage characteristics at five different time points (0, 100, 300, 500, and 1000 h) by the two tests. The HTRB test results exhibited no significant differences between the two devices. In addition, the burn-in test results, including severe conditions, exhibited no significant differences, similar to the HTRB. These results were also similar to other reported reliability test results of DMOSFETs fabricated on monocrystalline substrate [7]. Therefore, we believe that the bonded-MOS has no issue concerning the high temperature reliability. It is necessary to investigate the long-term reliability at the bonded interface.

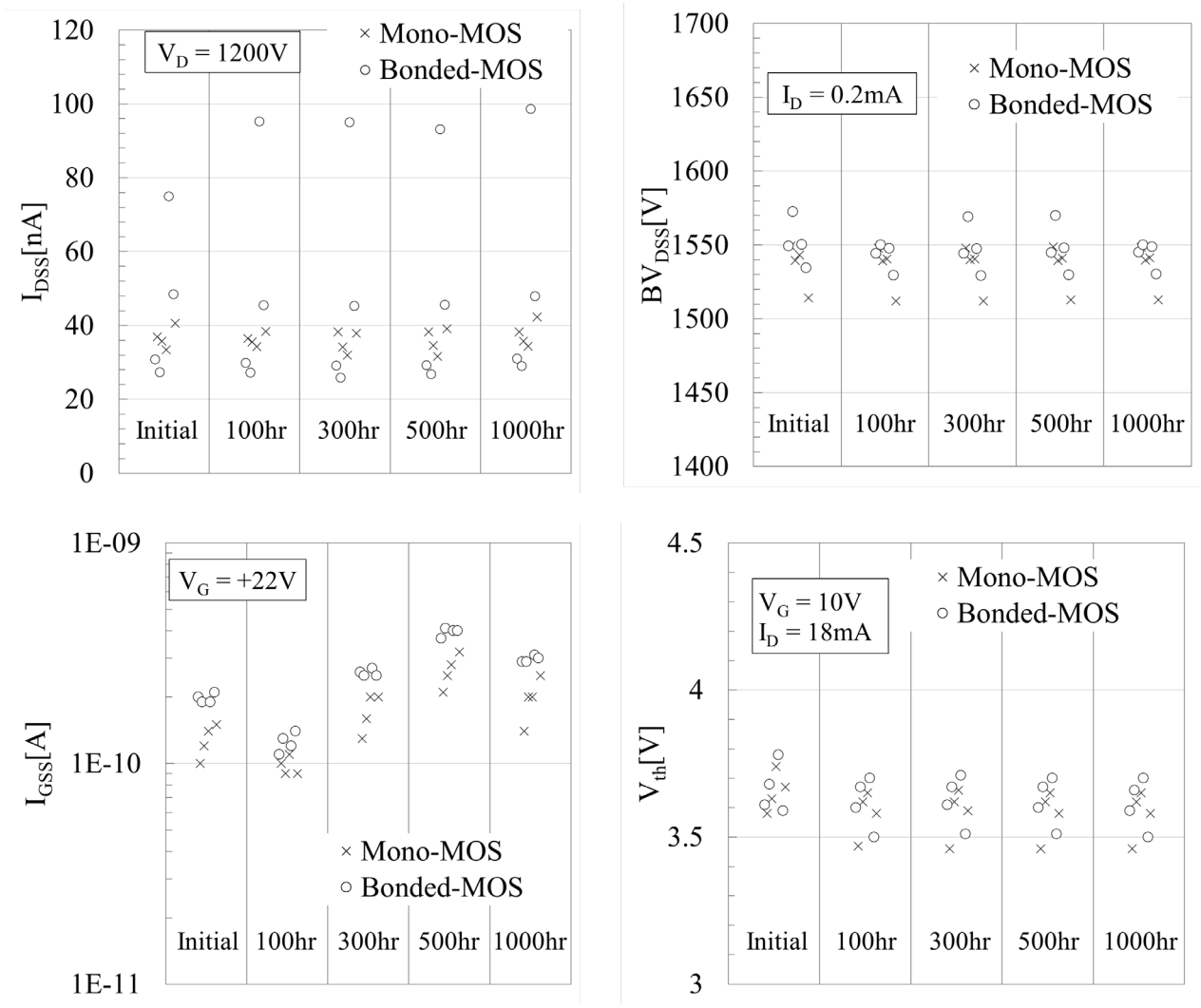

Fig. 11 Characteristic values (I_{DSS}, BV, I_{GSS}, V_{th}) after HTRB testing

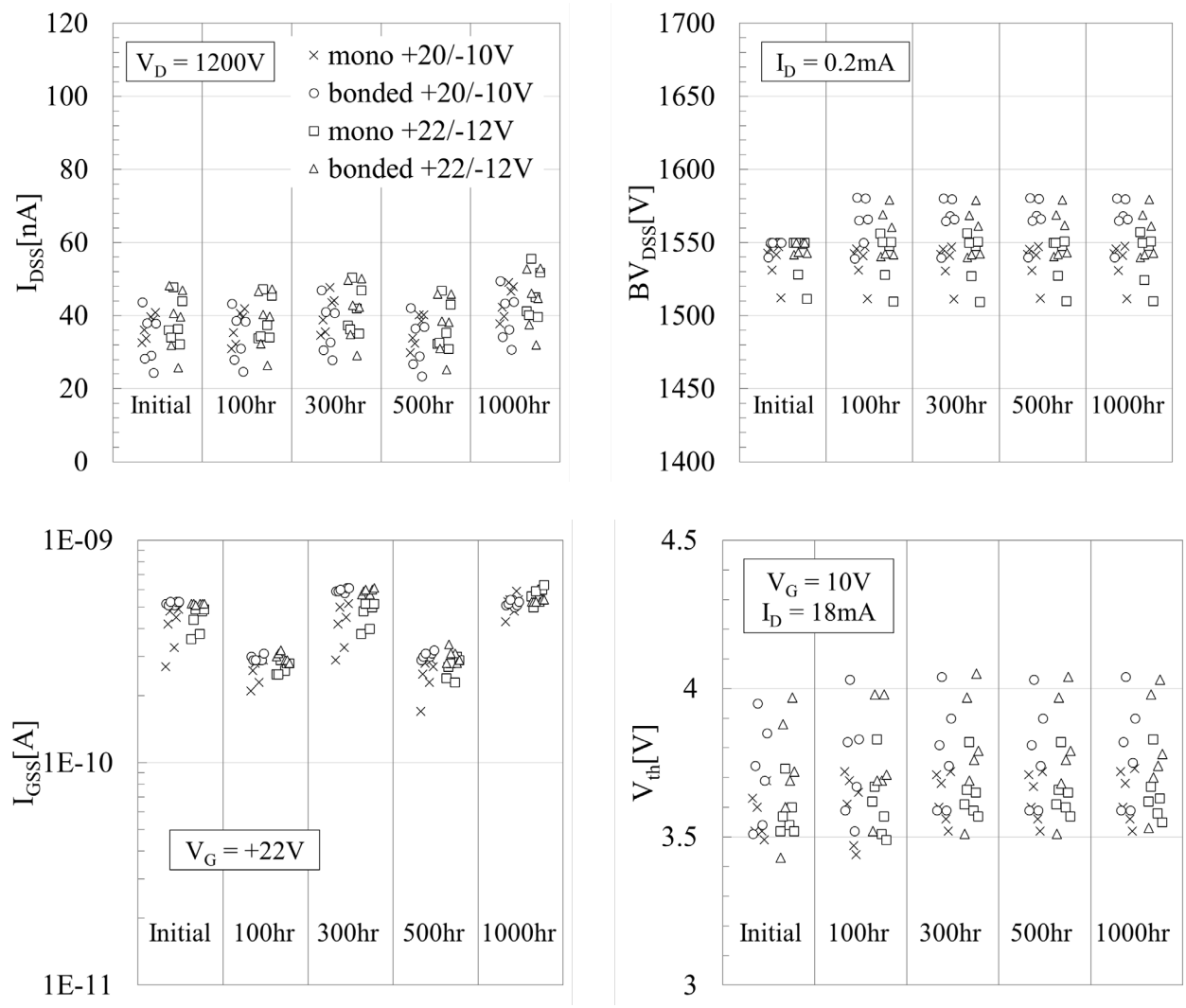

Fig. 12 Characteristic values (I_{DSS}, BV, I_{GSS}, V_{th}) after burn-in testing

Conclusion

In this study, we have reported, for the first time, the superior characteristics of a DMOSFET fabricated on a 4H-SiC bonded substrate. The bonded-MOS had clearly lower on-resistance than the mono-MOS because of the low resistivity of the polycrystalline substrate even though there were no difference in blocking voltage. On the other hand, the body diode in the bonded-MOS exhibited a higher V_F and lower I_{RR} than that in the mono-MOS at high temperature. By the forward-current stress testing, the ΔV_F increased with increased current stress in mono-MOS, and its SSFs significantly expanded over the entire area, whereas the ΔV_F remained unchanged and no SSFs were observed in the bonded-MOS. Such superior characteristics of the body diode were due to the decreased carrier lifetime in both drift layer and transfer layer on the bonded substrate. Additionally, high-temperature reliability of bonded-MOS was the same as that of Mono-MOS. These results indicated that the bonded substrate has the potential to solve several issues of DMOSFETs fabricated on monocrystalline 4H-SiC substrates.

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