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1200 V 4H-SiC VDMOSFET Having >2.5x On-Current Improvement

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Abstract. We experimentally demonstrated >2.5x on-current improvement on VDMOSFET fabricated in a standard 1200 V-rated 4H-SiC based VDMOSFET. The on-current improvement is achieved by applying a positive bias to the p-well region when the VDMOSFET is in the on-state. A $>10^4$ ratio between the on-current gain and the p-well current gain is shown. TCAD simulations are performed to study the underlying mechanisms of the on-current gain.

Introduction

SiC has been increasingly used in high-voltage, high-power applications due to its high critical electric field. Improvements in the on-current and specific on-resistance are continuously being sought after through various methods, such as process optimizations [1-3], cell topologies [4], and charge modulations [5]. In this work, we experimentally demonstrated >2.5x on-current improvement on 1200 V-rated 4H-SiC based VDMOSFET.

Fig. 1(a) illustrates a schematic cross-sectional view of our device, which is fabricated in a standard 1.2 kV 4H-SiC process. A breakdown voltage of 1500 V is obtained as shown in Fig. 1(b). Typical aluminum and nitrogen implants were used for p+/JTE/p-well and n+/JFET, respectively. These implants were activated by a high temperature annealing with a carbon cap layer. Gate dielectric was fabricated, including passivation of interface and oxide traps. The front ohmic contacts to n+/p+ were enabled via a self-aligned nickel silicidation. A power metal stack, consisting of Ti/Al/Cu, was used to form metallization. For the ohmic back contact, the deposited metal was laser annealed to form an ohmic contact followed by a solderable back metal stack.

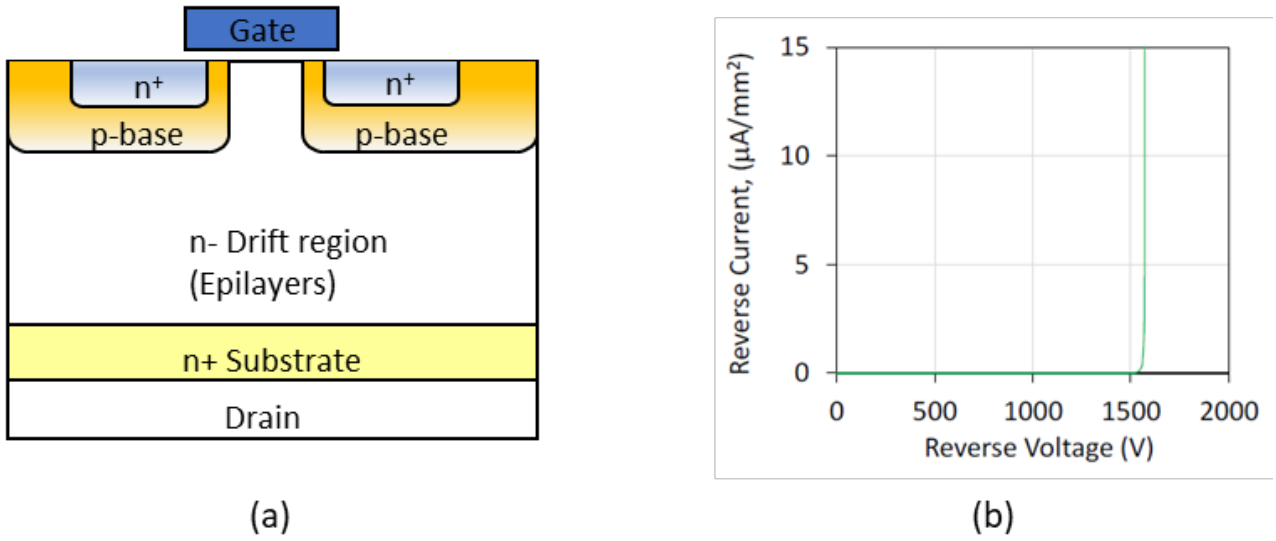

Fig. 1.(a) Cross-sectional view of the 1.2 kV VDMOSFET device structure **(b)** Breakdown characteristic of typical 1.2 kV device

Results and Discussion

In this work, separate contacts are formed for the p-well and source regions, allowing for independent biasing of the p-well and source regions. A positive bias is applied to the p-well region when the VDMOSFET is in the on-state and is removed when the VDMOSFET is in the off-state. In a conventional VDMOSFET, the p-well and source regions are shorted and typically connected to a common ground.

Fig. 2(a) shows the transfer curves measured from a test structure having a JFET width of 15 μm with different voltage applied to the p-well region for different Vds. The ratio of the VDMOSFET drain current with Vp=2.5V and Vp=0V applied to the p-well region for a range of applied gate voltage is shown in Fig. 2(b). As shown in Figs. 2, the drain on-current with a positive bias Vp=2.5V applied to the p-well region is 2.5x higher than a conventional VDMOSFET (with Vp=0V applied to the p-well region). The ratio of the drain on-current as a function of applied Vp bias is also shown in Fig. 2(c), indicating that the amount of current flow across the VDMOSFET can be controlled by both gate voltage Vg and p-well bias Vp.

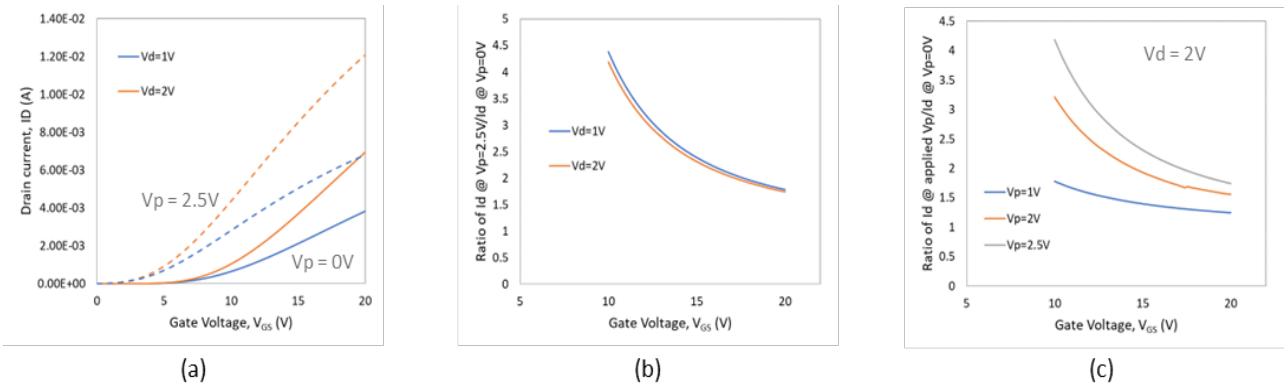

Fig. 2. (a) Transfer curve of VDMOSFET for Vd=1V and 2V with Vp=0V (solid) and Vp=2.5V (dashed) **(b)** Ratio of drain current with Vp=2.5V and Vp=0V applied, demonstrating the on-current gain with Vp=2.5V applied **(c)** Ratio of drain current at different applied Vp and Vp=0V for Vd=2V.

Fig. 3(a) shows the associated p-well current, demonstrating that the large on-current gain does not require large p-well current. The ratio between on-current gain to the p-well current can be calculated to be $>10^4$ and is shown in Fig. 3(b). Fig. 4 shows the corresponding transconductance (gm) curves. As the results show, both threshold voltage (Vth) shift and gm increase contribute to the on-current gain. When the VDMOSFET is turned off, the positive bias is removed and the off-state characteristics, including Vth, return to that with Vp=0V applied.

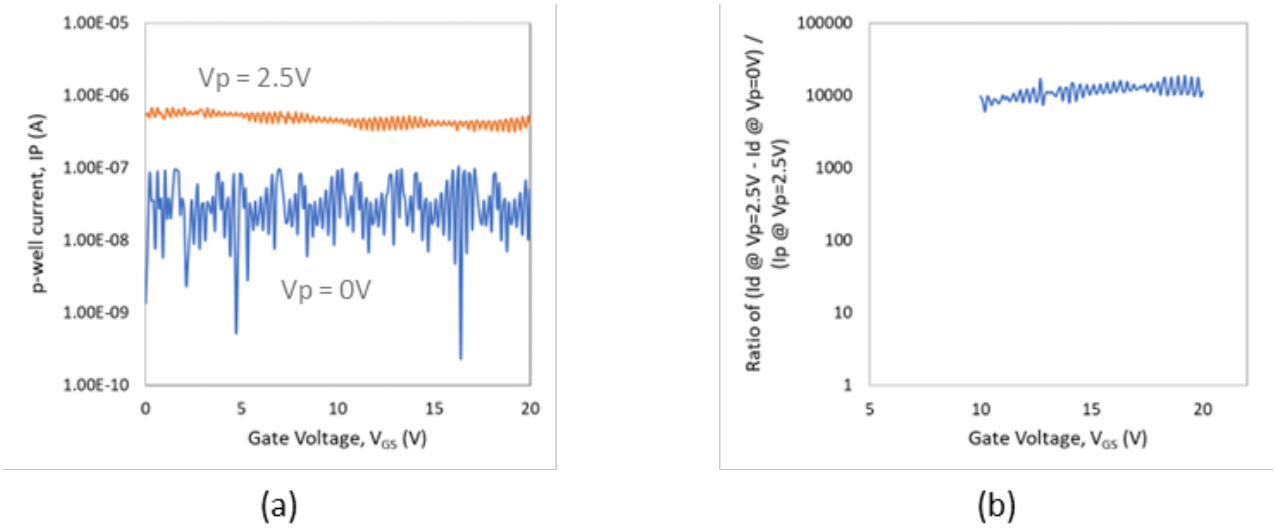

Fig. 3. (a) p-well current of VDMOSFET for Vd=2V with different applied Vp **(b)** Ratio of on-current gain (the difference between drain current with Vp=2.5V and Vp=0V) and p-well current for Vd=2V.

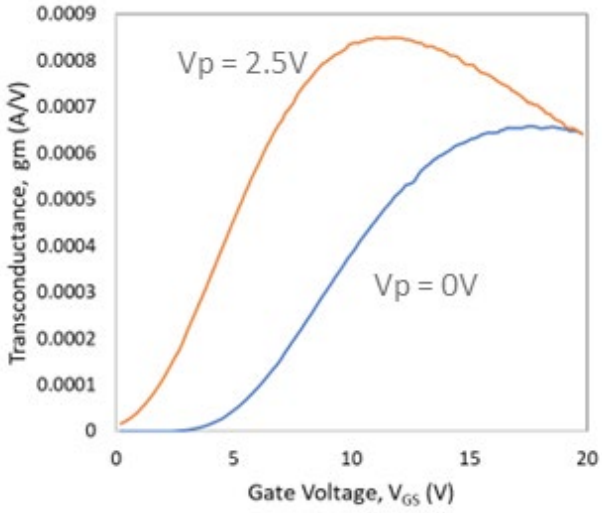

Fig. 4. Transconductance (gm) curves of VDMOSFET for Vd=2V with different applied Vp.

TCAD simulations are performed to study the underlying mechanisms of the drain on-current gain. The TCAD simulations are first calibrated to match the experimental results for the Vp=0V condition. When a positive bias Vp=2.5V is applied in the TCAD simulations, it similarly shows the on-current gain observed in experiments. Fig. 5 illustrates a comparison of the transfer curve from the TCAD simulations and the measurement results.

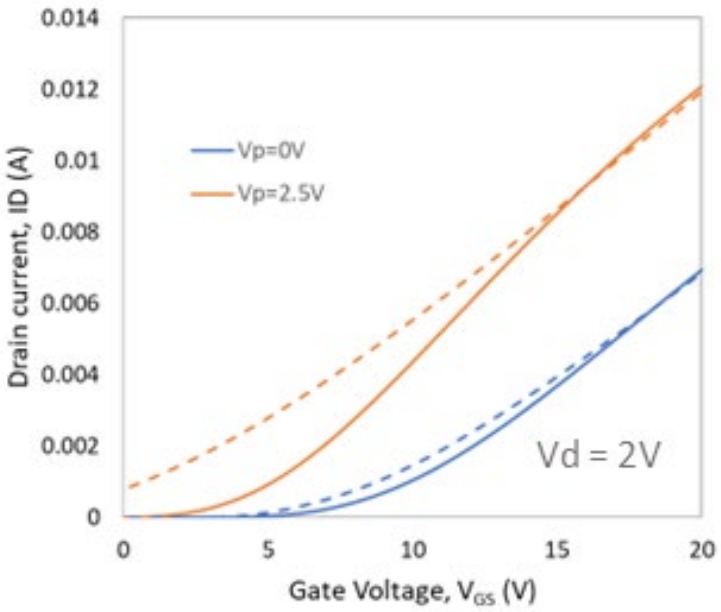

Fig. 5. Comparison of measured (solid) and TCAD simulation (dashed) results of VDMOSFET transfer curve for Vd=2V with different applied Vp.

Fig. 6 shows the current density of the VDMOSFET with Vp=0V and Vp=2.5V, respectively. When a positive bias Vp=2.5V is applied, the conduction area encompasses the source junction area and no longer limited to the area of the channel region. The additional conduction paths are not limited by the channel mobility, as can be seen from the higher transconductance in Fig. 4.

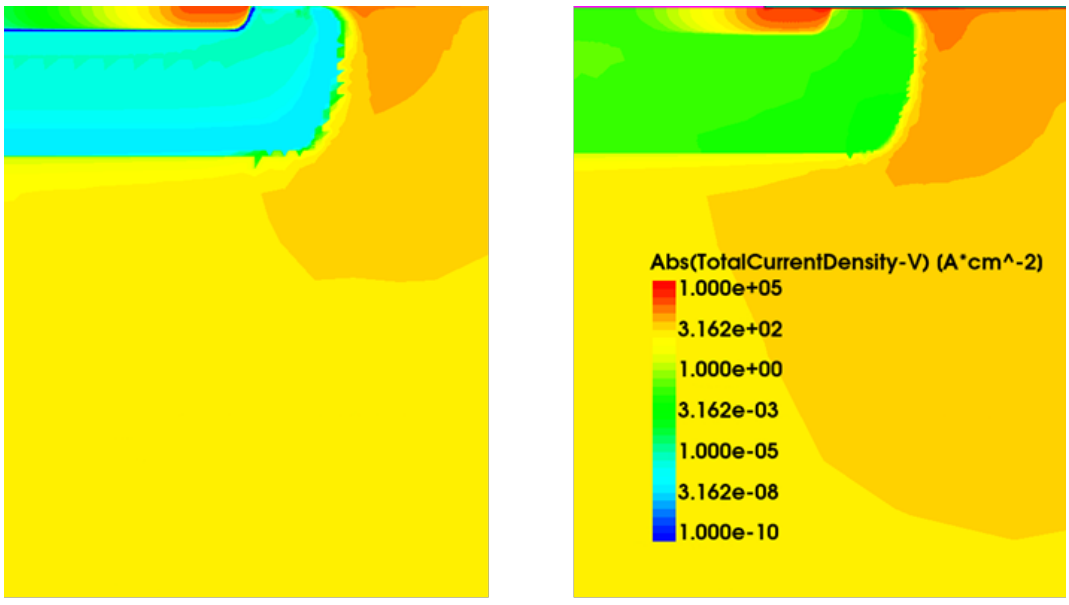

Fig. 6. TCAD analysis of total current density with **(a)** Vp=0V and **(b)** Vp=2.5V.

The improvement in the current flow due to increased conduction area can reduce temperature rise due to current crowding. Therefore, although a higher current density is achieved with positive Vp bias, the short circuit capability is not expected to degrade. The additional current path through the source junction region may be considered as bipolar junction transistor (BJT) current. As previously reported, BJTs typically exhibit better short-circuit capability than MOSFETs. [6, 7]

Further process improvements on the conventional SiC VDMOSFET and JFET width optimization have resulted in lowering on-state resistance Rds,on to 3 mΩ.cm^2 (Fig. 7). Using the p-well biasing technique described in this work, low Rds,on of 1.2 mΩ.cm^2 can be achieved.

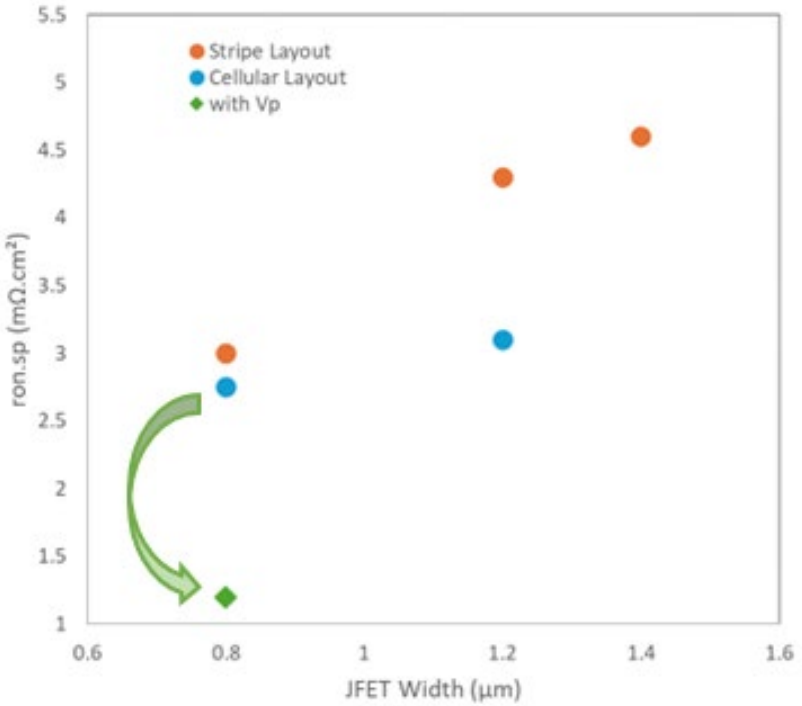

Fig. 7. Specific on-resistance for different JFET width and layouts.

Summary

The experimental results presented in this study highlight a significant advancement in the performance of 1200 V-rated 4H-SiC VDMOSFETs through the application of a positive bias to the p-well region. This technique led to more than a 2.5x improvement in on-current while maintaining a low p-well current, with a remarkable >10^4 ratio between on-current gain and p-well current. The TCAD simulations provided insights into the mechanisms responsible for this improvement, illustrating the expansion of the conduction area beyond the channel region when a positive bias was applied, thereby reducing the impact of channel mobility limitations. Additionally, the results showed that this technique could reduce the specific on-resistance to 1.2 mΩ.cm², a substantial improvement over conventional device. These findings underscore the potential of p-well biasing as a critical method for enhancing the performance of SiC-based power devices. Further research and process optimizations, for example in JFET width optimization and other design aspects, could unlock even greater performance gains, advancing the efficiency and capability of SiC devices in high-power applications.

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