Key Engineering Materials
ISSN: 1662-9795, Vol. 1021, pp 75-83
doi:10.4028/p-NJz1qy

Submitted: 2024-09-20
Revised: 2025-08-05
Accepted: 2025-08-05
Online: 2025-09-05

Static Analysis of Temperature-Dependence of Paralleled High Voltage Vertical Silicon & SiC NPN BJTs

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Keywords: Bipolar Junction Transistor, Static Performance, Vertical Devices, Temperature

Abstract. This paper compares the static properties for Silicon & SiC BJTs when connected in parallel, under various operating temperatures at various base currents and collector currents. This includes analysis of forward I-V characteristics, on-state resistance, DC gain, forward transfer characteristics and reverse leakage current to provide insights on paralleling of SiC & SiC BJTs.

Introduction

For power applications with voltage requirements lower than 1700 V, SiC BJT can compete with SiC MOSFET because of the absence of gate oxide which could potentially have defects and charge traps [1, 2] as well as its close static and dynamic power dissipation performance [3, 4]. Challenges in fabrication of bipolar power devices are carrier lifetime in conductivity modulation and reverse recovery, bipolar degradation and avalanche ruggedness [5]. Key interests are on static and dynamic performance and electrothermal ruggedness at larger on-state currents and elevated temperatures.

Experimental Set-Up

This paper characterizes the static properties for two-paralleled SiC power BJTs GA04JT17-247 and compare with the similarly rated Silicon BJTs FJL6920 by means of extensive experiments. To conduct experiments, a B2902A Source/Measure Unit (SMU) is directly connected to either power Silicon or SiC BJTs through high-temperature test leads as shown in the Fig. 1. To connect in parallel, two discrete BJTs are directly connected to each other via their leads for minimal parasitic resistance and parasitic inductance. BJTs are placed in a TAS LTCL600 climatic test chamber, as also shown in Fig. 1 to adjust the operating temperature from -50°C to 150°C in steps of 25 degrees.

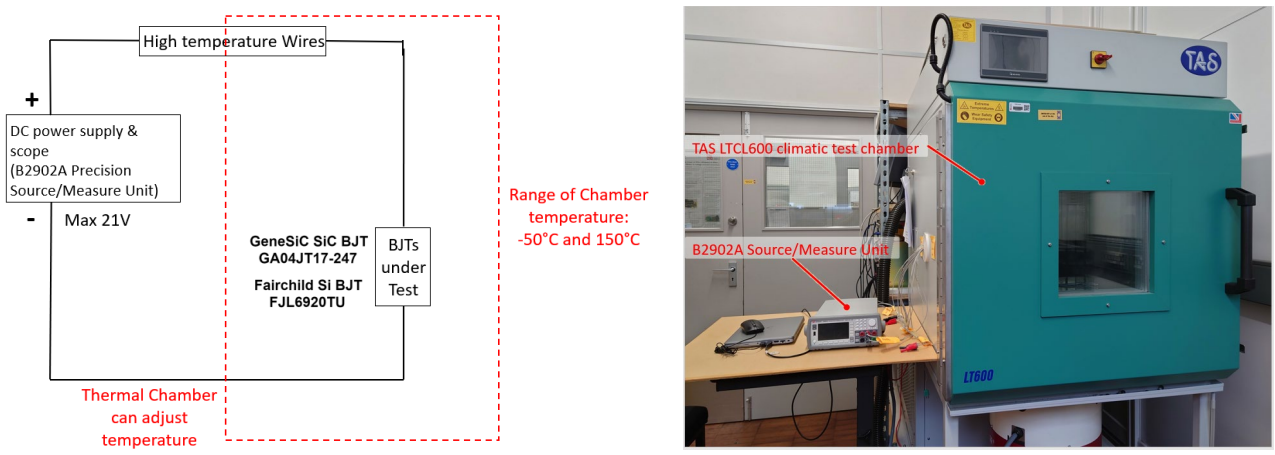

Fig. 1. Schematic and view of the experimental rig for static measurements of power BJTs.

Output Characteristics

To characterize the forward output characteristic, the Collector-Emitter current (I_{CE}) is measured while sweeping the Collector-Emitter voltage (V_{CE}) from 0 to 4 V in 0.04 V increments, with the fixed Base-Emitter current (I_{BE}) of 10 mA, 20 mA and 30 mA used in each set of measurements between -50°C to 150°C. This setting is chosen to ensure the safe operation of both Silicon and SiC BJTs because of the low current rating of SiC BJT at high temperatures while enabling fair comparison between performance of the two devices both in single and paralleled configurations.

In terms of paralleled BJTs, the maximum V_{CE} was set to 1 V from the SMU since the sweeping of V_{CE} cannot continue at higher voltages. Fig. 2 show the output characteristics of the two-paralleled Silicon BJTs under various chamber temperatures. Under such low Collector-Emitter voltages, the increase of collector current with increasing temperature is associated with the increased stored charge in the drift region. This is because with increase of temperature additional carriers will be released intrinsically to contribute to the current conduction while the carrier lifetime also increases [6-8]. The mobility is reduced with temperature, however, the impact of the two aforementioned parameters is more pronounced in increasing the Collector-Emitter current. This in turn leads to increase of the DC gain (β) with temperature in the Silicon BJT.

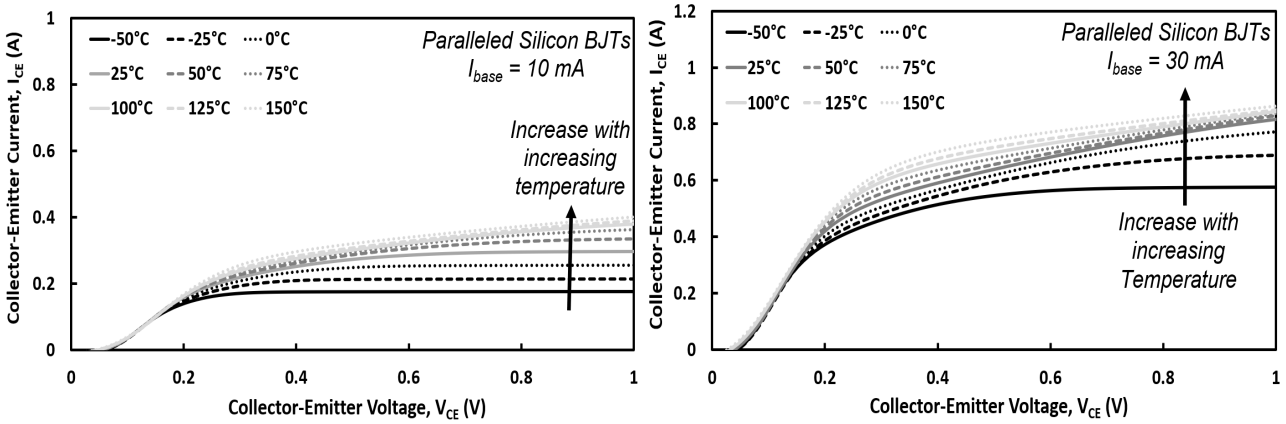

Fig. 2. Forward I-V characteristics for paralleled Silicon BJTs at I_{Base} of 10 mA and 30 mA under different temperatures.

The comparison between the I-V curves of single Silicon BJT and paralleled Silicon BJTs can be found in Fig. 3. When parallel BJTs are conducting a current, the slight difference in device parameters, namely, the on-state resistance of the Base-Emitter region, can cause current mismatch where the low resistivity one carries more base current and thus more collector current. At high base currents, the base current imbalance between paralleled becomes worse. At high chamber temperatures, the higher current device is prone to higher junction temperatures and attracts more current since it is more difficult to extract heat. Both conditions produce a huge difference in collector current between two devices together with a huge difference in Collector-Emitter conduction resistance. Such current imbalance can lead to the smaller on-state resistance of paralleled Silicon BJTs than that of single BJT and thus the larger collector current as can be seen in Fig. 3.

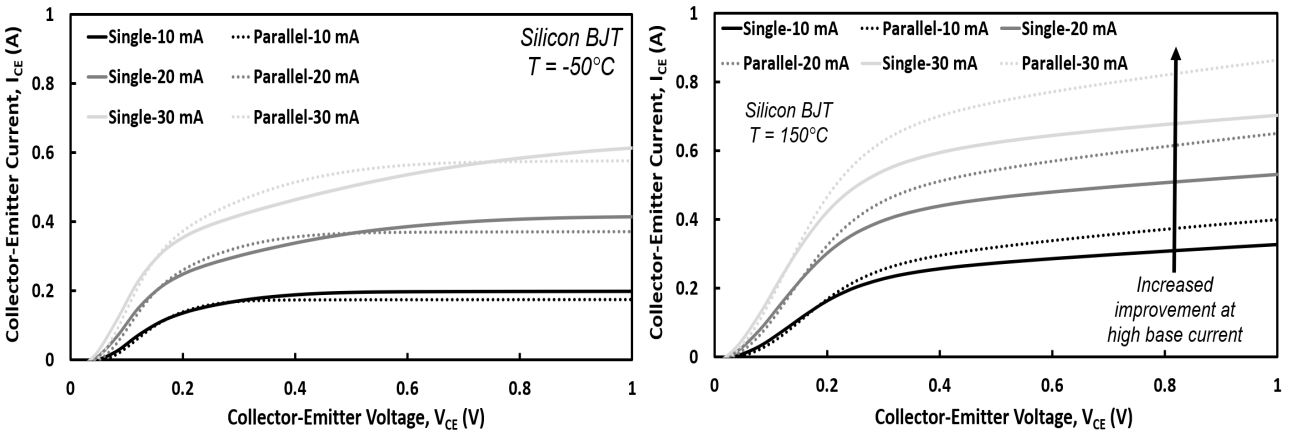

Fig. 3. I-V characteristics for paralleled Silicon BJTs at different base currents at -50°C & +150°C.

For paralleled SiC BJTs as shown in Fig. 4, the decrease of collector current is also observed because of the significant incomplete ionization of acceptors at room temperature in the base region. This in turn leads to the surge of hole concentration at high temperatures and reduces the current gain. The incomplete sweep of Collector-Emitter voltage is due to the current reaches the SMU's limit.

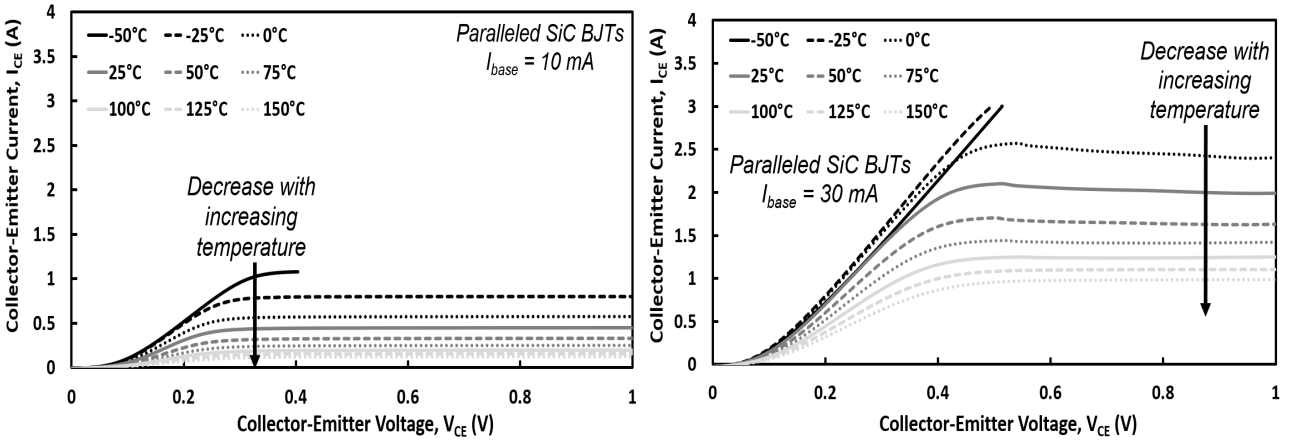

Fig. 4. Forward I-V of parallel SiC BJTs at I_{Base} of 10 mA and 30 mA by temperature.

Unlike the paralleled Silicon BJTs, the current gain in paralleled SiC BJTs reduces compared to its single device, as observed in Fig. 5. This is due to the fact the two devices are sharing the same base current supplied by a single base driver, and at lower base current the Collector-Emitter current drops more than expected due to reduced injection efficiency.

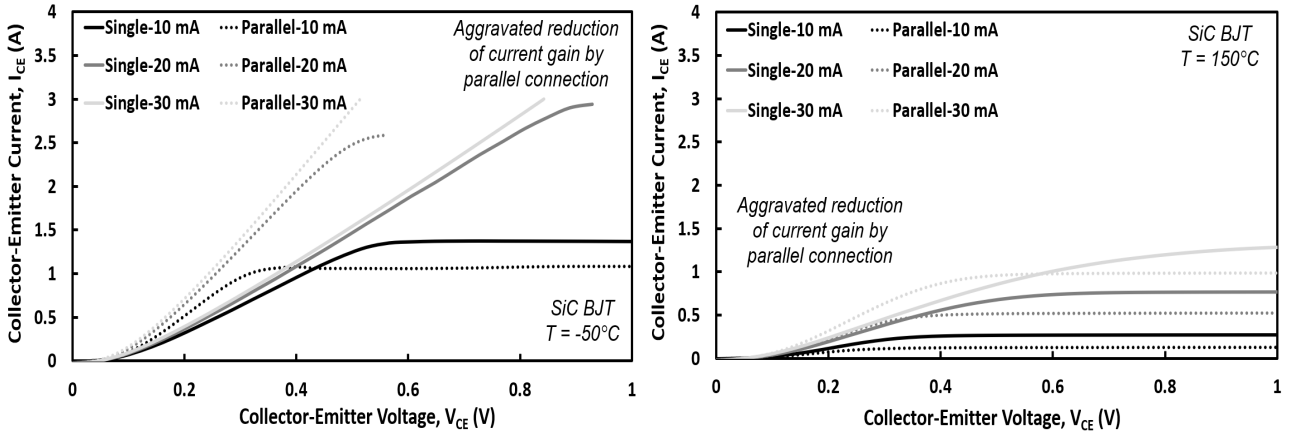

Fig. 5. Comparison of I-V characteristics for the single and paralleled SiC BJTs at different base currents under -50°C and +150°C.

The instability problem of current gain in SiC BJT becomes worse when in parallel connection as the reduction of Emitter efficiency can occur in both SiC devices, where the difference of current gain between paralleled Silicon BJTs and paralleled SiC BJTs is about 28 at 1 V as shown in Fig. 6 while the current gain gap is approximately equal to 20.5 at 4 V. It must be noted that in the case of the paralleled device the base current is supplied by the same base driver and shared between the two paralleled devices, further reducing the base current supplied per device which as expected has led to further reduction of the DC current gain in the SiC.

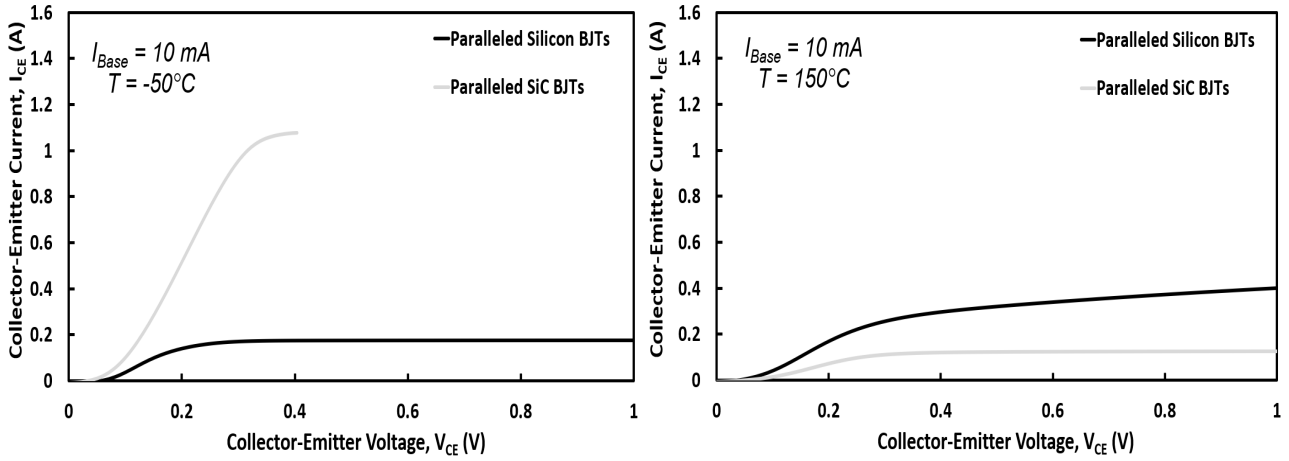

Fig. 6. I-V characteristics of paralleled Silicon and SiC BJTs at I_{Base} of 10 mA at -50°C & +150°C.

Static DC Current Gain

In terms of current gain for paralleled devices as observed in Fig. 7, the current gain of paralleled Silicon BJT is slightly lower than that of single BJT under low temperatures but higher current gain under high temperatures. This is because the improvement in current gain becomes evident at high temperatures. In contrast, the paralleled SiC BJTs lead to the lower current gain.

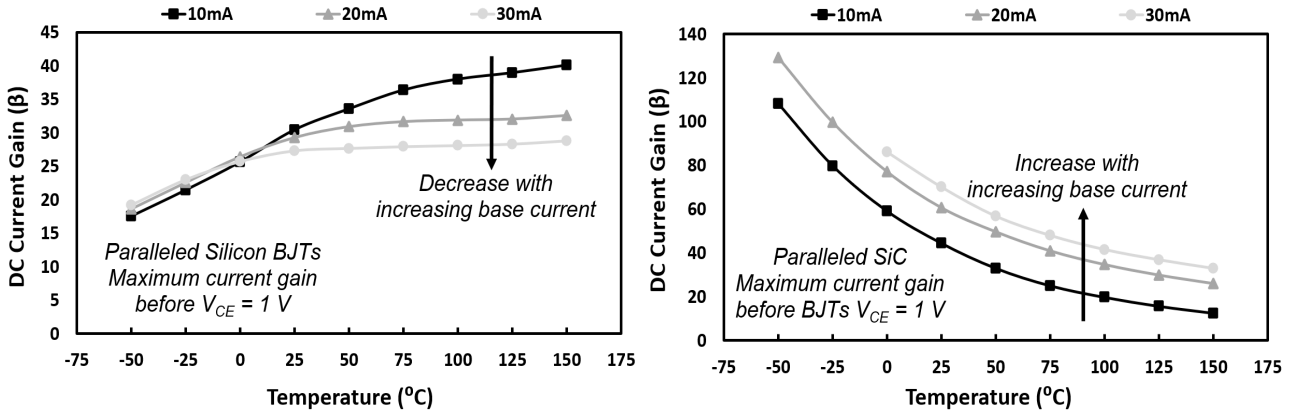

Fig. 7. Common-Emitter current gain for Paralleled Silicon BJTs and SiC BJTs.

On-State Resistance

Fig. 8 shows the on-resistance of two-paralleled Silicon BJTs under various temperatures at different collector currents. The parallel connection leads to reduction of on-resistance compared with Single Silicon BJT. A turn-around of measurements is seen in Silicon BJTs where the resistance first slightly increases with temperature between -50°C to 0°C at low base current and then drops with further increase of temperature. This is because at low base current and low temperature the impact of additional carrier generation by temperature is critical, however, as the temperature rises the role of reduced lifetime and mobility by scattering between carriers becomes more effective.

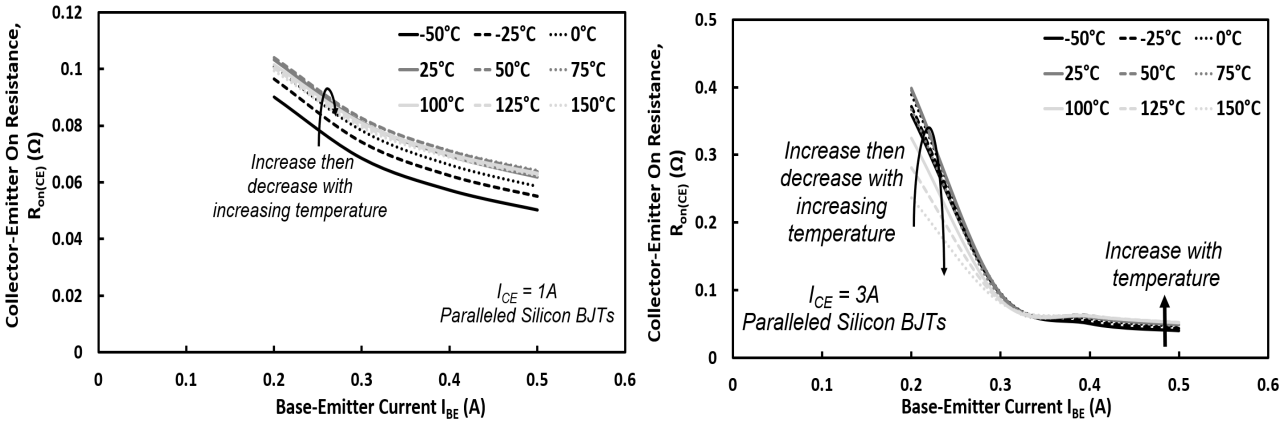

Fig. 8. On-state resistance for paralleled Silicon BJTs at I_{CE} of 1 A & 3 A in different temperatures.

Fig. 9 shows the on-resistance of two-paralleled SiC BJTs under various temperatures at different collector currents. Parallel connection of SiC BJTs can reduce the on-resistance when compared with Single SiC BJTs. This is more pronounced in comparison with single Silicon BJT at low base current. Parallel-connected SiC BJTs introduce the stronger negative temperature dependence of on-resistance, albeit it occurs only at low temperatures ranging from -50°C to 0°C.

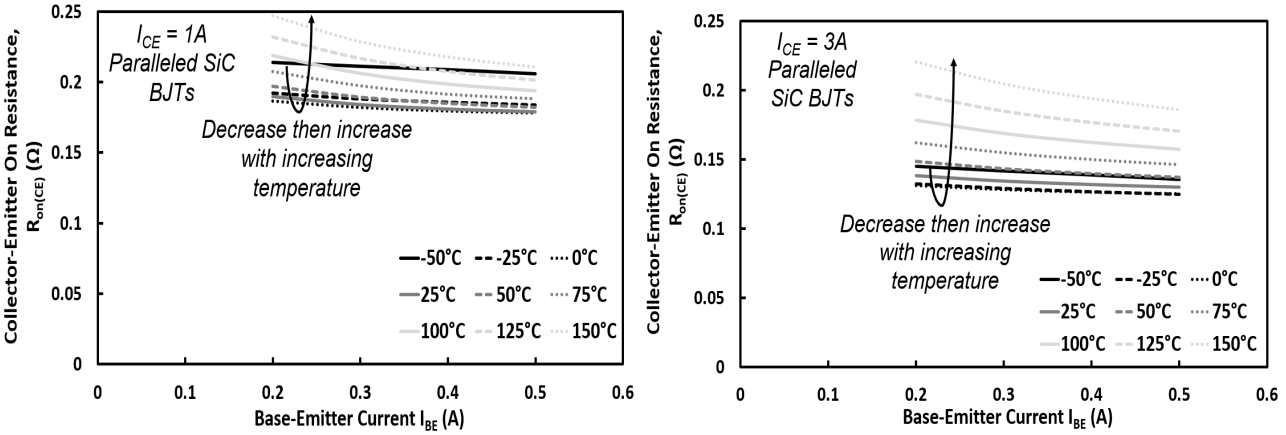

Fig. 9. On-state resistance for paralleled SiC BJTs at I_{CE} of 1 A and 3 A in different temperatures.

The turn-around seen is similar to the Silicon BJT, where at low base current and low temperature the impact of additional carrier generation by temperature becomes more critical, though with the rise of temperature the role of reduced lifetime and mobility by scattering becomes more effective. The on-resistance of paralleled Silicon BJT is found to be smaller than that of paralleled SiC BJTs at a collector current of 1 A. The decrease of on-resistance with base current for paralleled Silicon BJTs, as shown in Fig. 10, indicates the gradual transition between the active mode and the quasi-saturation mode of operation. In general, parallel connection can promote the conductivity of both Silicon and SiC BJTs especially at elevated temperatures and at low base currents, where the on-resistance of single Silicon BJT at I_{base} of 0.2 A under 150°C is reduced by 1.36 Ω when connected in parallel. In essence, the same trends seen for a single SiC BJT can be observed for the paralleled devices too, with the caveat that the base current is divided between two devices, leading to higher resistance per device and there is a slight decreasing trend with the base current.

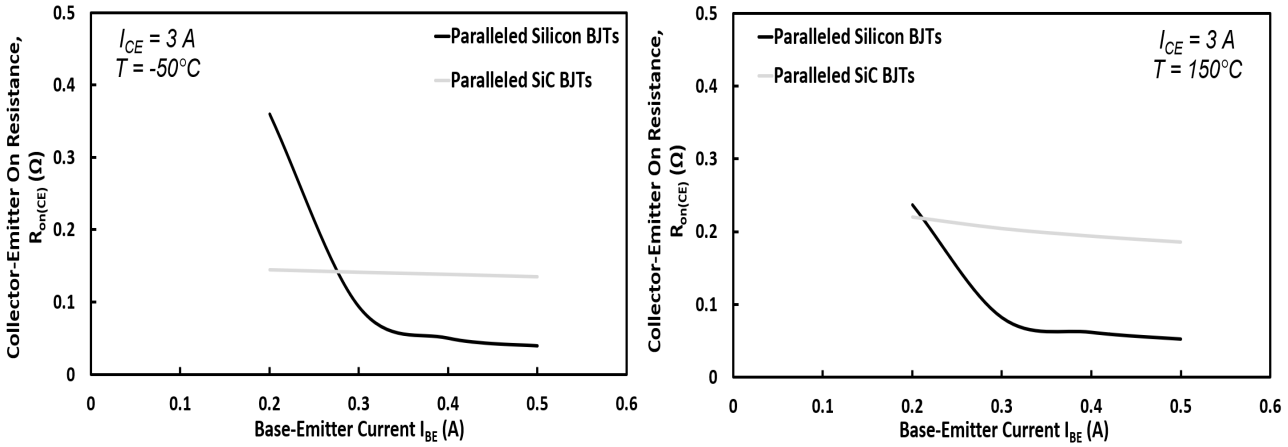

Fig. 10. Comparison of the on-state resistance of paralleled Silicon and SiC BJTs at I_C of 3 A under -50°C and +150°C.

Forward Transfer Characteristics

To characterize the forward transfer characteristic, the Collector-Emitter current (I_{CE}) is measured while sweeping the Base-Emitter voltage (V_{BE}) from 0 to 4 V in 0.05 V increment while fixed Collector-Emitter voltage (V_{CE}) of 0.3 V is used. The temperature is increased from -50°C to 150°C and the forward characteristics are measured and plotted. Fig. 11 and Fig. 12 show the transfer characteristic measured for the Silicon BJT and SiC BJT under various chamber temperatures for paralleled devices. Both Silicon and SiC devices exhibit a lower built-in voltage at high temperatures since the intrinsic carrier concentration increases with temperature, while the temperature increase from -50°C to 150°C reduces the Base-Emitter voltage by 0.4 V in both cases of Silicon and SiC devices, though this has a more pronounced impact on the Silicon device due to its low base voltage.

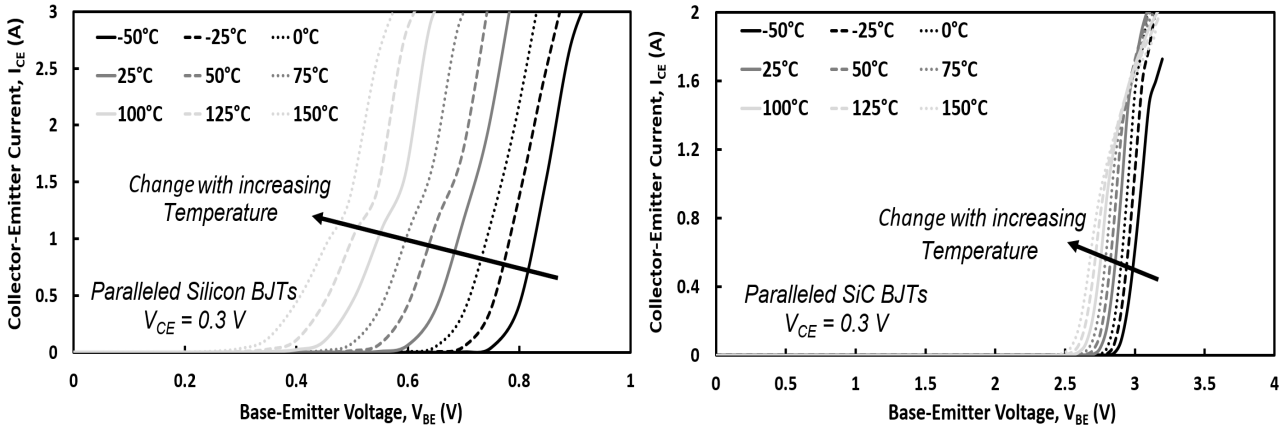

Fig. 11. Forward transfer characteristics of paralleled Silicon & SiC BJTs in different temperatures.

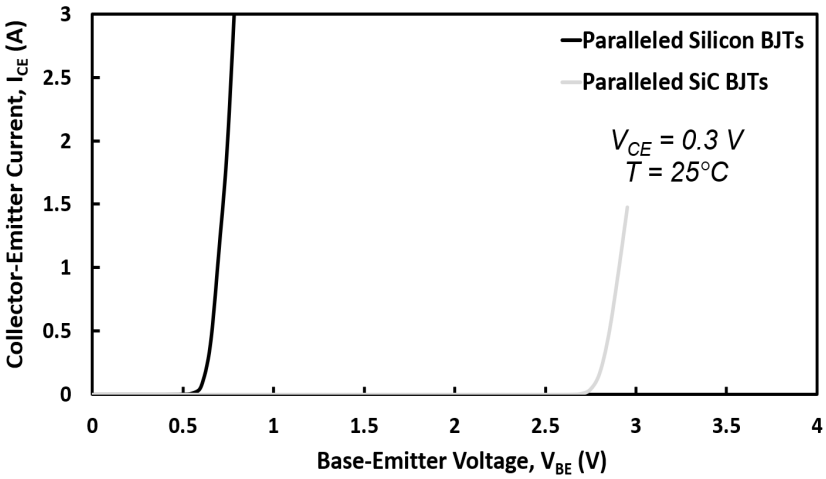

Fig. 12. Transfer characteristics of Silicon vs. SiC BJTs in paralleled connection.

Reverse Base-Emitter Leakage Current

To determine the voltage blocking capability of the Base-Emitter junction, the reverse Base-Emitter current (I_{RBE}), which is also referred to as the Base-Emitter current (I_{EB}), is measured when sweeping the Base-Emitter voltage from 0 to 20 V in the negative direction. The collector terminal is open-circuited. The measurements are done between -50°C to 150°C for paralleled devices.

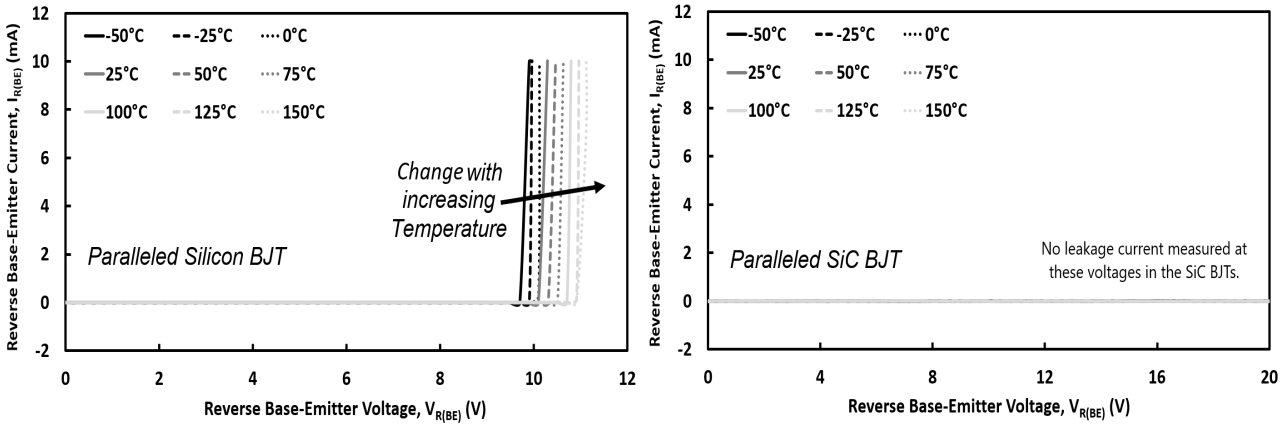

Fig. 13. Base-Emitter leakage current for paralleled Silicon and SiC BJTs in different temperatures.

Fig. 13 and Fig. 14 show the reverse Base-Emitter current of Silicon BJT and SiC BJT under various chamber temperatures for paralleled devices. The positive temperature dependence of the breakdown voltage of Silicon BJTs can be explained by the fact that the movement of free carriers is restricted by the collision with atoms at high temperatures [9, 10], which in turn generates less electron-hole pairs and thus less leakage current, noting that in Silicon almost all dopants are ionized in room temperature.

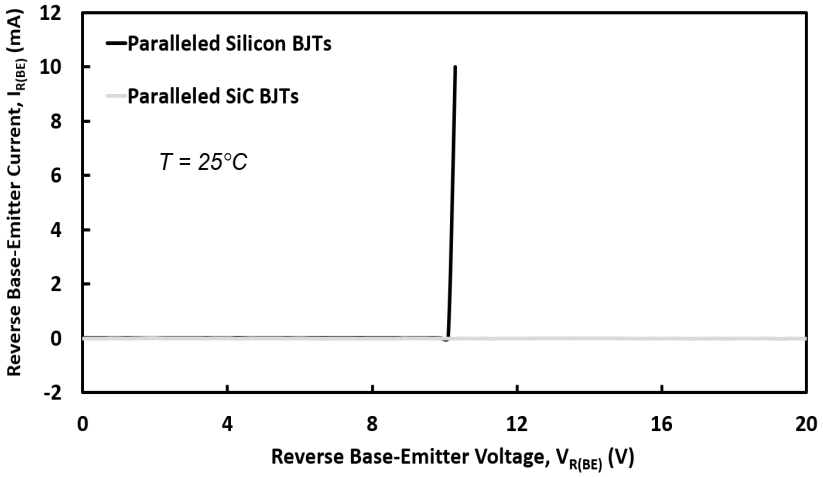

Fig. 14. Base-Emitter leakage current of Silicon vs. SiC BJTs in paralleled connection.

Applications

In applications, current imbalance between paralleled BJTs can lead to reliability problems. Minor differences in the thermoelectrical parameters of the individual devices always exists even if they are fabricated in the same batch. The low-resistance device in parallel connection attracts more current, becomes hotter, and conducts even more current if it exhibits a PTC for current gain (or NTC for on-resistance), while the cooler device conducts less [11]. Such positive feedback can result in thermal runaway until destruction. Here it is shown that the current gain of Silicon BJT has improved at high temperatures. Thanks to the parallel connection, the current gain and the conductivity of Silicon BJTs are further enhanced together with their temperature coefficient. However, SiC BJTs are favorable for long-term operation since the negative temperature coefficient counteracts the decrease of on-resistance with temperature and thus suppresses the current imbalance between parallel devices.

Summary

Parallel connection is found to promote both the conductivity and current gain for Silicon devices. This also leads to lower on-resistance in parallel SiC BJTs when compared with the single device whereas the current gain is reduced in parallel configuration. Nevertheless, SiC BJT may become preferable to be connected in parallel from the reliability point of view since the negative temperature dependence of on-resistance suppress the current imbalance and thermal runaway.

Acknowledgements

This research article is based on the PhD dissertation/thesis by Chengjun Shen submitted to the University of Bristol in the UK, with online access link to the thesis available on: https://research-information.bris.ac.uk/ws/files/383491217/Final_Copy_2023_12_05_Shen_C_PhD.pdf, validated by collaboration with the Compound Semiconductor Applications Catapult (CSAC) in Newport, UK, funded as part of the EPSRC Catapult Network's 'Innovation Launchpad Network+' program with grant EP/W037009/1 and partly funded by the UK EPSRC grant EP/Y000307/1.

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