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Economic Feasibility Analysis of Vertical High-Voltage 4H-SiC Superjunction MOSFETs Compared to Conventional Counterparts

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Abstract. Vertical high-voltage 4H-SiC superjunction (SJ) MOSFETs have emerged as a superior alternative compared to conventional SiC MOSFET or Si IGBT, as SJ MOSFETs present a better trade-off between specific on-resistance ($R_{ON,sp}$) and breakdown voltage (BV). The fabrication of SJ devices requires precise, and multi-step processes, such as multi-epitaxial growth, trench-refill processes, and MeV implantations [3,4,5]. However, these methods increase the overall costs of SJ devices compared to their conventional counterparts, potentially undermining their benefits. This paper compares the chip costs of SJ and conventional MOSFETs at a wide range of BV and current ratings, evaluating the economic feasibility of SJ MOSFETs in 4H-SiC. Our results highlight the potential improvements in SJ fabrication and design to enhance cost-effectiveness, particularly for medium-voltage applications (>3.3kV).

Introduction

In medium-voltage applications (>3.3kV), SiC MOSFETs (Fig. 1(a)) and Si IGBTs (Fig. 1(b)) are the main devices used. Despite their prevalence, these MOSFETs encounter issues such as high conduction losses in SiC MOSFETs due to the dominance of drift region resistance at these voltage ratings, and significant switching losses in Si IGBTs because of their bipolar nature. To address these challenges, vertical high-voltage 4H-SiC superjunction (SJ) MOSFETs (Fig. 1(c)) offer a better solution, enhancing both conduction and switching performance by reducing drift region resistance while maintaining a unipolar conduction. SJ devices provide a superior trade-off between specific on-resistance ($R_{ON,sp}$) and breakdown voltage (BV) ($R_{ON,sp} \propto BV^{1.1}$) compared to the traditional, uniformly doped vertical power devices ($R_{ON,sp} \propto BV^{2.296}$), as illustrated in Fig. 2 [1]. However, the complex and expensive fabrication processes of SJ devices could limit their adoption over conventional devices. Therefore, estimating the costs of SJ and traditional devices is crucial to assess the advantages of superjunction devices at specific breakdown voltage and current ratings.

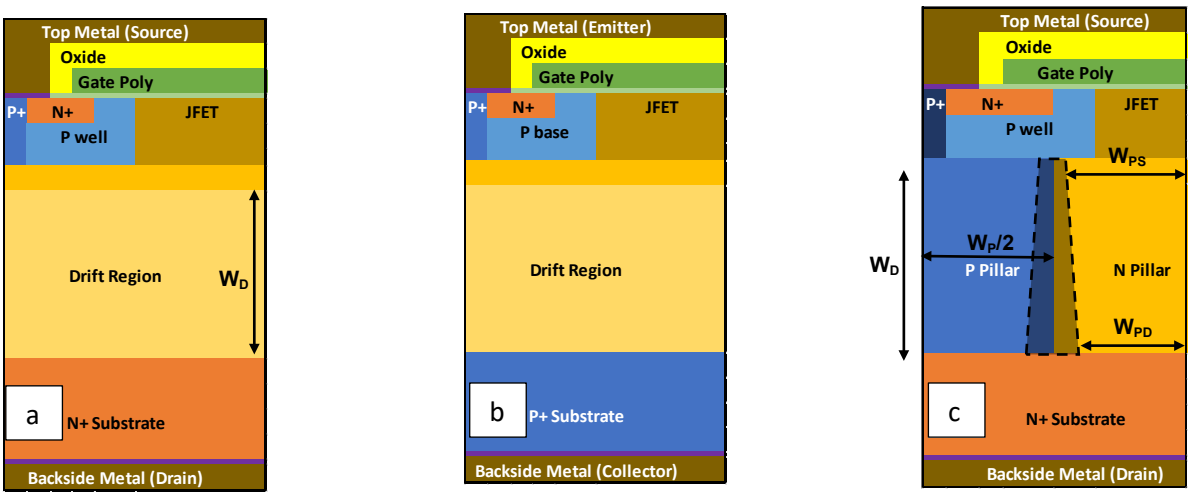

Fig.1. Schematic cross-section views of half unit cells of (a) conventional MOSFET, (b) IGBT and (c) SJ MOSFET.

Superjunction Theory

The key design of SJ devices is the alternating charge-balanced P and N pillars, where these pillars introduce a lateral electric field across their sidewalls to ensure a rectangular-like electric field profile along the vertical direction [2]. The lateral electric field is responsible for terminating the charges in the pillars laterally and deplete all the charges before breakdown occurs. Once the charges in the pillars are depleted laterally, the vertical electric field starts to develop uniformly. Only the thickness (W_D) of the pillars imposes the breakdown voltage capability of the device [2]. As shown in Fig. 2, decreasing the pillar width decreases the specific on-resistance offsets by enhancing the doping of the pillars to keep the pillar charge dose the same ($5\mu m$ and $1\mu m$ lines).

Unlike conventional devices, ideally, the doping in the superjunction devices does not alter the effective critical electric field or the breakdown voltage providing that the dose is not higher than the optimal value and the charges in the pillars are balanced. Consequently, it is important to design the pillars width and doping to ensure the best trade-off between $R_{ON,sp}$ and BV. Based on Gauss' law, the optimal pillar charge dose used here is 10^{13} cm^{-2} [2], ensuring an optimal $R_{ON,sp}$ without breakdown at the sidewalls of the pillars. Moreover, the drift region thickness of superjunction devices is shorter than that of conventional devices at the same breakdown voltage due to the rectangular-like electric field profile, reducing the overall resistance even further.

The fabrication of SJ devices necessitates precise processes involving multiple steps to ensure the desired charge-balanced pillars in terms of both doping and width, particularly for high voltage applications that require thicker pillars. Various techniques have been explored, including multi-epitaxial growth [3], trench-refill processes [4], and a series of MeV implantations and epi-growth processes [5]. However, these methods contribute significantly to the overall cost of SJ devices, potentially outweighing their benefits compared to conventional devices with similar breakdown voltage and current ratings.

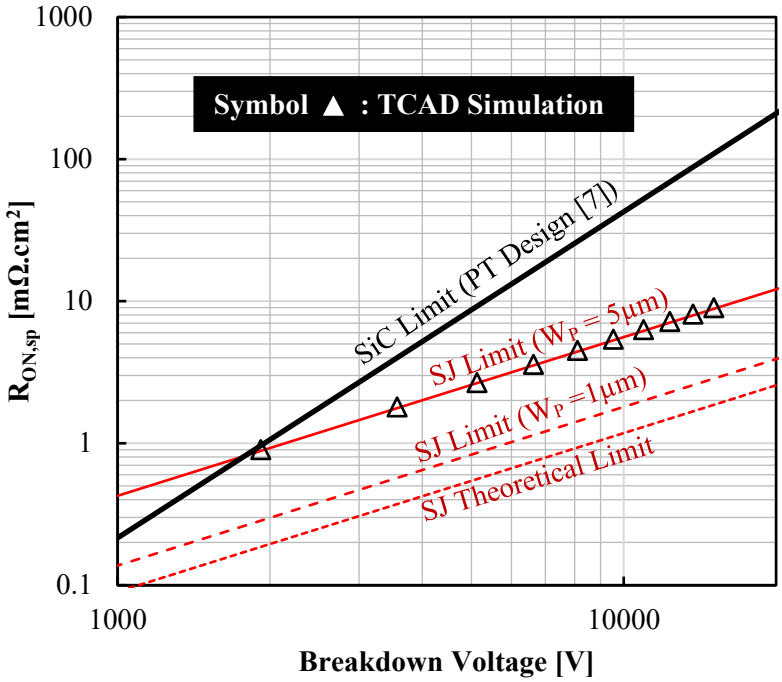

Fig.2. $R_{ON,sp}$ and breakdown voltage trade-off for conventional and superjunciton (SJ) devices with different SJ pillar widths.

Devices Modeling and Economic Analysis

We construct our cost model referring to GE's previous study [5], leveraging their scalable devices that exhibit less performance degradation. Instead of using multi-epitaxial growth or trench-refill processes, a 12μm epitaxial growth followed by MeV ion-implantation fabrication cycle can be employed. This reduces overall costs and mitigates process variation when compared to other methods. According to [6], only one fabrication cycle can yield a 12μm charge-balanced pillars resulting in breakdown voltage >2kV. We used a closed form set to calculate the performance parameters as a function of drift layer thickness for conventional MOSFETs developed by [7] assuming a punch through (PT) design which exhibits the best $R_{ON,sp}$ for a given BV compared to non-punch through (NPT) design. For SJ MOSFETs, we employed the simulation-based empirical formula developed by [8] for the blocking performance (BV). While for the conduction performance, we have used the JFET depletion approximation of the alternating pillars [9] as shown in Table 1 where ρ is the resistivity of the pillars, W_P is the pillar width, W_D is the pillar vertical thickness, W_{PS} is the pillar width at the source side and W_{PD} is the pillar width at the drain side. The JFET depletion is assumed to be linear from the source to the drain where the voltage at the source is zero and the drain is 1V. Additionally, we validate our static calculations through 2D Sentaurus TCAD simulations.

Table 1. Conventional and Superjunction MOSFETs design parameters [7,8,9]

Parameters	Conventional MOSFETs	Superjunction MOSFET
N_D [cm^{-3}]	$8.839\times10^{19}\ BV^{-1.234}$ [7]	$10^{13}/W_P$ [9]
W_D [μm]	$2.625\times10^{-3}\ BV^{1.117}$ [7]	$2.15\times10^{-3}\ BV^{1.1}$ * [8]
$R_{ON,sp}$ [Ω.cm^2]	$2.791\times10^{-11}\ BV^{2.296}$ [7]	$\frac{W_P}{\rho(W_{PS}-W_{PD})} ln\left(\frac{W_{PS}}{W_{PD}}\right) W_D$ [9]

* Extracted and calculated from [8]

To estimate the active area for both MOSFETs, we have used Eq. (1), which is a thermal-based analysis according to the maximum power handling capability of the device [10],

$$Active\ Area = \sqrt{\frac{I^2 \times k \times R_{ON,sp\_300K} \times \left(\frac{T_{j,max}}{300}\right)^{\alpha}}{T_{j,max} - T_c}} \qquad (1)$$

where I is the current rating of the device, k is the specific thermal resistance assumed to be 0.068 K·cm^2/W, R_{ON,sp_300K} is the specific on-resistance at room temperature, α is temperature coefficient assumed to be 1.8, $T_{j,max}$ is the maximum junction temperature and T_c is the case temperature assumed to be 425K and 300K respectively. The model in Eq (1) has been plotted and matched with 1.2kV SiC commercial MOSFETs for different current ratings [10]. The chip size is calculated by assuming a periphery of 10μm which is the P+ ring around the edges of the active area and an edge termination (ET) width of 5 times the drift layer thickness ($5\times W_D$) as depicted in Eq. (2).

$$Chip\ Size = \left(\sqrt{Active\ Area} + 2(10\mu m + 5 \times W_D)\right)^2 \qquad (2)$$

Since the active area is a function of $R_{ON,sp}$ with a square root dependence, and the edge termination width is a function of the drift region thickness, the total chip size is a function of BV as shown in Table 1. The active area is proportional to $\sqrt{R_{ON,sp}}$ which in turn is proportional to $\sqrt{BV^{2.296}}$

and $\sqrt{BV^{1.1}}$ for conventional and SJ MOSFETs respectively. Moreover, the edge termination width is a function of W_D which has the same BV dependence of $BV^{1.1}$ for both designs which means that the chip size due to the edge termination only has a dependence of $(BV^{1.1})^2$. For this reason, at lower BV where the active area dominates the total chip size, the active area of conventional MOSFETs is increasing with a higher rate than that of SJ MOSFETs. However, at a relatively higher BV where the edge termination of SJ starts to dominate the chip size, the chip size of SJ MOSFETs starts to increase by $(BV^{1.1})^2$ instead of $\sqrt{BV^{1.1}}$ increasing the rate of SJ chip density as depicted in Fig. 3. In this figure, SJ-to-conv. MOSFET chip density curve has an inflection point where the rate of increase of chip density starts to decrease. The SJ design in Fig. 3 has a pillar width of 5µm assuming 10A current rating.

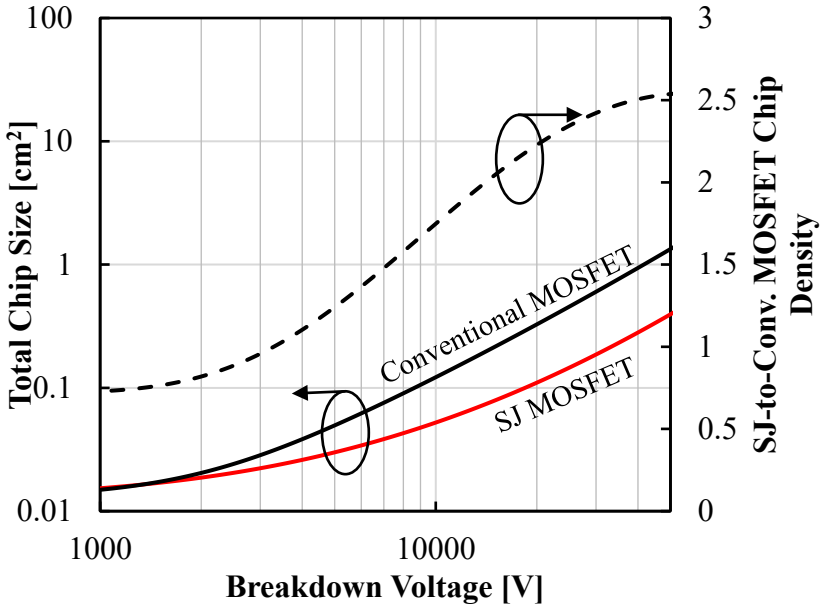

Fig. 3. Total chip size for conventional and superjunction MOSFET (left) and SJ-to-conventional MOSFET chip density assuming 10A current rating (right).

Based on the chip size of each MOSFET design, the price per chip is calculated using Eq. (3). For conventional MOSFETs, the substrate, epitaxial and fabrication costs are assumed to be $1000, a $50/µm and $1000, respectively. While SJ MOSFETs incur an additional cost of $500 and $2500 of an extra 12µm epi-growth operation and 12µm MeV ion implantation of both P and N pillars, respectively [4]. Table 2 illustrates all the cost and design assumption for both designs.

$$Chip\ Price = \left(\frac{Sub.cost + Epi.cost + Fab.cost}{\frac{Wafer\ size}{Chip\ size} \times Yield} \right) \times \frac{1}{Gross\ Margin} \tag{3}$$

Table 2. Cost Assumptions of Conventional and Superjunction MOSFETs

Assumptions	Conventional MOSFETs	Superjunction MOSFET
Substrate (Sub.) Cost	$1000	$1000
Epi Growth (Epi.) Cost	$50/$\mu$m	$50/$\mu$m + $500 per additional epi-growth
Fabrication (Fab.) Cost	$1000	$1000
MeV Ion Implant	NA	$2500 per run (12µm pillar) **(Variable)**
Wafer Size	6-inch	6-inch
Gross Margin	0.5	0.5
Yield	0.8	0.6 **(Variable)**
Pillar Width	NA	5 μm [4] **(Variable)**
Current Rating	10A **(Variable)**	10A **(Variable)**

Results and Discussion

We developed multiple cost scenarios and design approaches to evaluate the economic feasibility of 4H-SiC Superjunction (SJ) MOSFETs compared to conventional counterparts. The analysis covered three different fabrication cost scenarios (Cost #1, Cost #2, and Cost #3) and four chip design scenarios (Chip #1 to Chip #4) at varying breakdown voltage (BV) ratings, focusing on the crossover points where SJ MOSFETs become more cost-effective than conventional MOSFETs as illustrated in Table 3 and 4.

SJ Cost Scenarios: The baseline cost (Cost #1) assumes a fabrication cost of $3000 for implementing 12µm charge-balanced pillars, while Cost #2 and Cost #3 explore reduced fabrication costs of $2000 and $1000 per 12µm pillar, respectively.

SJ Chip Scenarios: The design scenarios varied pillar width and manufacturing yield. Chip #1 served as the baseline, with a 5µm pillar width and 60% yield, while Chip #2 reduced the pillar width to 1µm. Chip #3 increased yield to 80%, and Chip #4 combined the narrower pillar width and higher yield for optimal performance.

Table 3. Different cost scenarios for SJ MOSFETs

Scenarios	MeV Ion Implant plus Epi overgrowth (12µm-thick Pillars) ($) [4]
SJ Cost #1	**$3000 ($2500 implant + $500 epi overgrowth)**
SJ Cost #2	**$2000**
SJ Cost #3	**$1000**

Table 4. Different chip design scenarios for SJ MOSFETs

Scenarios	Pillar Width, W_P (µm)	Manufacturing Yield for SJ MOSFET
SJ Chip #1	5	0.6
SJ Chip #2	**1**	0.6
SJ Chip #3	5	**0.8**
SJ Chip #4	**1**	**0.8**

As shown in Fig. 4, the chip price is plotted against the breakdown voltage for all chip and cost scenarios. The BV crossover is defined as the BV point where both conventional and SJ MOSFETs prices are even. In the **Chip #1** scenario, the breakdown voltage crossover occurs at approximately 8.5 kV, assuming a fabrication cost of $1000 for each 12µm SJ drift region pillar (Cost #3). For **Chip #2**, reducing the pillar width to 1µm (the technological limit) significantly increases the chip density of SJ MOSFETs, as the specific on-resistance decreases by 50% compared to the 5µm width. This reduction leads to a 29% decrease in active area, with the BV crossover point dropping to around 3.6 kV, assuming the same $1000 fabrication cost, representing a 58% reduction in the crossover compared to **Chip #1**. In the **Chip #3** scenario, where the yield is increased by 33% (from 0.6 to 0.8), the crossover occurs at approximately 2.3 kV and 20 kV, assuming $1000 and $2000 fabrication costs, respectively. This results in a 73% reduction in the BV crossover compared to **Chip #1**. **For Chip #4**, the crossover points are around 1.2 kV and 4.6 kV, assuming fabrication costs of $1000 and $2000, respectively, though there is no crossover with **Cost #1**. Table 5 summarizes the breakdown voltage crossovers for different chip and cost scenarios, assuming a 10A current rating.

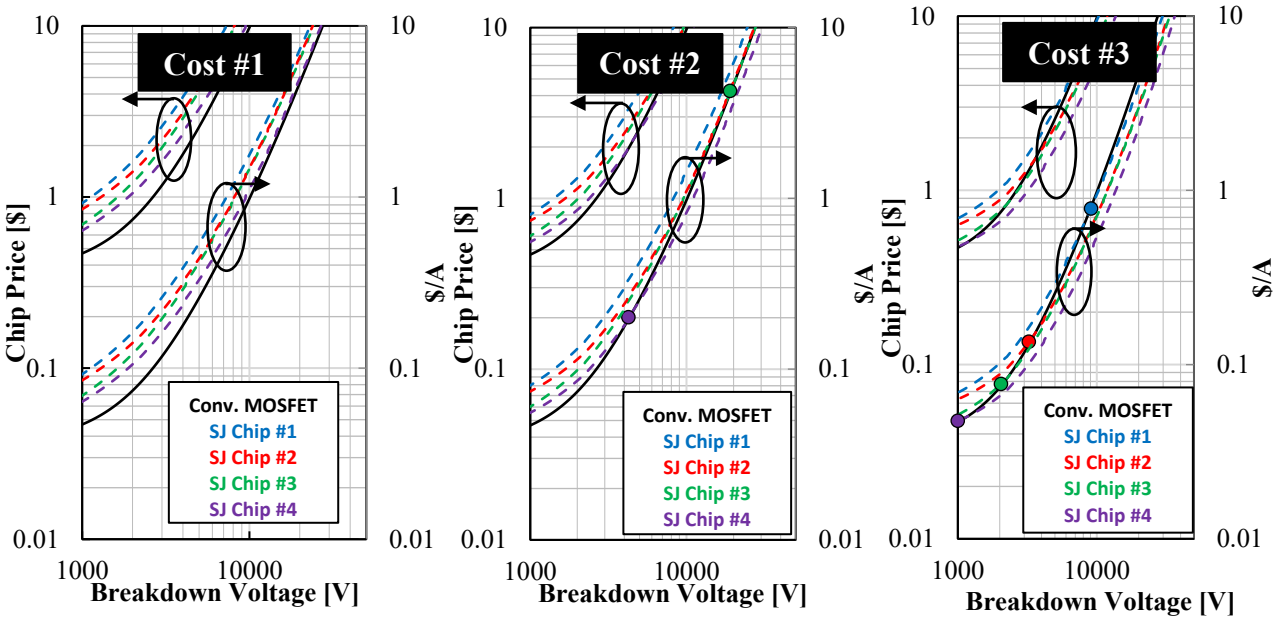

Fig. 4. Chip price and price per ampere for SJ MOSFETs with different design and cost scenarios compared to conventional MOSFETs assuming a current rating of 10A

Table 5. BV crossover and chip price per ampere for different SJ chip design and cost scenarios at 10A current rating.

Chip/Cost Scenarios (10A)	BV Crossover [kV]			Chip Price per Ampere [$/A]		
	Cost #1	Cost #2	Cost #3	Cost #1	Cost #2	Cost #3
SJ Chip #1	-	-	8.5	-	-	0.69
SJ Chip #2	-	-	3.6	-	-	0.15
SJ Chip #3	-	20	2.3	-	4.9	0.08
SJ Chip #4	-	4.6	1.2	-	0.22	0.05

Table 6. BV crossover and chip price per ampere for different SJ chip design and cost scenarios at 50A current rating.

Chip/Cost Scenarios (50A)	BV Crossover [kV]			Chip Price per Ampere [$/A]		
	Cost #1	Cost #2	Cost #3	Cost #1	Cost #2	Cost #3
SJ Chip #1	-	35	7.1	-	12.1	0.38
SJ Chip #2	34	9.2	3.5	11.2	0.64	0.12
SJ Chip #3	43	11	2.3	19.1	0.84	0.08
SJ Chip #4	9.3	3.9	1.2	0.65	0.14	0.05

Table 7. BV crossover and chip price per ampere for different SJ chip design and cost scenarios at 100A current rating.

Chip/Cost Scenarios (100A)	BV Crossover [kV]			Chip Price per Ampere [$/A]		
	Cost #1	Cost #2	Cost #3	Cost #1	Cost #2	Cost #3
SJ Chip #1	-	25	6.9	-	4.90	0.35
SJ Chip #2	20	8.6	3.4	3.09	0.52	0.12
SJ Chip #3	28	10	2.3	6.22	0.71	0.08
SJ Chip #4	8.7	3.9	1.2	0.54	0.14	0.05

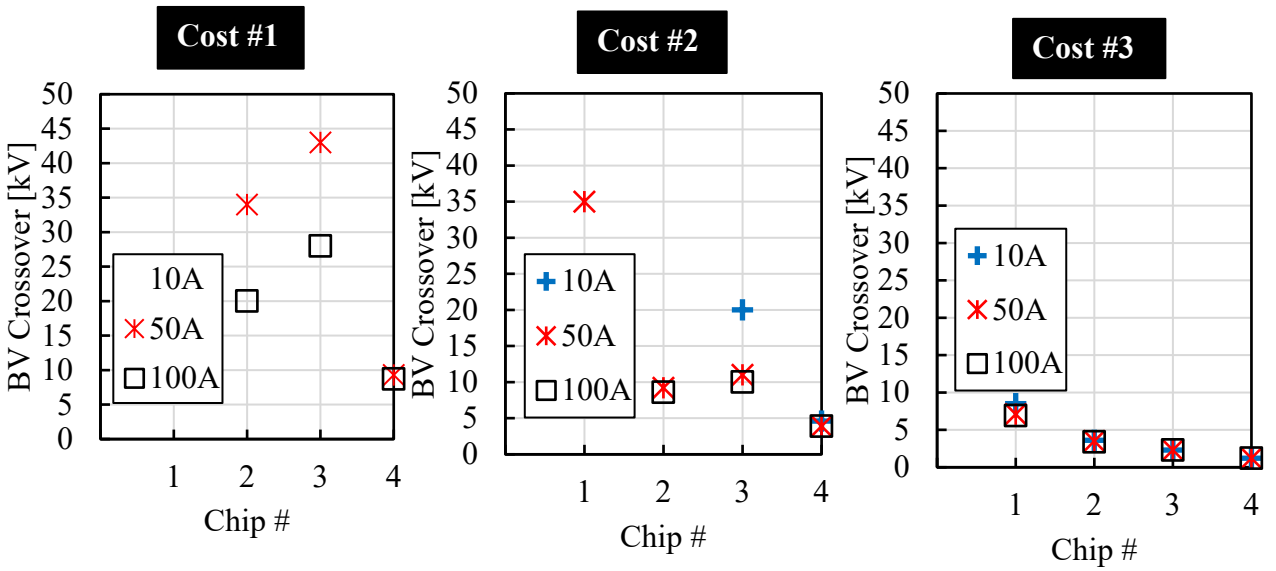

Fig. 5. BV crossover for all chip and cost scenarios at different current ratings. No data denotes no crossover.

At a 50A current rating as shown in Table 6, the breakdown voltage crossovers decrease across all chip scenarios at higher BV levels. This increase in SJ chip density is driven by the active area dominating the total chip size, rather than the edge termination. The dependence of the total chip size on the breakdown voltage is lower for SJ MOSFETs $\left(\sqrt{BV^{1.1}}\right)$ compared to conventional MOSFETs $\left(\sqrt{BV^{2.296}}\right)$ causing the crossover point to shift to the left, or decrease, at higher breakdown voltages. However, at lower BV values, the crossover point remains close to that of 10A, as the active area is already the dominant factor for both current ratings. While, at 100A current as shown in Table 7, the BV crossovers decrease for Cost #1 scenario even more as the active area is relatively more dominating compared to 50A current rating. Fig. 5 sums up all the BV crossovers for different chip and cost scenarios at 10A, 50A and 100A ratings.

Conclusion

The paper compares the economic feasibility of vertical high-voltage 4H-SiC Superjunction (SJ) MOSFETs with conventional SiC MOSFETs, focusing on the trade-off between specific on-resistance ($R_{ON,sp}$) and breakdown voltage (BV). SJ devices offer superior performance, especially at higher voltages, by reducing drift region resistance and achieving a better $R_{ON,sp}$ at a given BV. However, their complex fabrication processes significantly raise production costs. The analysis shows that despite the improved performance of SJ MOSFETs, their higher fabrication costs often limit their economic competitiveness compared to conventional MOSFETs, particularly at lower breakdown voltages and high-current applications. To make SJ MOSFETs economically feasible, the cost per chip must decrease or their yield and chip density must improve. The study concludes that SJ MOSFETs become more cost-effective as the breakdown voltage increases, especially in high-voltage and high-current applications, depending on the specific design and fabrication scenario. In summary, while SJ MOSFETs outperform conventional MOSFETs in high-voltage applications, reducing their production costs or improving fabrication processes is essential for widespread economic feasibility.

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