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Design Parameters Impact on Electrical Characteristics of 4H-SiC Thyristors with Etched Junction Termination Extension

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Abstract. 4H-SiC thyristors are of particular interest in pulsed power applications due to their ability to block high voltages and transfer high current densities along with fast switching times. Here, we present a paper that demonstrates both (i) the impact of the design parameters on the blocking characteristics based on simulations taking into account the anisotropy of 4H-SiC and (ii) a critical comparison to real devices having equivalent epitaxial structural design. Simulations and measurements show that an etched junction termination extension (JTE) is suitable to design high-voltage SiC thyristors. Concerning breakdown voltage, the real devices data agree to simulations for junction termination extension thickness in the relevant region. Besides the actual JTE thickness and doping concentration, the presence of a relatively thin field-stop layer might explain the discrepancy between experiment and simulation.

Introduction

Silicon carbide high power thyristors constitute the most promising switching device technology for pulsed power which potentially also could find their application in the civil domain, e.g., in HVDC distribution systems [1]. While medium-voltage (< 3.3 kV), unipolar SiC switches like SiC MOSFETs have been widely commercialized today, high voltage (3.3-6 kV) and especially very high voltage bipolar SiC devices like thyristors have not. This opens up the possibility for development and optimization of device parameters and technology. Here, we focus on the design and electrical characteristics of the thyristor and the effect of SiC anisotropy, the structural relationship of which between the junction termination extension (JTE) design and the underlying crystallographic orientation has been paid not that much of attention [2]. The main technological challenge is the design of an efficient JTE to significantly mitigate critical electric field distributions originating not only at the device periphery but also at their planar junctions, permitting to blocking very high voltage [3]. For ease of device processing, we focus on 1-step/3-step JTE design having the advantage to be realized using simple standard etching protocols [4].

Commercially high quality 4H-SiC wafers are grown in (0001) surface orientation, which causes the on-state current flow and electric field to be distributed mainly along the c-axis. However, the etched JTE introduces a crystallographic structure disorder in the direction perpendicular to the $(11\bar{2}0)$ plane. To optimize the breakdown voltage of a SiC thyristor it is important to design an appropriate JTE to avoid hot spots (spikes) of the electric field, which may generate local avalanche centers that trigger a breakdown in the device. Using multi-step design brings us closer to bevelled etch termination which is considered to be the most efficient one, by selectively removing charges from the junction at the edges [5]. The use of a 3-step design gives us another advantage over the 1-

step JTE. It can be seen that we achieve high breakdown voltage for different JTE etching depths, which are less prone against fluctuations resulting from reactive ion etching. The optimization can be done using TCAD simulation tools such as the Sentaurus software used in our case.

In this paper, we present the measurement results of breakdown voltage (V_{br}) and on-state characteristics of SiC thyristors with a thick drift layer and compare them with simulations. They prove that an etched JTE is suitable to design high-voltage SiC thyristors. We also report high influence of field-stop layer on V_{br} in punch through design which has not been fully investigated before. Finally, due to the complex and anisotropic nature of the SiC band structure, we investigate the influence of the <0001> and <11$\bar{2}$0> crystallographic orientations on the etched JTE thyristor breakdown voltage.

Device and Simulated Structures

A schematic cross-section of the fabricated and simulated thyristor with JTE is shown in Fig. 1. For our devices, we chose an n^+ substrate on which $p/p^-/n/p^+$ epitaxial layers were grown. The p^--drift layer is 100-µm thick and has a concentration of 4×10^{14} cm^{-3}; it is separated from the substrate by a thin field-stop (p-buffer) layer, the doping concentration of which, given by the manufacturer, is 1×10^{17} cm^{-3} and the thickness is 1 µm. The n-base (gate) layer is 2 µm thick and has a concentration of 1×10^{17} cm^{-3}, and the p^+-anode is 1-µm thick and has a concentration of 1×10^{19} cm^{-3}. The entire structure was covered with a 2-µm thick passivation of SiO_2. The fully processed wafer, fabricated at ISL, comprises 5×5 mm^2 thyristors with 1-step JTE, see Fig. 2. The devices have an active conduction area between the edge termination of 0.14 cm^2.

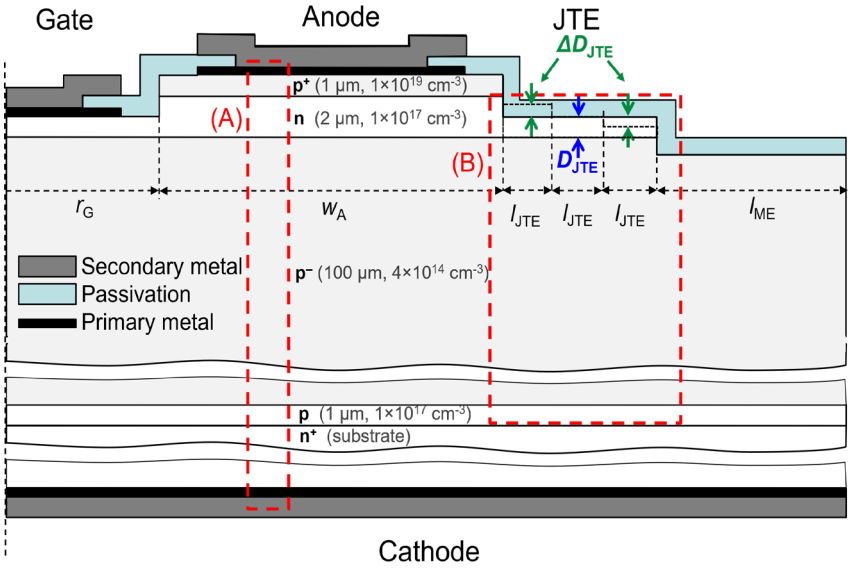

Fig. 1. Cross-section of thyristor half-cell, with simulated quasi-1D thyristor structure (region A) and central PiN diode with JTE (region B), respectively.

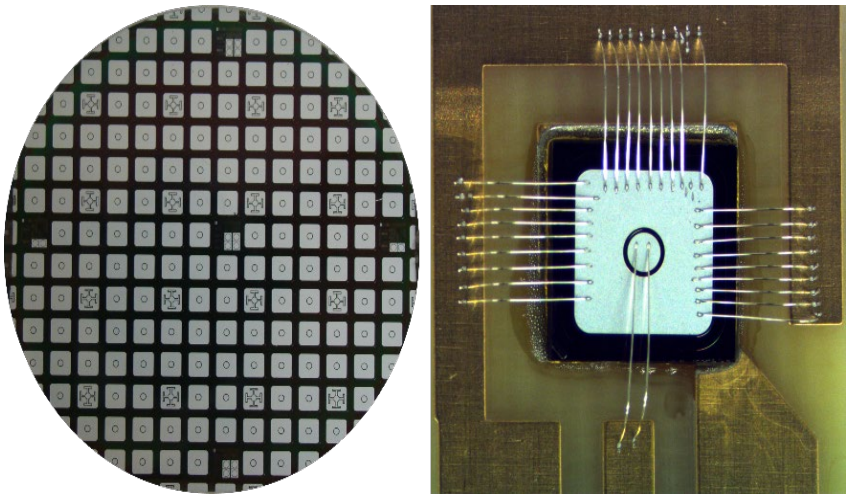

Fig. 2. Processed SiC wafer with thyristor devices under investigation (left) and bonded die (right).

In our simulations, in order to shorten the simulation time, the structure of the entire thyristor was simplified depending on the task under investi-gation. For simulating the maximum V_{br} and the on-state characteristic, it was simplified to a quasi-1D thyristor structure (*cf.* Fig. 1, region A). Simulating the V_{br} determined by the JTE, we can simplify the structure to the central PiN diode, located between the p^--drift and n-base (*cf.* Fig. 1, region B). For the PiN diode, the cell width in simulation is 250 µm and, for the quasi-1D thyristor structure, the width is 4 µm. All simulated structures are scaled in c-direction by an area factor of 10^8 per width, which corresponds to an area of 1 cm^2 for contacts.

In the study, we focused on de-vices with 1-step and 3-step JTE. For 1-step JTE, the simulation length is 150 µm and, for 3-step JTE, each step covers 50 µm which in total is equal to the single step design. The main parameter determining the V_{br} value is the actual JTE thickness, D_{JTE}. This thickness defines the amount of charge, which translates into a changing electric field distribution. In the case of the single-step design structure, we checked the breakdown voltage values for D_{JTE} depths from 0.5 to 1.1 µm. In case of the design with a 3-step JTE, it was first necessary to determine the most optimal ΔD_{JTE} step value (*cf.* Fig. 1). For this purpose, we used the D_{JTE} value of the single JTE step for which we obtained the highest breakdown voltage, and based on this we varied the height of the ΔD_{JTE} step from 0.2 to 0.5 µm. It turned out that the maximum V_{br} results were obtained for 0.4 µm. Using this value, we again performed simulations with D_{JTE} in the range of 0.5-1.1 µm. In parallel, we varied also the thickness of the field-stop (p-buffer) layer (using 0.8, 1, and 1.4 µm), and its concentration from 5×10^{15} cm^{-3} to 1×10^{18} cm^{-3}.

To portray the 4H-SiC thyristor in Sentaurus we used the built-in models for mobility, carrier lifetime, recombination, bandgap narrowing and avalanche. The two default lifetime models used in the simulations are the Shockley-Read-Hall (SRH) Concentration Dependent Lifetime Model and the Auger Recombination Lifetime model.

To simulate the breakdown voltage, it is necessary to use an avalanche model based on impact ionization coefficients. Due to the anisotropy of silicon carbide, the Okuto-Crowell model was used for avalanche generation, the simplified formula (see, Ref. 6 using: $T = T_0$, $\gamma = 0$, $\delta = 1$) of which is presented in Eq. 1:

$$\alpha(E) = a_{n/p} exp\left[-\frac{b_{n/p}}{E}\right] \quad (1),$$

where E is the electric field and a, b are impact ionization coefficients defined as the number of electron-hole pairs generated by impact ionization under a certain electric field. In our simulations,

we used the basic impact ionization coefficients taking into account the anisotropy of SiC which are presented in Table 1.

Table 1. Impact ionization parameters from Ref. 7 used for the Okuto-Crowell model.

Crystallographic orientation	a_n [cm^{-1}]	b_n [$V \times cm^{-1}$]	a_p [cm^{-1}]	b_p [$V \times cm^{-1}$]
<0001>	1.76×10^8	3.3×10^7	3.41×10^8	2.5×10^7
$<11\bar{2}0>$	2.1×10^7	1.7×10^7	2.96×10^7	1.6×10^7

The use of this model is important to correctly simulate the breakdown voltage because the mass of the carriers varies depending on the crystallographic orientation. From the point of basic device physics, it is clear effective masses have their impact on the acceleration of carriers when an electric field is applied which then directly translates into mobility, transport, and drift velocity, and in turn contributes to the impact ionization coefficients [8].

Blocking Characteristics

Simulation results concerning the breakdown voltage of the SiC thyristor under investigation with 1-step and 3-step JTE are shown in Fig. 3. The graph shows that using a larger number of steps results in a higher breakdown voltage. Regarding the 1-step JTE (anisotropic case) a maximum V_{br} of 11.5 kV is reached when D_{JTE} is close to 0.7 µm whereas, for the 3-step JTE, the maximum V_{br} is 15 kV for D_{JTE} = 0.8 µm. This corresponds to 66% and 86% of the theoretical value, respectively, simulated using a simple 1D-diode structure.

The results of measurements, performed on a thyristor with a 1-step JTE, where the optimal D_{JTE} was assumed to be 0.9 µm (see Fig. 3, denoted "only <0001>"), show that for the best device the breakdown voltage is 7 kV. Fig. 4 shows the I-V characteristics in forward blocking direction. Comparing the measurement results with simulations for a 2D-PiN diode with 1-step JTE, it can be seen that the blocking voltage more closely corresponds to the D_{JTE} etching depth of 0.8 µm (Fig. 3), which is within the limit of technological and measure-ment errors.

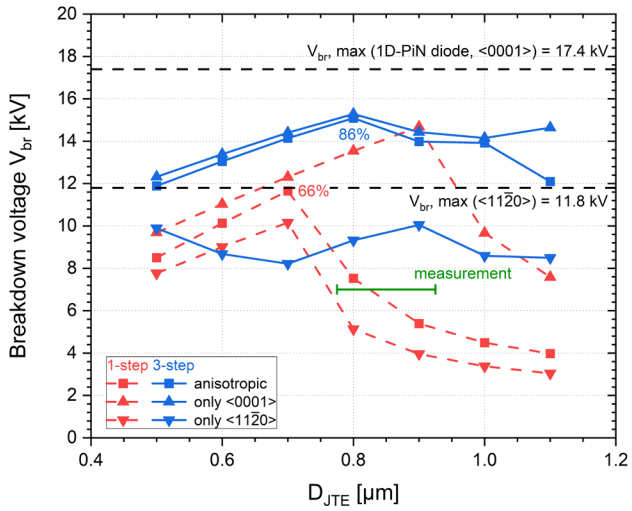

Fig. 3. Simulation of V_{br} as a function of D_{JTE} for 1-step (ΔD_{JTE} = 0 µm) and 3-step JTE (ΔD_{JTE} = 0.4 µm), l_{JTE} = 50 µm, each for anisotropic and isotropic impact ionization (*cf.* values in Table 1).

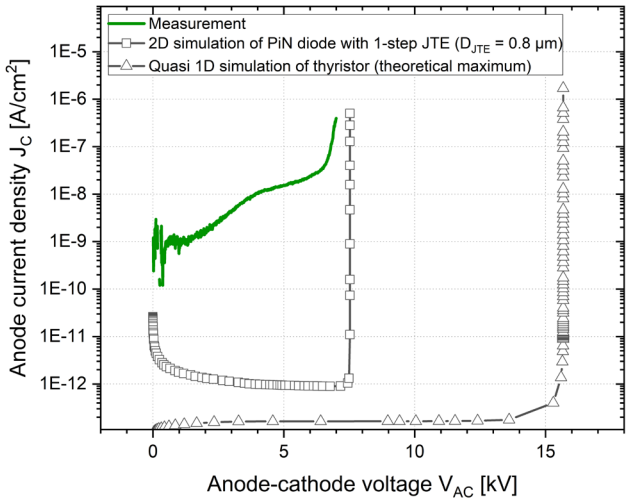

Fig. 4. Measured forward blocking characteristic of one of the best devices compared to simulation.

Regarding these measurement results, we see that the experimentally obtained breakdown voltage does not attain the best simulation results, based on the specifications/capabili-ties of the SiC wafer used. Therefore, we investigated how the blocking voltage is influenced by the para-meters of the field-stop (p-buffer) layer (Fig. 5). Due to the punch-through design of our thyristor, which provides a more gradual distribution of the electric field in the drift layer [5], the field-stop layer concentration is of great importance. Regarding the simulation results in Fig. 5, it can be assumed that the 1-µm thick field-stop (p-buffer) layer must actually have a concentration of 3×10^{16} cm^{-3}, instead of 1×10^{17} cm^{-3}, as denoted in the wafer specification. Thus, if only the field-stop layer is considered, the limited efficiency of 7 kV gained in measurement could be attributed to its unexpectedly low doping concentra-tion.

In Fig. 3, we also present the influence of 4H-SiC anisotropy for devices with 1-step and 3-step etched JTE. In addition to the simulations already described above, Hatake-yama's impact ionization coefficients (Table 1) were used individually, with the anisotropy deactivated. This made possible to investigate the influence of individual crystallo-graphic orientations on the break-down voltage. For 1-step JTE with D_{JTE} up to 0.7 µm, we observe that the anisotropic results are in between the results for the individual crystallo-graphic orientations. Above this D_{JTE}, the V_{br} values are closer to those for the <11$\bar{2}$0> orientation. For 3-step JTE, it can be seen that the breakdown voltage results, for practically the entire range of D_{JTE} thicknesses, are close to the voltage value obtained when using coefficients of the <0001> direction. A deviation is observed only for the thickness of 1.1 µm, for which (with ΔD_{JTE} = 0.4 µm) we are approaching a quasi-2-step JTE (same holds for values below 0.6 µm).

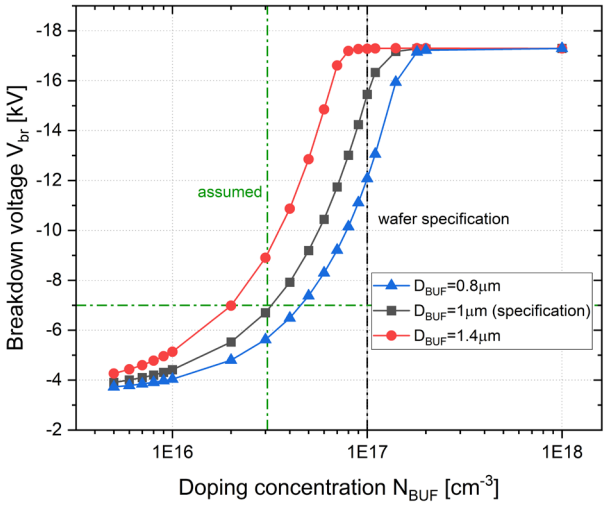

Fig. 5. Simulation of V_{br} as a function of field-stop (p-buffer) layer concentration (N_{BUF}) and thickness (D_{BUF}).

Analyzing these results, we observe that in the case of a 1-step JTE, the electric field distributed along the JTE translates into a larger share of the anisotropy phenomenon in <11$\bar{2}$0> direction, while, for a 3-step JTE, due to the divided JTE regions, <0001> direction becomes dominant. Regarding the 1-step JTE, the interpretation corresponds to what has been shown and concluded in Ref. 7, concerning an implanted JTE: When the implantation dose (which compares to the thickness D_{JTE} in case of our etched JTE) becomes higher than the optimum, the breakdown occurs at the outer edge of the JTE, where the electric field is rather lateral, and thus is dominated by the lower impact ionization coefficients in <11$\bar{2}$0> direction. In case of an etched JTE, the same argumentation holds for a thickness, lower than the optimum, when the breakdown occurs at the inner edge of the JTE. Around the optimum thickness, the electric field is homogenously spread along the JTE and therefore, rather aligned in <0001> direction. Thus, as can be observed in Fig. 3 for the "anisotropic" curve of the 1-step JTE, the breakdown voltage is turning over towards the "<0001>" curve and then back to the one for <11$\bar{2}$0> direction. Using a 3-step JTE, on the other hand, allows spreading the electric field for a much wider range of D_{JTE}. Therefore, the "anisotropic" curve of the 3-step JTE in Fig. 3 approaches the one limited to <0001> orientation along almost the entire range.

On-State Characteristics

The on-state characteristics of the simulated and measured SiC thyristors are presented in Fig. 6 for two drift layer thicknesses (D_{DRI}), 10 µm [9] and 100 µm, respectively. The default carrier lifetime values for electrons (τ_e) and holes (τ_h), implemented in the Sentaurus 4H-SiC parameter file, are 2.5 µs and 0.5 µs, respectively. To turn the thyristors on, we apply a current I_G = -100 mA to the gate, for both simulations and measure-ments. The measurements for both the 10-µm and 100-µm thick drift layer show a much higher on-state voltage drop than the simulations, when the default lifetime values and no contact resistance are considered. For a 10-µm thick drift layer, we measure a forward voltage drop of 3.8 V at 100 A/cm^2, while, for a 100-µm drift layer, we determine 5.8 V. At first glance, this is consistent as the thicker drift layer comes up with a higher resistance. However, com-paring the results with the simu-lations we see that the thickness of the drift layer does not have that much of an impact on the forward voltage drop.

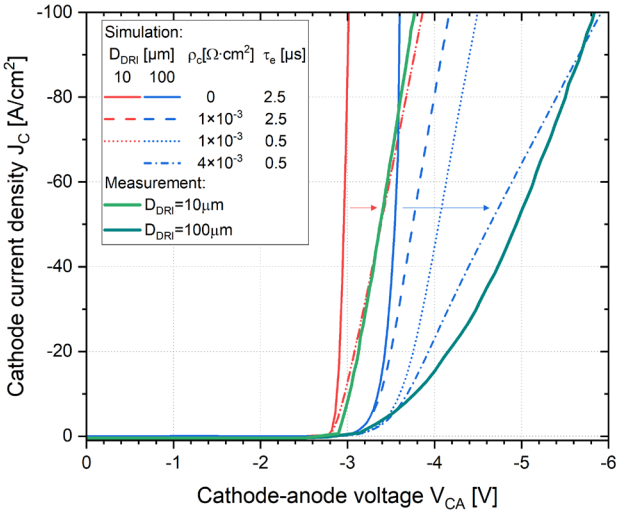

Fig. 6. Simulated and measured on-state characteristics of SiC thyristors with different drift layer thicknesses D_{DRI} (ρ_c: specific contact resistivity, τ_e: electron lifetime).

One reason for this behavior could be that no additional series resistance has been taken into account in the initial simulations. Looking for a relevant contribution of such a resistance, we identified the anode contact resistance, the value of which was determined using TLM test structures on both SiC wafers concerned, here, quantitatively in the order of $\rho_c = 1\times10^{-3}$ Ω·cm^2. Using this value in the simulations allowed getting close to the measured on-state characteristic in case of the 10-µm drift layer. For the 100-µm drift layer, however, the dashed line in Fig. 6 indicates that some other contribution must be attributed to the much larger, measured voltage drop.

An additional explanation for the discrepancy between simulation and measurement could be the very short lifetime of the carriers due to the large amount of carbon vacancy defects incorporated, which shorten the diffusion length of minority carriers in the drift region [10]. It should be noted that, to effectively reducing the number of these carbon vacancy defects, various high temperature processes (1300-1700°C) have been proposed, although, here, none of our devices was treated in that direction. Thus, in order to investigate the influence of the electron lifetime, τ_e, the minority carrier lifetime in the p-type drift layer, was reduced to 500 ns, a value still seen as typical in spite of the underlying indirect-transition band structure [10]. As the dotted lines in Fig. 6 show, this reduction further increases the voltage drop in the case of the 100-µm drift layer. As expected for a thin drift layer (here 10 µm), the carrier lifetime has no significant effect in this aspect.

Finally, in order to getting close to the measured curve of the SiC thyristor with the 100-µm drift layer, the contact resistance was further increased in the simulations, in accordance with a specific resistivity of 4×10^{-3} Ω·cm^2, a value taken from TLM measurements in the center of the wafer under investigation (*cf.* Figs. 2). Even though a further reduction of τ_e would increase the total voltage drop, it further increases the threshold voltage as well, and therefore does not result in a better match to the measurement curve.

Conclusion

In this paper, SiC thyristors with 1-step and 3-step JTE were presented as high voltage blocking devices for pulsed power applications. Experimental devices with a 1-step JTE confirm the breakdown voltage simulation results when a lower doping concentration value of the field-stop (p-buffer) layer is taken into account. According to the simulations, the use of a 3-step JTE would allow a breakdown voltage of 12-15 kV for an appropriately selected etching depth. Comparing breakdown

simulations based on anisotropic impact ionization with those just partially using coefficients for either <0001> or <11$\bar{2}$0> orientation, revealed that a 1-step JTE is strongly affected by the lower coefficients of the <11$\bar{2}$0> direction. Therefore, a JTE with multiple steps does not only benefit from an increased robustness to process variations, in particular concerning the thickness D_{JTE}, but also from a higher breakdown voltage in <0001> direction. Thus, the relatively low breakdown voltage of our experimental devices can partially be related to the fact, that they have only a 1-step JTE implemented. Regarding on-state characteristics, we demonstrated that the SiC thyristor devices under investigation work properly with a relatively low on-resistance. TCAD simulations permitted to relate the actual voltage drop to both a series resistance, most probably of the anode contacts, and a relatively low minority carrier lifetime in the drift layer of 500 ns. Further investigation on the carrier lifetime impact needs to be done due to its high relevance for dynamic switching.

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