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On the Characterization of 4H-SiC PiN Diodes and JFETs for their Use in High-Voltage Bidirectional Power Devices

Arne Benjamin Renz[1,a*], Yifan Jiang[3,b], P.M. Gammon[1,2,c], Erfan Bashar[1,d] and Jiankang Bu[3,e]

[1]University of Warwick, School of Engineering, Coventry, UK

[2]PGC Consultancy Ltd, Stratford-upon-Avon, UK

[3]Ideal Power Inc, Austin, TX, USA

[a]Arne.Renz@warwick.ac.uk , [b]Yifan.jiang@idealpower.com , [c]P.M.Gammon@warwick.ac.uk, [d]E.Bashar.1@warwick.ac.uk , [e]Jiankang.Bu@idealpower.com

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Abstract. A bidirectional field-effect transistor (FETs), known as a BTRAN™, was designed, fabricated and characterized on silicon carbide (SiC) for the first time. After grinding to original N+ substrate, atomic force microscopy revealed grinding marks and an increase of surface roughness to a rms value of 7.812 nm (50 µm x 50µm scan area), but these were suitable for further device processing. A lifetime enhancement oxidation process carried out on both sides of the drift region at 1400°C for 4 hrs in dilute oxygen (4 slm Ar : 1 slm O_2) enhanced the average carrier lifetime from 1 µs to 5 µs. After device fabrication, functionality was proven both on-die and on a custom-made PCB design that enabled access to all four terminals (topside and bottomside) in the on-state and off-state. Off-state measurements revealed a breakdown voltage exceeding 7 kV. In summary, these encouraging results, with necessary improvements of contact resistivity, will build the foundation for the second generation of SiC BTRAN™ devices.

Introduction

Power electronics are a key enabling technology in the process towards a fully electrified society. Modern power conversion is integral in delivering efficient electric vehicles (EVs) and their fast charging stations, advanced motor drives and the integration of renewable energy into a modern grid. With an EV market share of 50% targeted by the US Government and the fact that about 50 % of all electricity is used to power and drive electric motors, it becomes evident that efficiency of power electronics systems will be at the center of any policy that wants to steer society towards a more sustainable energy economy.

In these applications, well-developed converter topologies are key. Ideally, these would contain semiconductor switches that have both excellent blocking capabilities in both directions and bidirectional current conduction in the on-state [1]. However, none of the conventional semiconductor switches, e.g., insulated-gate bipolar transistors (IGBTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs), can provide these functionalities alone, such that multiple discrete device topologies are typically deployed. As an example, an inverse-series connection of two silicon (Si) MOSFETs achieves switching functionality in two directions, but the total on-resistance (R_{ON}) is doubled compared to a single device. To circumvent this, a second arrangement needs to be connected in parallel. This means that, for the realization of bidirectional switching capability, using common power semiconductors results in a fourfold increase in chip area and cost. The introduction of monolithic bidirectional switches (MBDSs) with a single shared drift region for blocking either voltage polarity, and two gates, means that these converter topologies need to reevaluated.

The research activities on MBDS devices can be traced back to the early 2000s, with early activities focusing on IGBTs that were reverse-blocking [2]. Within a few years, multiple companies started to investigate MBDSs based on gallium nitride (GaN) high-electron mobility transistors (HEMTs). These devices were typically rated at around 600V, with resistances reaching 140 mΩ [3].

In silicon carbide (SiC), MBDS device development is still at a very early stage. Research activities have so far resulted in the successful fabrication of a monolithic bidirectional IGBT, where demonstrator devices have successfully blocked up to 7 kV [3]. However, processing requires a non-standard, processing methods, including grinding away the original wafer to access the backside of the drift region, double sided lifetime enhancement, and double-sided photolithography including backside alignment. When packaged, novel cooling solutions as both sides of the wafer feature intricate structures, such as gates, base and emitter regions.

This work aims to demonstrate a SiC BTRAN^{TM} device concept that was originally developed for Si processing [4]. This features a field-effect transistor (FET) on each side of the wafer with a shared collector region (B-TRAN ^{TM}). Vertical Si devices have achieved a blocking voltage of ± 1200 V and were able to support pulsed currents of up to ± 100 A. In this investigation, we aim to transfer this concept to 4H-SiC. Firstly, vertical PiN diodes and lateral devices were simulated, fabricated and characterized on both the C-face (000-1) and Si-face (0001), as required to produce a SiC B-TRAN^{TM}. The carrier lifetime of the thick drift region was then optimized to enable sufficient carrier diffusion for conductivity modulation.

Experimental

Devices were fabricated on a 100 mm diameter, 350 µm thick n+-substrate, onto which was grown a 150 µm thick n-type unintentionally doped (<1 x 10^{15} cm^{-3}) epitaxial layer. After initial alignment mark formation between topside and bottomside, the samples were flipped to remove the n+-substrate by means of grinding. The scanning electron microscope (SEM) image in Fig. 2 shows the resulting cross-section of the wafer. High-temperature oxidation was then carried out at 1,400°C in a dilute oxygen ambient (4 slm Ar : 1 slm O_2) on both the Si-face and C-face to improve the carrier lifetime,

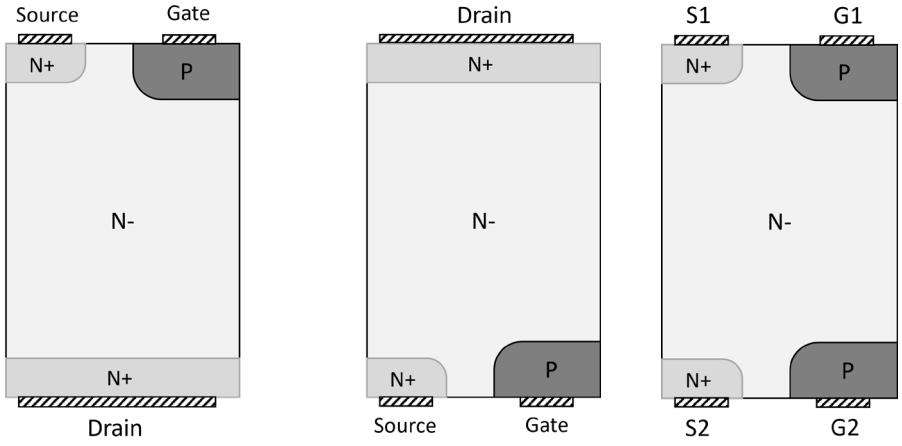

Fig.1. Cross-sectional representation of the JFET structures (left and middle) and the full BTRAN ^{TM} device (right).

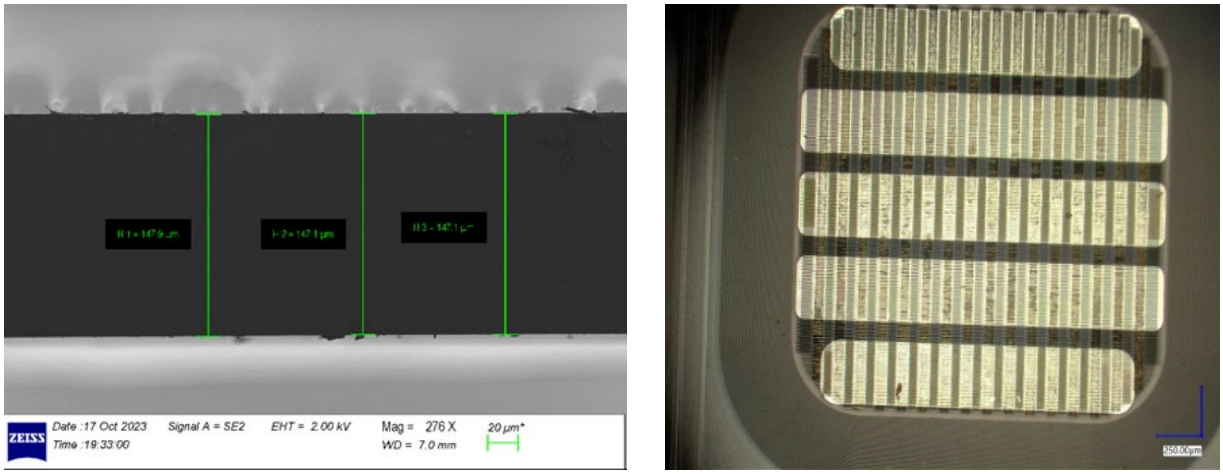

Fig. 2. (Left) The drift region thickness post-grinding, measured by cross-sectional SEM imaging. (Right) Optical microscopy image of the finished one-sided BTRAN device, fabricated on the C-face after substrate removal.

similar to [5]. P+- implants and n+-implants were then carried out on both the Si-face and C-face to enable gate, source (on the BTRAN) and cathode and anode ohmic contact formation (on the PiN diodes). A 1.5 µm thick passivation layer was then deposited on both samples by means of low-pressure chemical vapour deposition (LPCVD), using tetraethyl orthosilicate (TEOS) as Si precursor before a 1.5 µm thick aluminium (Al) pad metal was deposited to aid with device testing and wire bonding. The final device structure can be seen in Fig. 1, with microscopy images in Fig. 2. Atomic force microscopy (AFM) measurements were carried out on a Bruker Icon AFM in peakforce tapping mode to extract surface roughness and quantify any possible large wafer bow post-grinding.

The enhancement throughout the drift thickness is diffusion limited due to the low diffusion coefficients of carbon and oxygen in SiC. Common carrier lifetime measurement techniques such as microwave-detected photoconductance decay (µ-PCD) probe the near-surface region of the epilayer, give an indication of carrier lifetime. Time transient data was measured by µ-photoconductive decay (PCD), which has a 355 nm ultraviolet (UV) laser source. The effective carrier lifetime was assessed prior to and after lifetime enhancement in a custom Freiberg Instruments spotMDP setup.

Results

Low surface quality post-grinding is required for the success of the device fabrication. An extensive AFM investigation was conducted once the samples had their substrates removed and prior to further processing. An overview of the extracted root mean square (RMS) values can be found in Table 1. Representative images of the top side and bottom side can be found in Fig. 3 below. A full wafer post-grinding is depicted in Fig. 4 (left), too.

Table I. Extracted surface roughness parameters post-substrate removal. All measurements were done at room temperature.

		Scan area	
Topside/backside	**Position on 4" wafer**	**5 µm x 5 µm (nm)**	**50 µm x 50 µm (nm)**
Topside	**Centre (0,0)**	0.267	0.494
Topside	**Bottom right (25mm, -25mm)**	0.256	0.615
Topside	**Top left (-25mm, 25mm)**	0.254	0.538
Backside	**Centre (0,0)**	4.377	7.812
Backside	**Bottom right (25mm, -25mm)**	5.122	5.473
Backside	**Top left (-25mm, 25mm)**	3.369	4.619

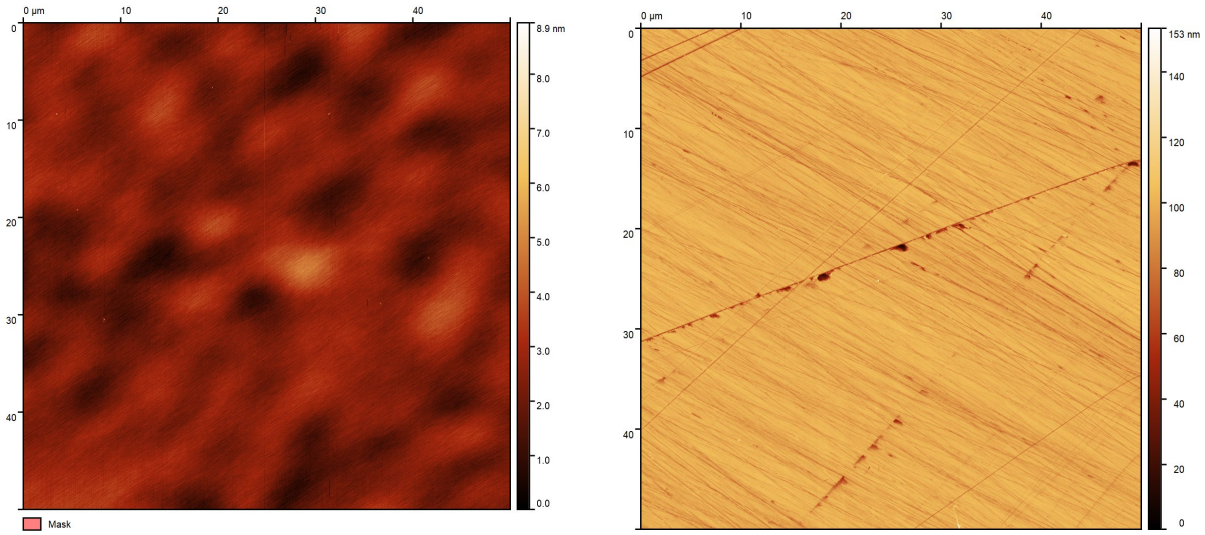

Fig. 3. (Left) Image of a representative 50 um x 50 um scan of the (left) frontside, which did not undergo the processing and achieved a <1 nm rms surface roughness value and (right) backside, which was grinded, showing grinding marks post-processing.

The surface quality of the thick, as-grown, epitaxial layer can be seen when observing the extracted rms values from the top. Here, even surface roughness values that are extracted from a 50µm x 50µm scan area are significantly lower than 1 nm, with values averaging 0.55 nm. No obvious further surface modifications/decorations were visible during any topside measurement, with all measurements averaging tightly at around 0.5 nm. After the substrate was then fully removed by grinding, the surface showed grinding marks throughout, with surface roughness values averaging 10 times higher at 5.96 nm. With all contacts in the BTRAN^{TM} devices being ohmic, fabrication was then continued.

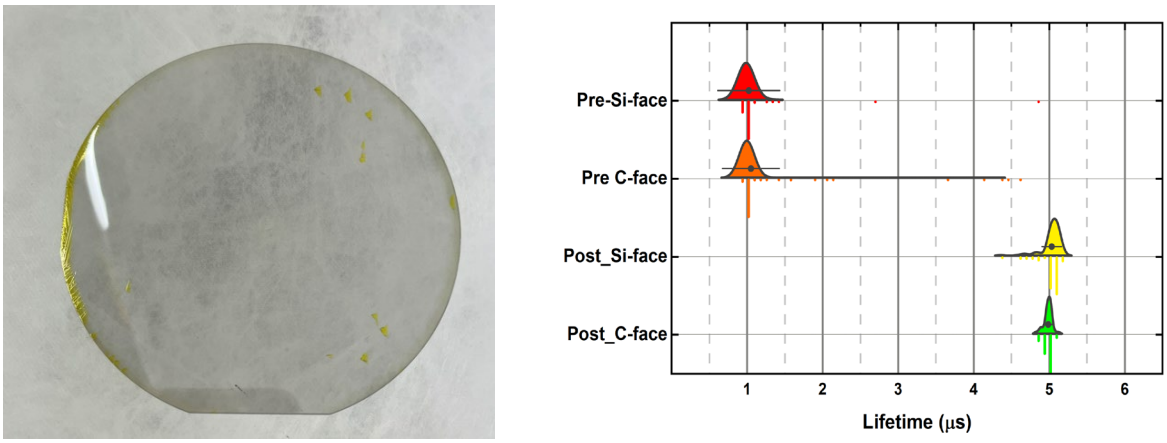

Fig. 4. (Left) Image of a full four inch wafer post-grinding, with bright spots representing triangular defects in the 4H-SiC epilayer and right) u-PCD measurements before and after high-temperature oxidation (λ = 355 nm), with 400 measurements being taken at room temperature per dataset.

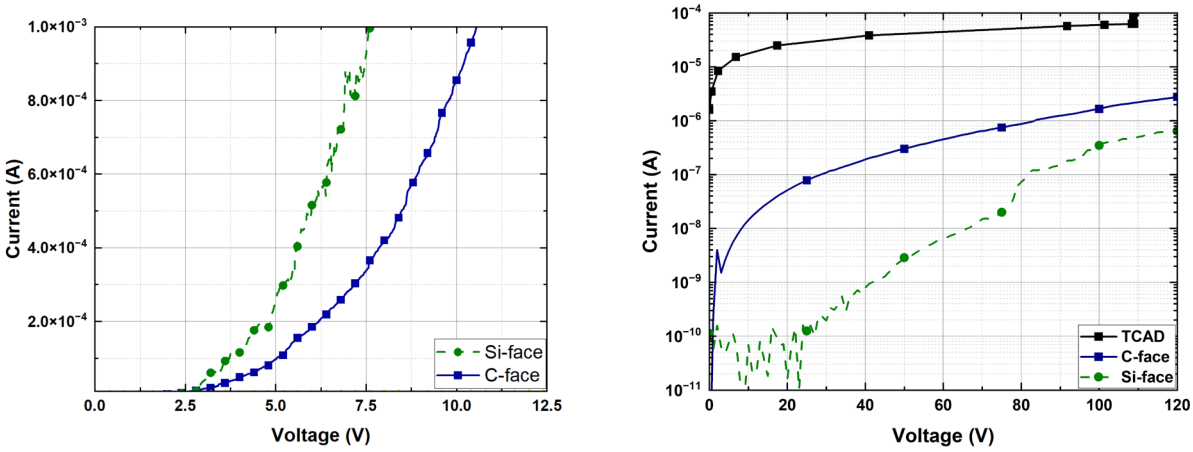

Fig.5. Gate-source forward (left) and reverse (right) characteristics of diodes fabricated on C- and Si-face.

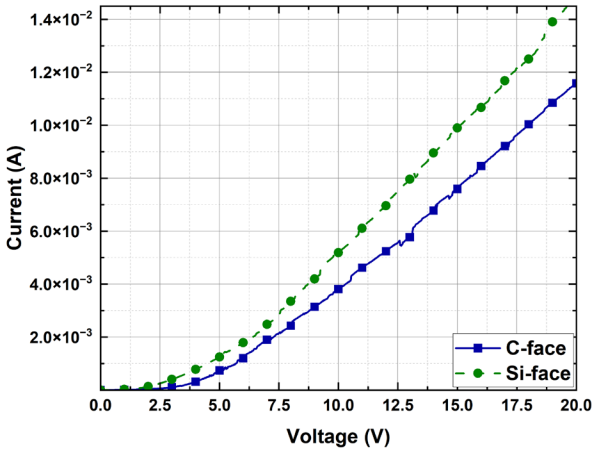

Fig.6. On state of vertical PiN diodes fabricated on both the C-and Si-face.

After the grinding process, an analysis of the transient carrier lifetime on the Si- and C-face was carried out before and after the lifetime enhancement oxidation process. The results are shown in Fig. 4 (b), where 400 spot measurements were taken at room temperature across the wafer. More details about the 4 hour lifetime enhancement procedure can be found in [5]. Prior to the lifetime enhancement treatment, the effective carrier lifetime on the thinned wafer averaged about 1 µs, both on the Si- and the C-face. After the thermal oxidation process, the lifetime was increased to approximately 5 µs, which will enhance conductivity modulation in the thick drift region.

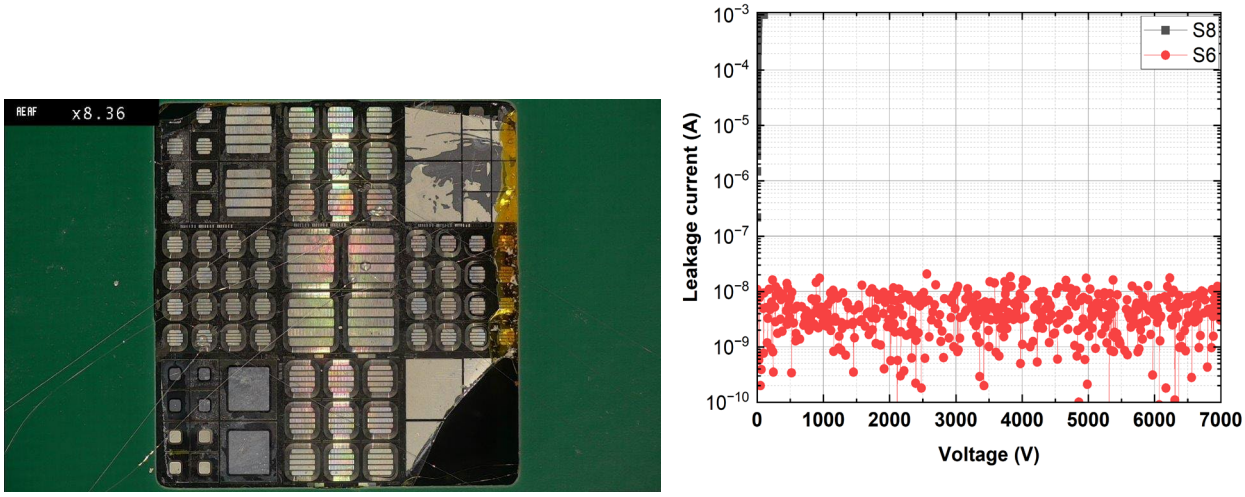

Fig. 7. (Left) Final chip on PCB for bi-directional switching of the BTRAN^{TM}, allowing for the static characterization of multiple devices on that chip. Individual devices were then wire bonded to contact pads that are located outside of this chip. (Right) blocking voltage of a single tested BTRAN^{TM} device, showing no visible signs of leakage up to 7 kV.

The active area design comprised a 1 µm trench etch into the gate area, into which a p+-region of 200 nm was implanted.

After fabrication, the lateral P-gate to N-source breakdown in the devices was measured on wafer, depicted in Fig. 5, right, where the breakdown exceeds 100 V, outperforming TCAD simulation results. Representative on-state results for the lateral JFETs (Fig. 5, left) and vertical PiN diodes (Fig. 6) show the functionality of the fabricated structures.

Having proven the general functionality of the fabricated structures on-die, wafers were laser cut and chips were then soldered onto custom-made PCBs. These were designed to allow access to terminals on both the back side and the top side of the same chip. An example of a chip that had been soldered onto one of these PCBs can be seen in Fig. 7 (left) below. Terminals were bonded to terminal pads by means of wire bonding using approx. 50 µm aluminium wire. Once this was done, we were able to measure the blocking voltage (S1-G2) between the topside source and bottom side gate, all the way up to 7 kV. To prevent arcing, fluorinert gel was applied directly before the leakage measurements were carried out. A representative device with poor leakage performance is shown in Fig. 7 (right). Some devices managed to show excellent breakdown performance, as demonstrated in the same figure.. For leakage measurements, all other terminals were left floating.

The same configuration also allowed for the on-state measurement of devices, which can be seen in Fig. 8 (left) and the on-state voltage drop in Fig. 8 (right).

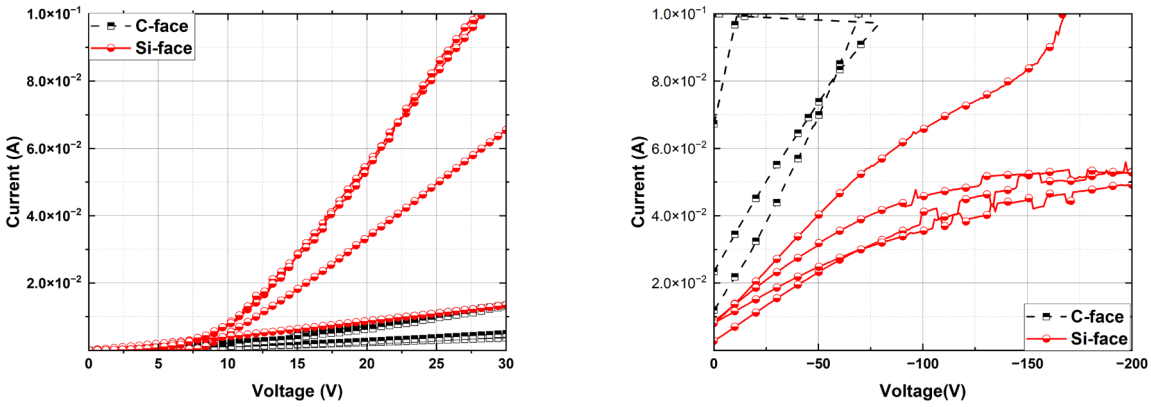

Fig. 8. (Left) On-state of the observed SiC BTRAN^{TM} and (Right) on-state voltage drop on individual devices..

The on-state (G1-S1) was then measured using a B1505 A probe station with a high-current extender (bottom left). The G1-S1 diode performance, with forward current up to 100 mA, could be observed on Fig. 8(left). The other terminals were left floating. A specific contact resistivity of the p-type ohmic contact of 1.16 x 10^{-2} Ω.cm^2 and 1.34 x 10^{-3} Ω.cm^2 of the n-type ohmic contact were extracted from TLM measurements and can be one source of the relatively high resistance that can be observed in the on-state of the PiN diodes, as well as the BTRAN^{TM}. In Fig. 8 (right), the on-state voltage drop between devices can be seen, confirming this trend. Here, a DC voltage of 30 V was applied across the topside of the base, for current injection through the base. The voltage was then swept between the topside source (S1) and gate on the bottom side (G2).

Conclusion

In this investigation, we successfully simulated, designed, fabricated and characterized the first fully functional silicon carbide BTRAN^{TM} device. As part of the challenges in the fabrication process, we demonstrated, that, after substrate removal, the backside of the wafer showed grinding marks and an increase in surface roughness up to 7.812 nm, when investigated on a 50µm x 50µm by means of atomic force microscopy.

To help conductivity modulate the device, a carrier lifetime enhancement investigation was conducted, where we oxidized the samples in a high-temperature furnace at 1400°C for 4 hrs in dilute oxygen ambient (4 slm Ar : 1 slm O_2). This raised the lifetime relatively uniformly from 1 µs (pre-treatment) to approximately 5µs (post-enhancement), both on the C- and Si-face of a full 4” wafer.

The fully fabricated structures were then measured on-die, where on-states showed the full functionality of one-sided structures laterally, although the conduction response suffered heavily from high specific contact resistivities, averaging 1.16 x 10^{-2} Ω.cm^2 and 1.34 x 10^{-3} Ω.cm^2 on TLM structures for p-type and n-type ohmic contacts, respectively. Selected chips were then soldered on a custom-made PCB design, allowing the static characterization of the full BTRAN^{TM} devices by enabling access to both contacts on the topside and backside of the chip. Here, on-states of the full device structures showed general functionality, although suffering from high specific contact resistivities. A promising performance off-state was demonstrated, blocking more than 7 kV. In summary, these encouraging results, with necessary improvements of contact resistivity, will build the foundation for a second generation of BTRAN^{TM} devices to full commercialization.

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