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The 3rd Quadrant Operation of 4th Generation SiC MOSFETs: Recovery Charge & Bipolar Degradation

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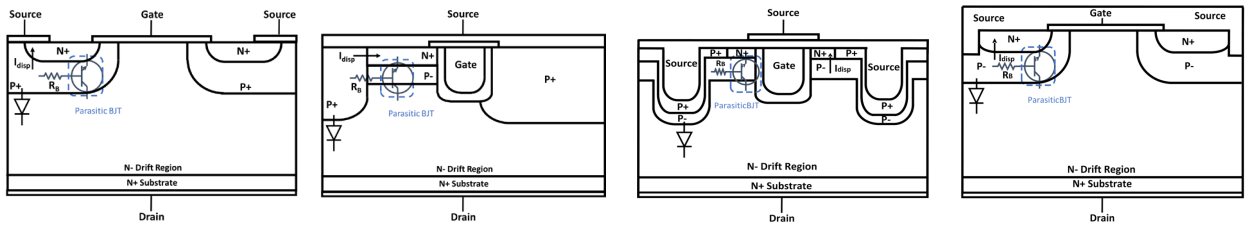
Abstract. In this paper, the performance in 3rd quadrant operation of 3rd and 4th generation SiC power MOSFETs have been evaluated. These are the Gen-3 1.2 kV & 18 A Planar SiC MOSFET, Gen-3 1.2 kV & 19 A Asymmetrical Trench SiC MOSFET, Gen-4 1.2 kV & 26 A Symmetrical Double-Trench SiC MOSFET and Gen-4 1.2 kV & 19 A Trench-Assisted Planar SiC MOSFET. Further, the transients of early-stage degradation development are investigated by conducting continuous stress current thorough body diode of the aforementioned devices to explore the extent of degradation in the body diodes of SiC MOSFETs. These devices are compared to provide a better understanding of the impact of different structures.

Introduction

The evolution of power electronics has been recently entangled with the developments of silicon carbide (SiC) MOSFET technologies due to its high breakdown electric field and thermal conductivity [1-4]. Over the years, SiC MOSFET technology has undergone several generational improvements. The newest 4th generation SiC MOSFETs have delivered improvements in critical performance metrics, i.e. the switching rates and on-state resistance due to the novel design structures employed such as aggressive cell pitching and substrate thinning. The cross-sectional schematics of both the 3rd Generation and 4th Generation devices are shown in Fig. 1. The Fig. 1(a) and (b) show the typical structure of Gen-3 SiC Planar and Asymmetrical Trench MOSFETs, while Fig. 1(c) and (d) show the newer SiC Symmetrical Double-Trench and Trench-Assisted Planar MOSFETs. The Gate-Trench structured SiC MOSFETs typically suffer more from gate oxide reliability issues because of the high electric field at the bottom of the gate trench [5]. To improve this, the P-wells in Gen-4 design are deeper, as shown in Fig. 1(c), which further distances the high electric field from the gate, providing better protection. These improvements provide better gate oxide reliability and higher efficiency in the first quadrant operation.

MOSFETs also allow the 3rd quadrant channel conduction while the body diode is used for freewheeling during the switching dead band. This feature helps prevent voltage spikes, ensuring device protection and enhancing circuit reliability [6-9]. There are some questions in terms of the performance of the body diode of recent devices though. For example, body diode of the Symmetrical Double-Trench MOSFET could have worse reverse recovery because of the deeper P-wells, which results in additional carriers that must be extracted during the turn-off process. This is also unclear in case of the SiC Trench-Assisted Planar MOSFETs [10]. It is also unclear whether different structures could mitigate the severity of bipolar degradation. To address this, double pulse tests and continuous DC current stress tests are conducted on both 3rd and 4th Gen devices to investigate the impacts of the newly emerged structures to these performance metrics.



(a) (b) (c) (d)

Fig. 1. The cross-sectional view of the studied SiC MOSFETs: (a) Planar; (b) Asymmetrical Trench; (c) Symmetrical Double-Trench; (d) Trench-Assisted Planar.

The 3rd Quadrant Operation: Transients & Reverse Recovery

Firstly, measurements are performed at a wide range of switching rates using a bespoke double pulse test board on 1.2 kV devices, planar rated at 18 A, Asymmetrical Trench rated at 19 A, Symmetrical Double-Trench rared at 26 A, and Trench-Assisted Planar rated at 19 A. All devices have the same range of on-resistance. The body diode reverse recovery for each device is tested under different switching rates emulated by gate resistances on the switching MOSFET ranging between 10 Ω to 100 Ω in room temperature to enable evaluation of their performance under different switching rates. The trends of reverse recovery at room temperature for gate resistances of 10 Ω & 100 Ω is shown in Fig. 2, while the performances of different device technologies are compared with the charges calculated as shown in Fig. 3. The measurements indicate that the Planar SiC MOSFET and Trench-Assistant Planar MOSFET exhibit swift reverse recovery and lower peak reverse recovery currents at room temperature, while the SiC Symmetrical Double-Trench MOSFET show slightly higher peak currents.

As temperature increases, the carrier lifetime extends, resulting in longer reverse recovery times. Different MOSFET structures have different sensitivities to the changes in temperature. The SiC Planar MOSFET and the Trench Assisted Planar MOSFET exhibit very short reverse recovery periods and lowest peak reverse recovery currents at room temperature, while the SiC Symmetrical Double Trench MOSFET shows slightly higher peak currents, and the SiC Asymmetrical Trench MOSFET shows the highest. However, as temperature increases to 75°C, and then further followed to 175°C, as shown in Fig. 3, the SiC Asymmetrical Trench MOSFET maintains a relatively stable peak reverse recovery current while other devices show significantly deteriorated reverse recovery especially in the case of the SiC Symmetrical Double-Trench MOSFET.

The temperature dependence of the reverse recovery charges of different gate resistances under temperature 25°C and 175°C are also calculated as shown in Fig. 4. The reverse recovery charges of the Planar and Trench-Assisted Planar are close under different temperatures. The Asymmetrical Trench are less sensitive to the change of temperatures, while the Symmetrical Double-Trench devices are more sensitive to the temperature variations especially at higher temperatures. This indicates the effect of the deepen P-well in the structure which provide more carriers to be removed during the reverse recovery.

The above experimental results highlight the importance of considering both thermal dynamics and device architecture in SiC MOSFET performance. The varying impacts of temperature on different devices emphasize the need for further research.

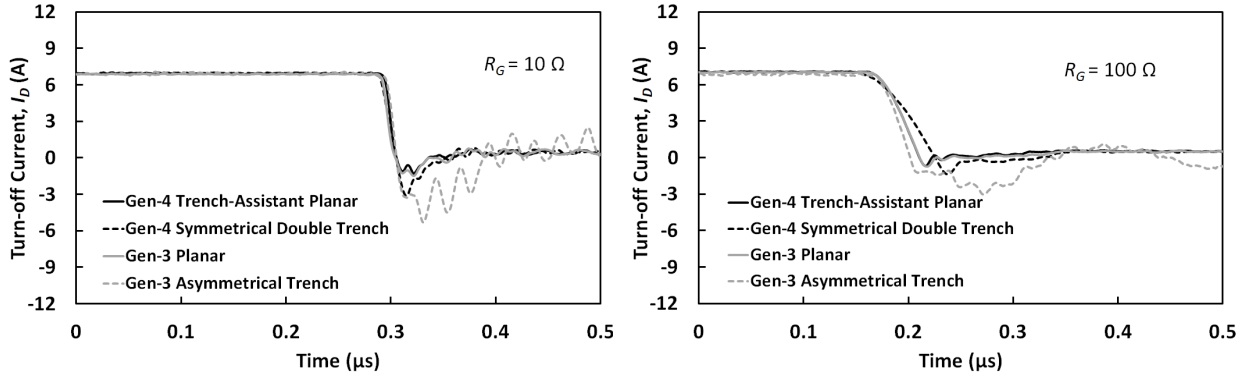


Fig. 2. Reverse recovery trends at room temperature with R_G of 10 Ω and 100 Ω.

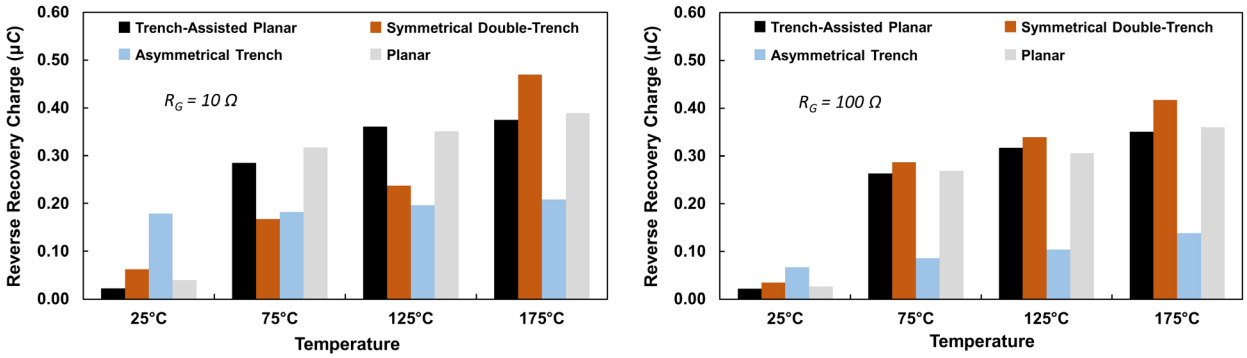


Fig. 3. Reverse recovery charges with temperature from 25°C to 175°C with R_G of 10 Ω & 100 Ω.

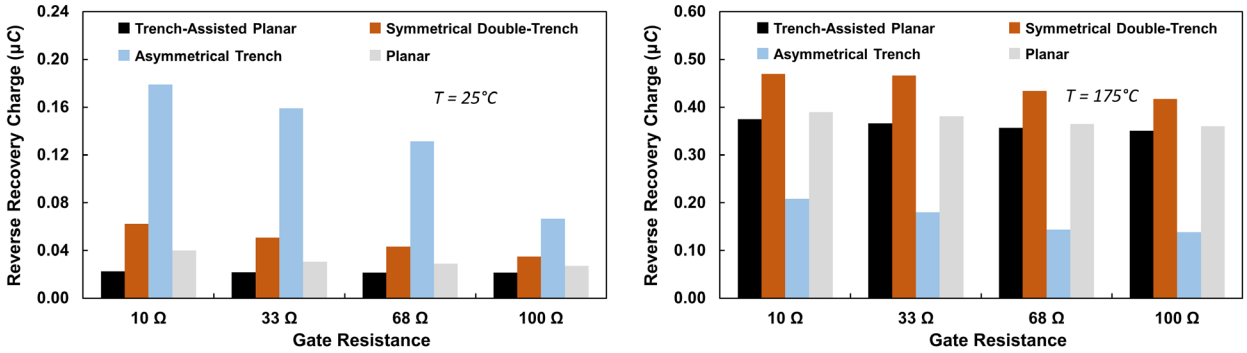


Fig. 4. Reverse recovery charges with temperatures 25°C & 175°C with R_G between 10 to 100 Ω.

Evaluation of Degradation

Bipolar degradation in a MOSFET's body diode occurs due to the existing Basal Plane Dislocation (BPD) in growth, formed during the device fabrication. BPDs can expand during device operation, especially under high current conditions, leading to Shockley Stacking Faults (SSFs) which will result in higher on-state resistance.

According to [11-14], bipolar degradation can be fully developed even in relatively short time span if under adequate electrothermal stress in converter operation. To investigate the development of bipolar degradation in different structures of SiC power MOSFETs, constant current stress are conducted on the body diode of DUTs for 8 hours with increasing levels of electrothermal stress with the test board shown in Fig. 5. The real-time V_{SD} are logged using the Tektronix MDO34 oscilloscope. The change of V_{SD} indicates the change of the on-state resistance of body diode. It is noted that during the test, the temperatures are controlled by a temperature controller to prevent thermal runaway. All data is collected only after the temperature of MOSFETs reach steady state. During the tests, the temperature of devices are monitored using FLIR E5 thermography camera.

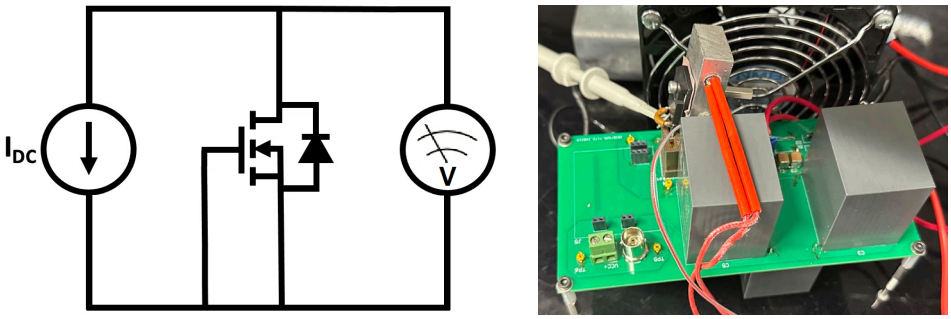


Fig. 5. Test set up for analysis of bipolar degradation mechanisms under continuous current stress.

The logging data of devices under different current stresses of 3 A, 6 A and 8 A are compared in Fig. 6. The difference in large-scale is negligible, given the level of electrothermal stress applied, however, zooming indicate the staring trends of degradation which could cascade if the stress time is further prolonged. It is important to note that the bipolar degradation level and process could vary among the different samples of the same structure and manufacture [13], as it is also dependent on the BPDs that are formed during the fabrication process. More detailed performances of different devices under various current stresses are discussed below.

Firstly, devices are tested under 3 A for 8 hours. Slight increasing trends can be found in Planar, Asymmetrical Trench, and the Trench-Assisted Planar, while the V_{SD} of Symmetrical Double-Trench remains stable throughout. This indicates that under lower current, the development of degradation is slow.

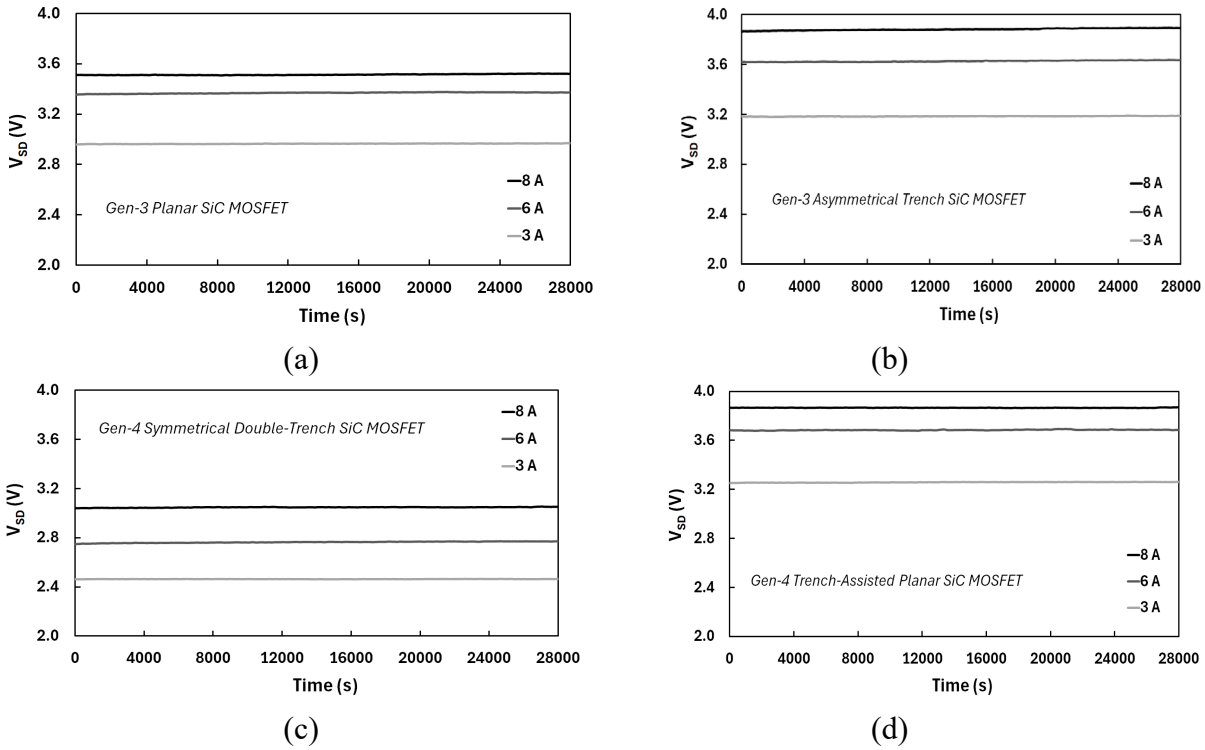


Fig. 6. Comparisons under different current stresses: (a) Planar; (b) Asymmetrical Trench; (c) Symmetrical Double-Trench; and (d) Trench-Assisted Planar.

To further investigate the rate of degradation under different stresses, the continuous current is increased to 6 A. The V_{SD} of the devices are shown in Fig. 7, Fig. 8, Fig. 9 and Fig. 10 together with the IV characteristics. The measured temperatures that was monitored during the tests. A consistently increasing trend occurs at the start of the test for Planar and it keeps increasing gradually for approximately 4 hours, which indicates the gradual development of initial stages of SSFs. After that, V_{SD} remains relatively stable until the test is ceased. The temperature of device is controlled around

100°C. Different from the continuous increase of the Planar, V_{SD} of Asymmetrical Trench remains stable at the first 3 hours with the temperature 108°C. Afterwards, it keeps increasing gradually for 4 hours. This indicates a small step change, followed by a stable state. In the Symmetrical Double Trench, it is observed that V_{SD} begins to rise after the temperature reaches 86°C and remains steady, which could correspond to the initial expansions of BPD defects. The increasing trend last for 6 hours. More specifically, increasing slope in the first hour is relatively larger and then V_{SD} remains stable for a short period, followed up by a gradual long increasing process. This suggests that even under the same current stress, the development speed of BPDs can vary. As for the Trench-Assisted Planar, there is no obvious increasing trend or abrupt increase while V_{SD} remains relatively stable throughout the test.

The I-V characteristics are compared for before and after the tests. Through local amplification it can be found that the on-state resistances increase slightly. Nevertheless, the difference between fresh and stressed devices are still very small. It must be noted that to prevent the spontaneous turn-on of the device, the gate and source terminals of the device are short-circuited to each other through hard-wiring. Nevertheless, as the gate voltage is not negative, the potential role of channel conduction in third quadrant must be observed.

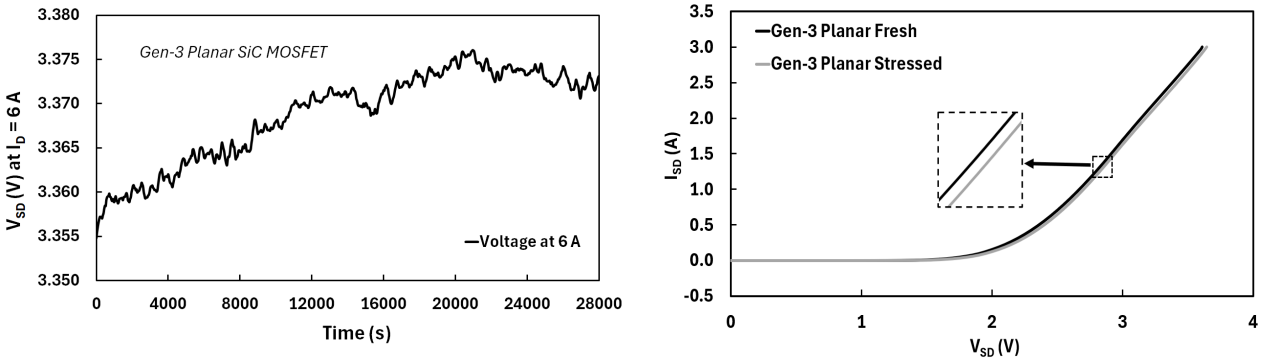


Fig. 7. V_{SD} of Planar under continuous DC current stress 6 A and comparisons of I-V characteristics of body diode before and after the test.

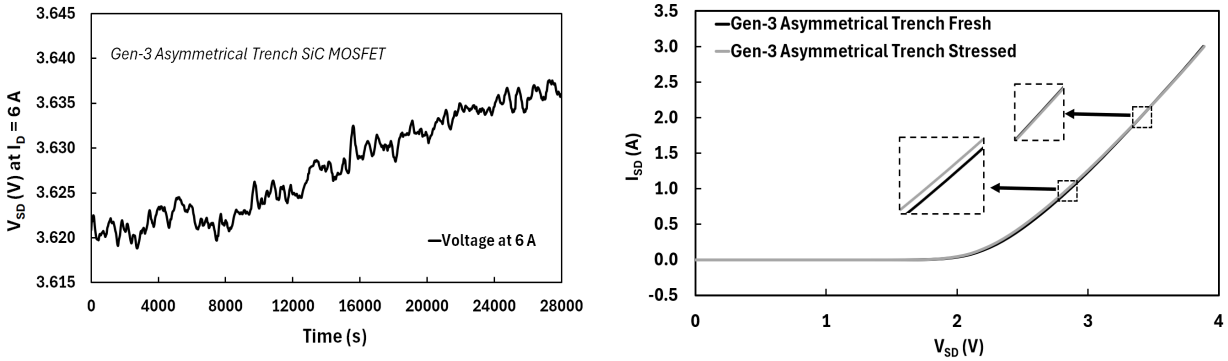


Fig. 8. V_{SD} of Asymmetrical Trench under continuous DC current stress 6 A and comparisons of I-V characteristics of body diode before and after the test.

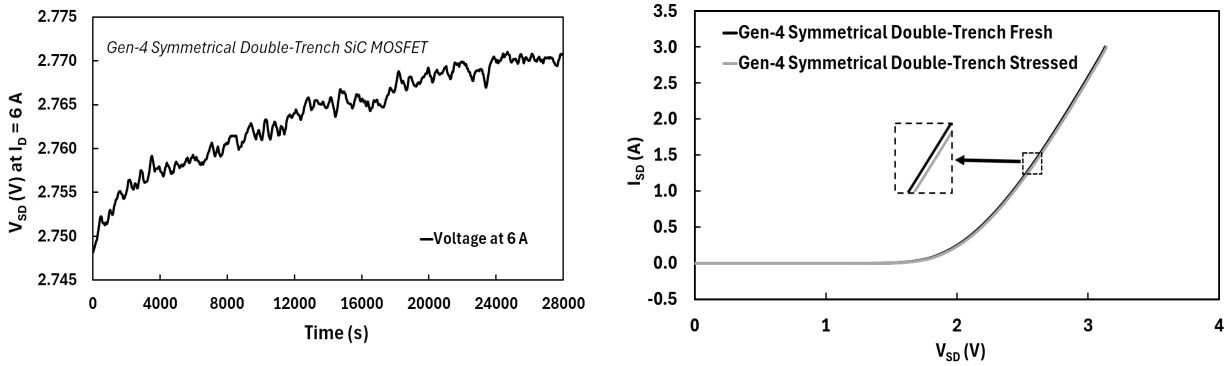


Fig. 9. V_{SD} of Symmetrical Double Trench under continuous DC current stress 6 A and comparisons of I-V characteristics of body diode before and after the test.

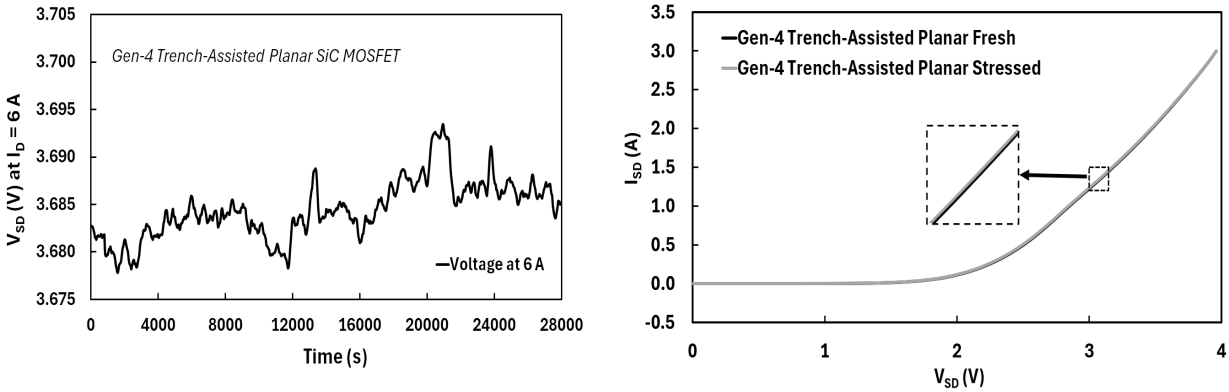
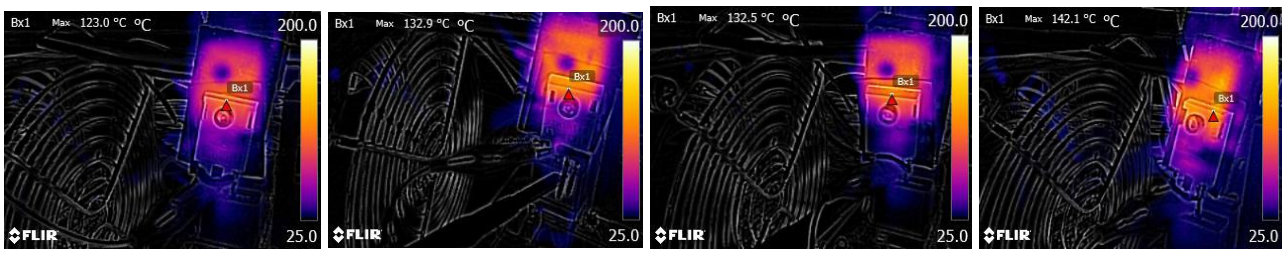


Fig. 10. V_{SD} of Trench-Assisted Planar under continuous DC current stress 6 A and comparisons of I-V characteristics of body diode before and after the test.

The observation in Figures 7 to 10 is just the beginning of any potential degradation, with 6 A current at only 8 hours. To observe actual degradations, both the current and time period of stressing of the device must be increased. This is expected to lead more deviations in the IV.

To promote further electrothermal stress, the current is further increased to 8 A to apply additional stress on the devices and check if the initiation of any BPD defects will change. The temperatures under steady state are shown in Fig. 11 while the logging data are shown in Fig. 12. The outer temperatures of devices are all above 120°C while the maximum operating temperature is about 175°C for all devices. From the Fig. 12 it can be seen that the Planar remains stable for 4 hours and then increases gradually. As for the Asymmetrical Trench, two step increase can be found. And the second formation of BPD defect is obviously quicker than the first one, which happened after 5 hours. Only one step increase can be found in the Symmetrical Double-Trench device and the Trench-Assisted remains stable through the test.



(a) (b) (d) (d)

Fig. 11. Thermal images of DUTs during the 8A DC stress test: (a) Planar with T_{max}=123.0°C; (b) Asymmetrical Trench with T_{max}=132.9°C; (c) Symmetrical Double-Trench with T_{max}=132.5°C; and (d) Trench-Assisted Planar with T_{max}=142.1°C.

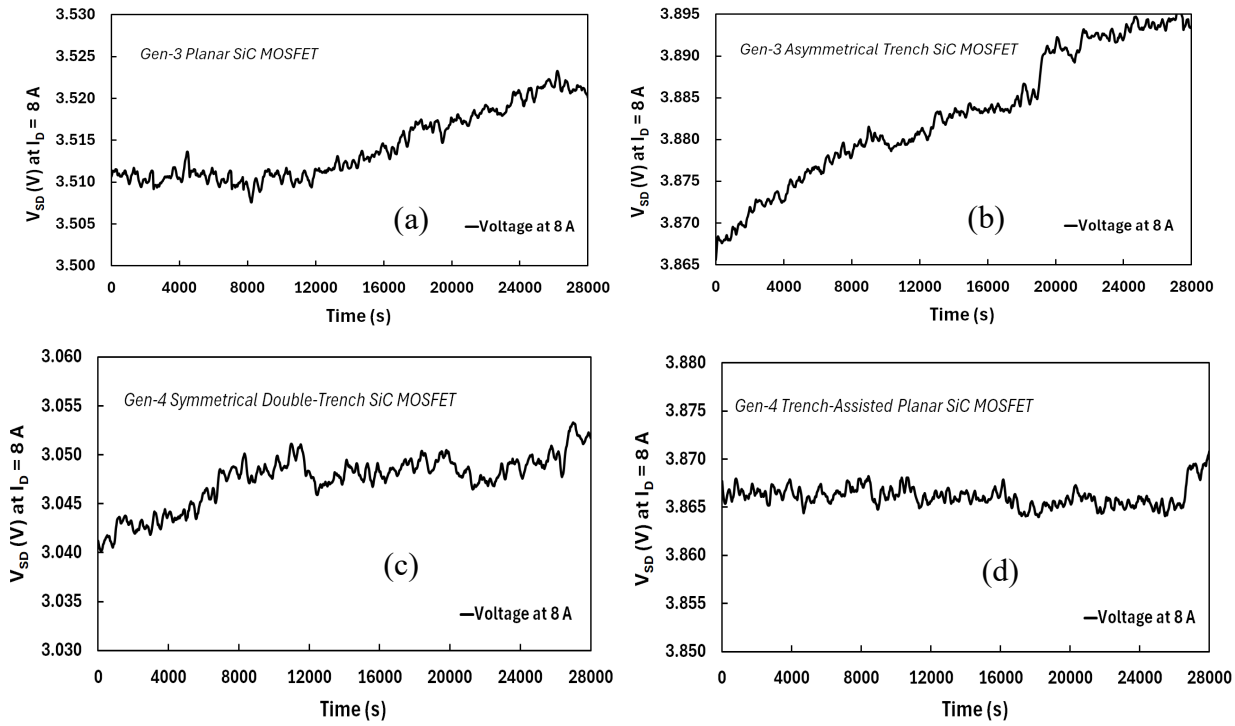


Fig. 12. V_{SD} of four structures in continuous DC current stress of 8A: (a) Planar; (b) Asymmetrical Trench; (c) Symmetrical Double-Trench; (d) Trench-Assisted Planar.

To gain a better understanding of mechanism of degradation, a 3C-layer as 50% of total cell width is inserted in the structure of different SiC MOSFETs at different depths, including 4 μm, 6 μm, 8 μm and 10 μm in the models developed in Silvaco TCAD in Fig. 13. The different locations of defect do not lead to an obvious change in I-V characteristics, indicating that the location of the defect has low impact on the overall increase of on-state resistance, though local amplifications of current density can be observed. More research is required to investigate the impact of the defect density, location and severity on amplification of the degradation effects in trench SiC devices.

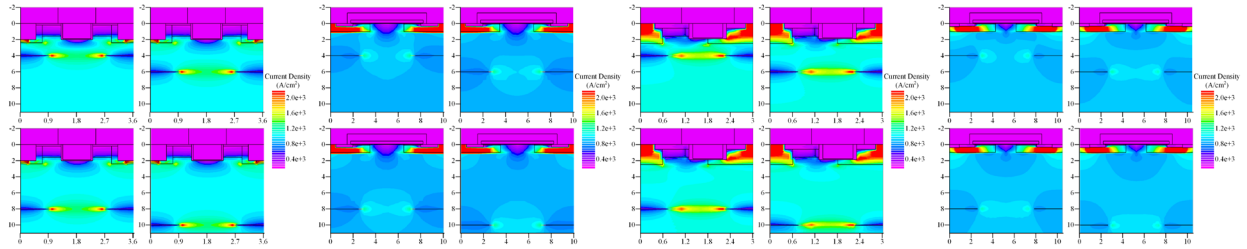


Fig. 13. The cross-sectional views of current densities of, (a) Symmetrical Double-Trench, (b) Planar, (c) Asymmetrical Trench, and (d) Trench-Assisted Planar gate SiC MOSFETs with a 3C-layer at 50% of total cell width inserted in depths of 4 μm, 6 μm, 8 μm and 10 μm.

Conclusion

In this paper, the 3rd quadrant operation and the effects of bipolar degradation of the Gen-3 and Gen-4 SiC MOSFETs are studied. In the 3rd-quadrant measurements, the Gen-4 devices show more variations in responses to temperature changes in terms of reverse recovery characteristics compared to Gen-3 devices. In terms of initiation of bipolar degradation, it can be seen that the Symmetrical Double-Trench SiC MOSFET starts to exhibit some signs of bipolar degradation similar to the devices, while the Trench-Assisted Planar MOSFET maintains a very stable performance throughout the tests. Although these findings highlight the impact of different structures on the temperature

response and reliability of MOSFET body diodes, and the fact that electrothermal stress can initiate some bipolar degradation, the observed variations are still too small for conclusive conclusions on the exact scope of degradation in long term operations. Based on this study, further measurements are required likely in range of 100+ hours of operation to cascade the SSF and BPD faults to the extent that degradation would be observable.

Acknowledgements

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