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Optimizing 1.2 kV SiC Trench MOSFETs for Enhanced Performance and Manufacturing Efficiency

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Abstract. This paper presents the development and optimization of a 1.2 kV Silicon Carbide (SiC) Trench MOSFET with a Bottom P-well (BPW), designed to achieve a compact structure and a simplified fabrication process. By performing the BPW implant before the trench etching process and utilizing it in conjunction with a shallow trench, the process complexity was reduced while maintaining effective corner coverage of the trench gate. Comprehensive simulations and unit process analyses were conducted to evaluate the effects of the hard mask sidewall angle, P-well, and JFET implant doses on device characteristics. Optimal performance was achieved by introducing an additional P+ implant in the P-well region, which significantly enhanced breakdown voltage without affecting channel properties. The optimized device demonstrated a specific on-resistance ($R_{on,sp}$) of 2.2 m$\Omega \cdot cm^2$, a breakdown voltage (BV) of 1600 V, and a threshold voltage (V_{th}) of 3 V, with potential further reductions in $R_{on,sp}$ through substrate thinning.

Introduction

Silicon Carbide (SiC) Trench MOSFETs have attracted significant attention due to their inherent scalability, leading to high cell densities and a high mobility plane, which result in low channel resistance—especially advantageous for voltage ratings of 1200 V or less. The key feature of the SiC Trench MOSFET structure is the formation of a deep P-region to protect the trench corners. This can be achieved by epitaxial regrowth after implantation [1], etching followed by implantation through the etched region [2], or high-energy deep aluminum (Al) implantation [3].

Recently, trench structures have been developed in more sophisticated ways, featuring extremely narrow cell pitches [4], the use of multiple epi-regrowth techniques [5], and 3D designs [6] to optimize the trade-off between on-resistance (R_{on}) and the electric field at the oxide more efficiently. Many of these advanced structures have been developed by Integrated Device Manufacturers (IDMs) or laboratories with internal process development and integration capabilities.

Developing a complete process flow for trench structures from ground up is a time-consuming, costly, and challenging endeavor, especially when working with fabrication facilities that lack support for trench process design kits. This is because the technologies mentioned above require multiple process development steps, in addition to developing the trench module process (etching, rounding, oxidation, etc.), which are not necessary for the basic SiC planar MOSFET process. Therefore, it is highly desirable for device engineers to design a simple trench structure that lowers the barriers to adoption for fabrication facilities.

Our objective is to create a 1.2 kV SiC Trench MOSFET structure with the simplest possible process flow and validate its feasibility through TCAD simulations and unit process fabrication. This paper introduces the novel concept and fundamental characteristics of a compact 1.2 kV SiC Trench

MOSFET featuring a Bottom P-well (BPW), illustrating its optimization using process parameters derived from unit process development. The proposed device is characterized by a shallow trench structure with a BPW that can be implemented through conventional ion implantation, eliminating the need for a multi-MeV ion implanter.

Device Design and Process Flow of the Proposed Device

Fig. 1(a) illustrates a 1.2 kV SiC Trench MOSFET with a BPW implemented through TCAD process simulation (Synopsys Sentaurus). The P+ source contacts are intermittently placed in the orthogonal direction to reduce the cell pitch. The easiest way to think of forming a BPW is to have an Al implant on the bottom of a trench. Forming a BPW on the etched bottom after trench etching offers the advantage of utilizing the etched depth to create a deep P-region with a low-energy implant. Additionally, the self-aligned process ensures there is no misalignment between the gate trench and the BPW. However, in this case, the BPW width is typically not wide enough to fully cover the trench corners, and several process-related factors must be considered, including the formation of hard masking when implanting after etching, and surface protection during activation annealing of the etched side. Therefore, to streamline the fabrication process, we decided to first perform all implantations (JFET, JTE, BPW, P-well, N+, P+), activate them, and then proceed to etch the gate trench, as shown in Fig. 1(c). By completing all implantations and activation prior to trench etching, we were able to leverage the already established planar MOSFET implant module process.

For the effective BPW formation, the Al implant needs to be deep enough to cover the trench gate corners. We limited the Al implant energy to a reasonably high value, with a maximum of 1.1 MeV. As a result, the peak depth of the BPW is around 1 μm, which sufficiently covers the relatively shallow 0.9 μm trench corners, as shown in Fig. 1(b). The use of a 1.1 MeV Al implant,

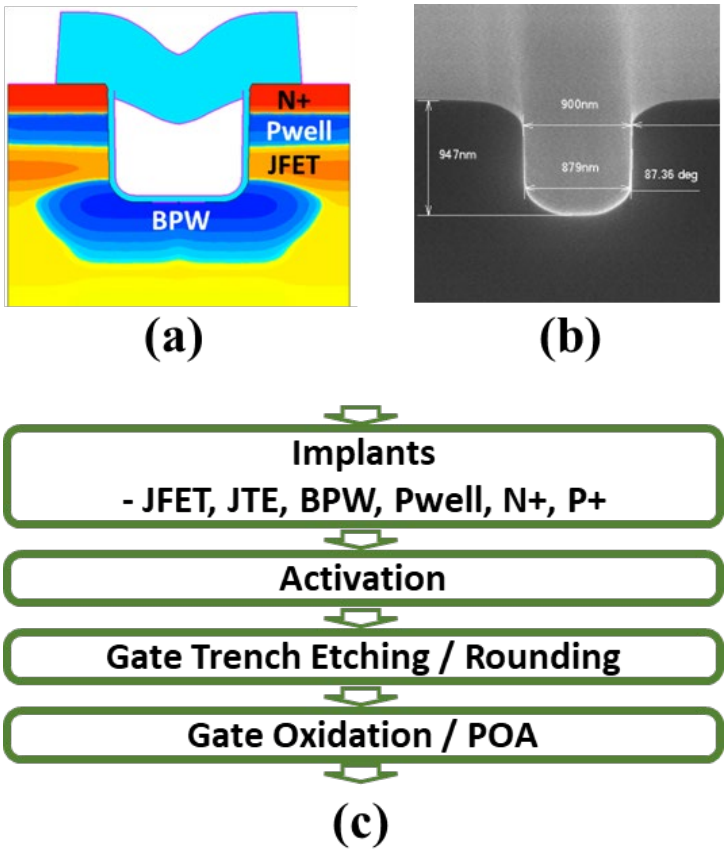

Fig. 1. (a) Cross-sectional view of the SiC Trench MOSFET with Bottom P-well (BPW) by TCAD process simulation. (b) SEM cross-section image of the etched SiC wafer followed by rounding process. (c) Brief process flow from Implantation to Gate oxidation.

resulting in a 1 μm-deep BPW, makes the MOSFET structure vertically compact. Additionally, the design avoids extra structures on each side, such as a deep P-well or source trench [7]. The BPW is much wider than the gate trench to fully cover the trench corners—even in the case of misalignment—and to block the high bias from the bottom in the OFF state. This also makes the structure horizontally compact.

To effectively arrange the N+ / P-well / JFET / BPW regions in a vertically and horizontally compact manner, the N-type doping concentration in the JFET region must be high enough to prevent pinch-off. However, an excessively high N doping concentration in the JFET region would lower the breakdown voltage (BV), necessitating careful optimization of the process.

Results and Discussion

The simulated electrical properties of this structure are presented in Fig. 2. We simulated the specific on-resistance ($R_{on,sp}$), threshold voltage (V_{th}), and BV as functions of the total dose of P-well and JFET implants. The compact structure needs to ensure stable blocking performance by maintaining sufficient Al doping concentrations in the P-well while also achieving low on-state resistance with adequate N doping concentrations in the JFET region.

We set the maximum total P-well dose at 2.84E13 cm^{-2} and then tested reduced doses. The total JFET dose was varied from 1.31E13 to 2.45E13 cm^{-2}. At a total JFET dose of 1.31E13 cm^{-2}, the JFET region is completely pinched-off, resulting in a very high $R_{on,sp}$. As the JFET dose exceeds 1.5E13 cm^{-2}, $R_{on,sp}$ typically falls below 2.4 mΩ·cm² under most conditions, despite the structure having a very narrow JFET region for current flow. This is due to the high JFET doping concentration, which exceeds 1E17 cm^{-3}.

However, lower BV is observed when a high JFET dose is combined with a P-well concentration below 80%. The optimized conditions were found with a JFET dose of 1.5E13 cm^{-2} and a P-well dose at 80%, resulting in an $R_{on,sp}$ of 2.4 mΩ·cm², a BV of approximately 1600 V, and a V_{th} of 5-6 V.

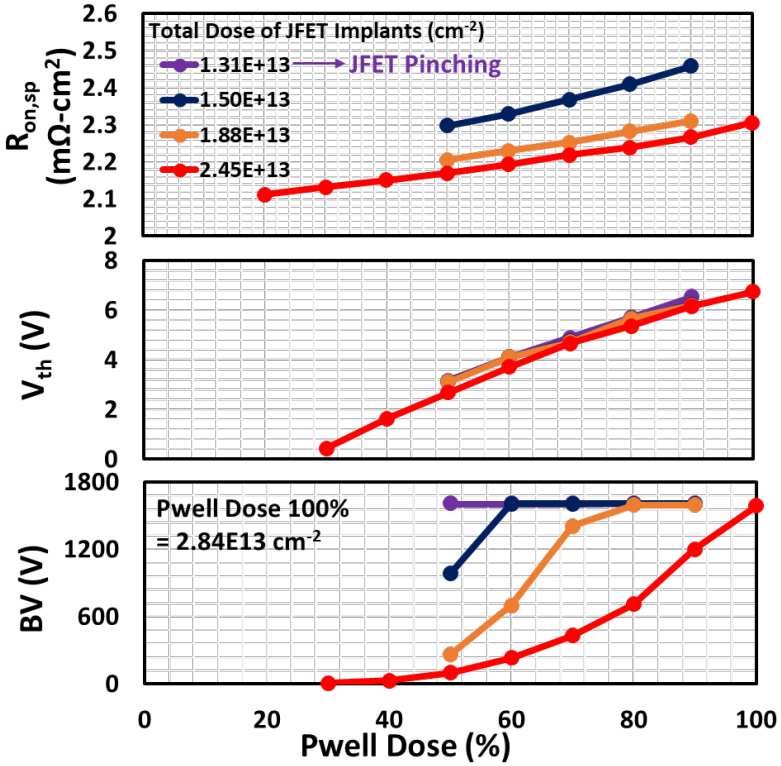

Fig. 2. Simulated specific on-resistance ($R_{on,sp}$), threshold voltage (V_{th}), and breakdown voltage (BV) of the SiC Trench MOSFET. Total JFET dose and total P-well dose were validated for different split.

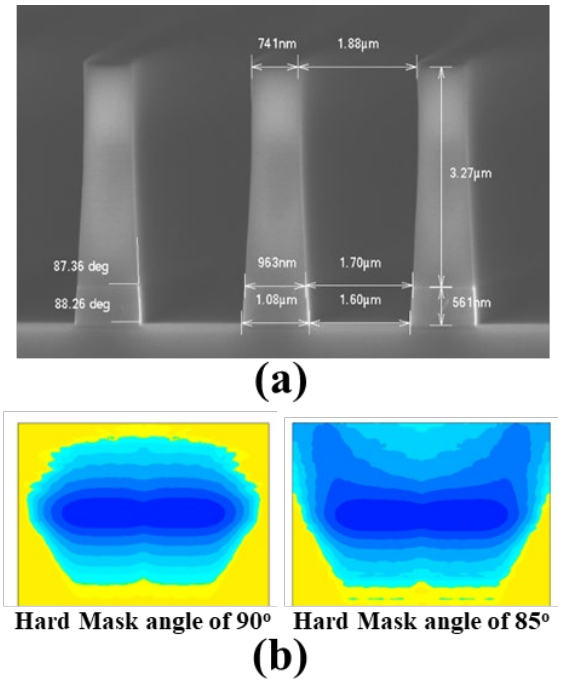

Fig. 3. (a) SEM cross-section image of the fabricated 3.8 um thick hard mask for the BPW implantation. (b) BPW implant profiles from the process simulation with the hard mask angle of 90° and 85°.

For the 1.1 MeV Al implant to form a BPW region, a relatively thick oxide hard mask is required. The sidewall angle of the hard mask affects the implant profiles, making it crucial to investigate the impact of the hard mask angle on device performance. To block the 1.1 MeV Al implant, a 2.6 µm hard mask is sufficient, but to accommodate a wider range of BPW depths, we developed a 3.8 µm-thick hard mask (Fig. 3(a)) and examined its impact on the BPW implant profile using TCAD process simulation.

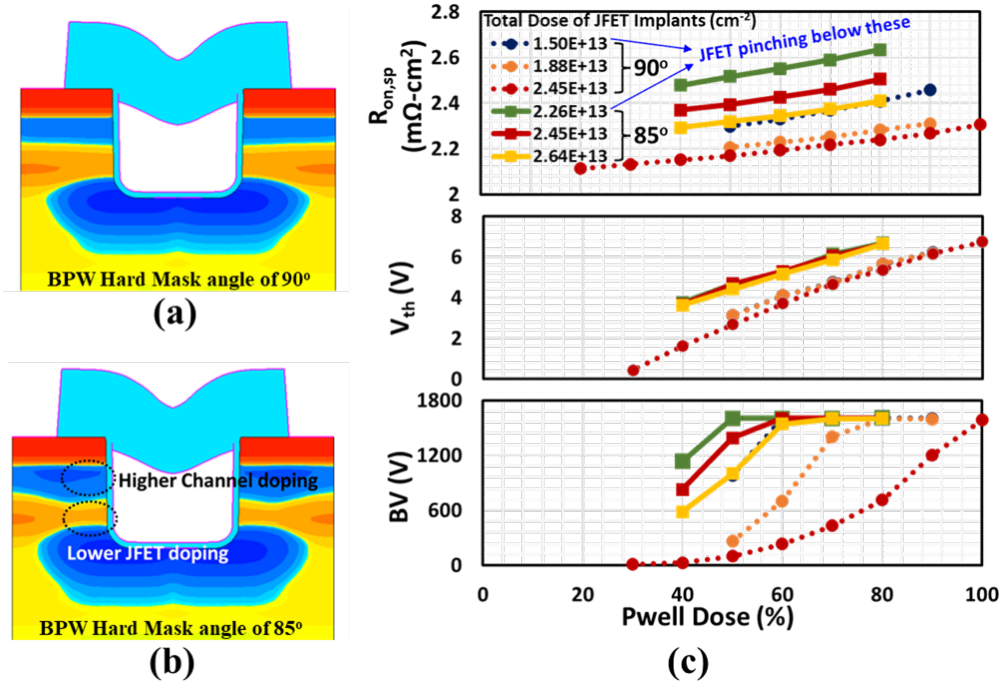

Fig. 4. (a) Simulated cross-sections of the SiC Trench MOSFET with the BPW hard mask angle of (a) 90° and (b) 85°. (c) Simulated Ron,sp, Vth, and BV of the devices with the hard mask angle of 90° and 85°. Various JFET and P-well dose splits were tested.

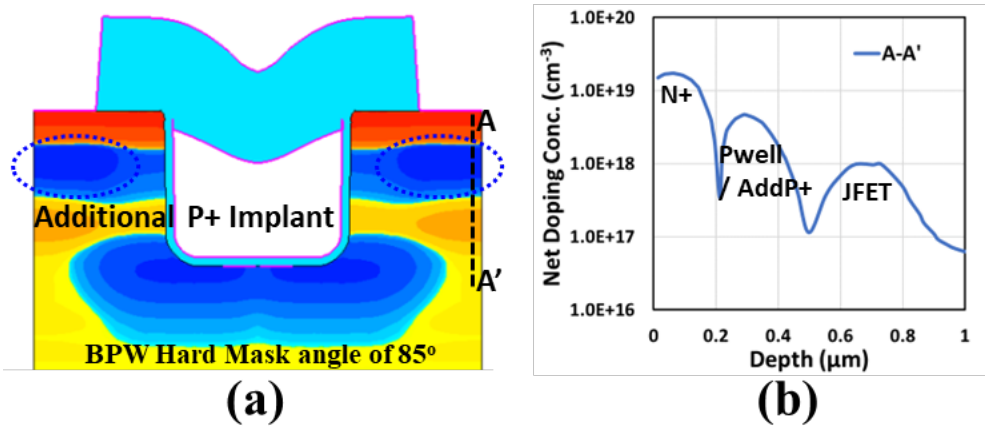

Fig. 5. (a) Cross-sectional view of the proposed SiC Trench MOSFET. P-doping in the P-well region is enhanced by the additional P+ implant. (b) Net doping concentration profile across the additional P+ enhanced region.

As shown in Fig. 3(a), the SEM analysis of the fabricated hard mask revealed an average angle of 87°. However, when simulated with TCAD process simulator, we assumed an 85° angle to account for potential process variations. As illustrated in Fig. 3(b), the 85° hard mask results in a noticeable Al upward tail compared to the 90° case, which could significantly affect device performance.

Simulation results show the impact of this process variation on device characteristics, as illustrated in Fig. 4. Compared to the 90° case (Fig. 4(a)), the upward Al tail caused by the 85° hard mask angle increases the Al concentration in the channel region (Fig. 4(b)), reducing the JFET width and the net N doping concentration. As a result, the overall V_{th} is elevated, and the $R_{on,sp}$ also increases. However, the overall BV is improved across the tested P-well dose range.

Thus, the optimization process should prioritize lowering the P-well doping concentration and increasing the N concentration in the JFET region to achieve reasonable $R_{on,sp}$ and V_{th}. However, constraints from reach-through effects due to weak P-well doping in combination with excessive N concentration must also be considered. The optimized conditions result in an $R_{on,sp}$ of 2.6 mΩ·cm², a BV of approximately 1600 V, and a V_{th} that is too high, exceeding 6 V.

To address performance trade-offs, we introduce an additional P+ implant in the P-well region on either side of the device, where reach-through occurs, to enhance the Al concentration (Fig. 5). We added a single Al implant positioned at an appropriate distance from the gate trench. If placed too close to the channel region, it could affect the Vth and channel resistance. While this additional P+ structure may require a new mask layer, it is possible to share the contact source mask to simplify the process.

The addition of the P+ implant dramatically improves device performance, as summarized in Fig. 6. When comparing the structure without the added P+ to the one with the added P+, for a JFET total dose of 2.45E13 cm^{-2}, there is no alteration to the channel concentration, thus maintaining the same $R_{on,sp}$ and V_{th}. However, the BV margin significantly increases due to the prevention of reach-through. As a result, the P-well dose can be reduced to 20% or less without causing reach-through, allowing for a further increase in the JFET concentration, thereby reducing $R_{on,sp}$.

For a JFET total dose of up to 3.55E13 cm^{-2}, the BV is maintained, and the avalanche breakdown occurs at the bottom of the BPW. The optimized performance with the proposed enhanced P+ doping yields an $R_{on,sp}$ of 2.2 mΩ·cm², a BV of 1600 V, and a reasonable V_{th} of 3 V. The maximum electric field of the gate oxide at a drain voltage of 1200 V remains sufficiently low, around 1.6 MV/cm. It is important to note that this simulation was conducted with a 350 µm substrate; therefore, if substrate grinding is accounted for, $R_{on,sp}$ could be as low as 1.8 mΩ·cm².

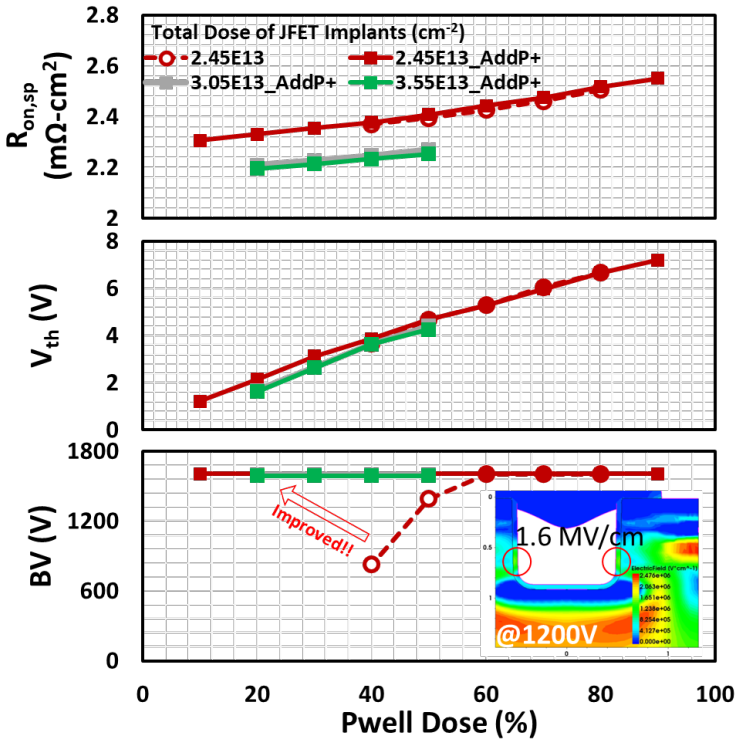

Fig. 6. Simulated Ron,sp, Vth, and BV of the proposed SiC Trench MOSFET. The results for the device without additional P+ implants are plotted for the reference. The maximum electric field at the gate oxide was measured to be 1.6 MV/cm when drain voltage was 1200 V as shown in the inset.

Summary

In this study, we developed and optimized a 1.2 kV SiC Trench MOSFET with a Bottom P-well (BPW), focusing on achieving a compact device structure with a simplified process flow. By performing the BPW implant before trench etching and using it in conjunction with the shallow trench, we reduced process complexity while maintaining effective corner coverage of the trench gate. Through extensive simulations, we investigated the impact of various factors such as hard mask angle, P-well and JFET implant doses on key device characteristics, including on-resistance ($R_{on,sp}$), threshold voltage (V_{th}), and breakdown voltage (BV). To improve device performance, we introduced an additional P+ implant in the P-well region, which significantly enhanced the breakdown voltage without altering channel properties. This addition enabled the reduction of P-well dose and allowed for higher JFET doping concentrations, leading to a further reduction in $R_{on,sp}$. The final optimized structure achieved an $R_{on,sp}$ of 2.2 mΩ·cm², a BV of 1600 V, and a V_{th} of 3 V, with a gate oxide electric field of 1.6 MV/cm at 1200 V drain voltage. Further substrate grinding could reduce $R_{on,sp}$ to 1.8 mΩ·cm². These results demonstrate that the proposed design and process optimizations are effective in balancing performance trade-offs while maintaining manufacturability, making this approach highly attractive for fabricating SiC Trench MOSFETs.

Acknowledgements

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