Novel SiC MOSFET Edge-Termination Structure for Electric Field Relaxation Using an Oxide Film Along the Trench Surface

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Abstract. In this study, we investigated a trench-gate silicon carbide metal-oxide-semiconductor field-effect transistor (SiC-MOSFET) edge-termination structure using an oxide film along the trench surface to simplify the manufacturing process. The trench structure in the termination region serves as a guard ring, eliminating the need for a separate guard ring process and thereby reducing the number of process steps. To suppress electric field concentration at the edge of the cell region under high voltage, a boundary region between the cell and termination regions was implemented. Technology Computer-Aided Design (TCAD) device simulations confirmed that by using the boundary region and narrowing the mesa width, avalanche breakdown was prevented up to the breakdown voltage of the cell region.

Introduction

A trench-gate silicon carbide metal-oxide-semiconductor field-effect transistor (SiC-MOSFET) is anticipated to achieve low specific on-resistance (Ron,sp) by increasing cell density and enhancing channel mobility [1]. We previously reported a 1.2 kV class trench-gate SiC-MOSFET that achieved low Ron,sp [2]. With the increasing demand for 1.2 kV class trench-gate SiC-MOSFETs in the electric vehicle market, reducing the number of process steps is crucial. Various termination structures for trench-gate SiC-MOSFETs have also been explored [3, 4]. Conventional termination structures require additional process steps to form a guard ring. In this study, we investigated an edge-termination structure using an oxide film along the trench surface. Since the trench structure in the termination region acts as a guard ring, the need for a separate guard ring process is eliminated, thereby reducing the number of process steps. Technology Computer-Aided Design (TCAD) simulations confirmed the breakdown voltage, electric field, and impact ionization characteristics of this structure.

Design and Fabrication

Figure 1 shows the schematic cross-sectional view of the edge-termination structure using an oxide film along the trench surface [5]. This structure is composed three regions: the cell, boundary, and termination regions. The color of the electrodes in the trench structure corresponds to the electrical potential. Gray electrodes within the cell region are connected to the gate potential. Light gray electrodes within the boundary region are connected to the source potential. Green electrodes within the termination region are at floating potential and are not connected to each other. In the cell region, current flows when the gate is turned on. The termination region comprises floating electrodes, an oxide film along the trench surface, and a surrounding p-type implanted layer. The lateral electric field is gradually relaxed due to the oxide film along the trench surface. In the boundary region, the gate electrode is connected to the source electrode, preventing current flow through the channel, and avoiding changes in the lateral electrostatic potential. The boundary region separates the cell and termination regions.

Figure 2 also illustrates the cross-sectional fabrication process flow of the trench-gate SiC-MOSFET edge-termination structure. (i) First, the p-type well region and n-type source region are formed by vertical Al and N implantation into the n-type drift layer using photolithography. (ii) Next, an SiO₂ hard mask for SiC trench etching is created by dry etching after SiO₂ deposition with photolithography. (iii) The SiC trench structure is then formed by dry etching using the SiO₂ hard mask. (iv) The bottom p-well (BPW) is formed by vertical self-aligned implantation into the trench bottom with the SiO₂ hard mask remaining after SiC trench etching. In conventional edge-termination structures, a resist mask must be formed by photolithography in areas where the BPW is not to be formed. However, in this structure, the BPW is used as a guard ring, eliminating the need for a resist mask, and the BPW is formed using only an SiO2 hard mask, making photolithography unnecessary and reducing the number of process steps. (v) The SiO₂ hard mask is then removed, and the p-type and n-type sidewall regions are formed by tilted Al and N implantation with photolithography, respectively. Conventional edge-termination structures require additional implantation steps involving photolithography to form edge-termination structures such as guard rings [6] or the junction termination extension (JTE) [7], but the edge-termination structure of the present invention eliminates these steps. (vi) Finally, activation annealing, gate formation, contact formation, and metallization are carried out.

By adopting this edge-termination structure, it is possible to eliminate manufacturing processes required for forming edge-termination structures such as guard rings or JTE, thereby reducing the need for multiple steps, including photolithography, etching, and cleaning. However, forming trenches in the boundary and termination regions with the same mesa width as the cell region leads to electric field concentration at the edge of the cell region, which reduces the device breakdown voltage below the cell breakdown voltage. Therefore, we explored methods to suppress the reduction in breakdown voltage.

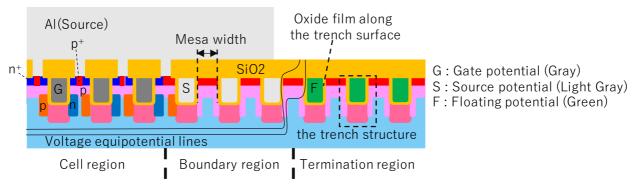


Fig. 1. Schematic of the cross-sectional view of the edge-termination structure

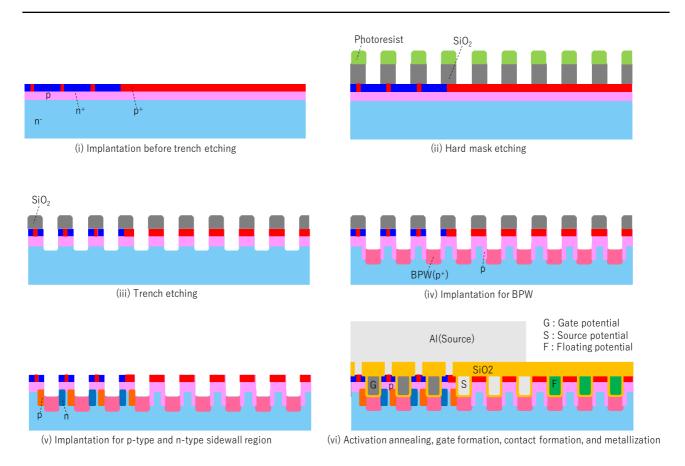


Fig. 2. Cross-sectional fabrication process flow of the trench-gate SiC-MOSFET edge-termination structure

Structure that Realizes Cell Breakdown Voltage

Figure 3 illustrates the schematic cross-sectional view of (a) the structure where the termination region is directly adjacent to the cell region and (b) the structure where the cell and termination regions are separated by a boundary region. Figure 4 shows the electric-field distribution and voltage equipotential lines for (a) and (b) when 1.35 kV is applied. The structure with a boundary region (b) suppresses the electric field at the edge of the cell region more effectively than the structure without a boundary region (a). Figure 5 presents the electric field profile at the C1 point in Figure 3 under 1.35 kV. The maximum electric field value is higher in structure (a) than in structure (b). Additionally, in structure (a), the maximum electric field occurs at the edge of the cell region, whereas in structure (b), it is located within the cell region. In the cell region, an n-type implanted layer extends to the trench sidewall to ensure a current path. A depletion layer forms in the n-type implanted layer, resulting in a higher electric field compared to the area surrounded by the p-type implanted layer [8]. In structure (a), the electric field is further concentrated due to lateral electric field relaxation [9], reducing the breakdown voltage. In structure (b), the trench structure adjacent to the cell region, where the electric field tends to concentrate, is set to the source potential. Consequently, lateral electric field relaxation begins at a point farther from the cell region, separating the electric field concentration caused by lateral electric field relaxation from that on the trench sidewalls, thereby preventing a decrease in breakdown voltage.

Figure 6 depicts the simulated breakdown voltage dependence on mesa width for structures with and without a boundary region. Structures with a boundary region exhibit higher breakdown voltages compared to those without one. This improvement in breakdown voltage is attributed to the separations of the cell and termination regions by the boundary region, which suppresses electric field concentration at the edge of the cell region.-Furthermore, reducing the mesa width further suppresses electric field concentration [10]. BPW at the bottom of the trench acts as a guard ring, if the mesa

width is reduced, the electric field that can be mitigated by a single trench structure becomes smaller. Reducing the mesa width extends the depletion layer, but it suppresses electric field concentration and increases the breakdown voltage. When the mesa width is $1.7~\mu m$ or less, the breakdown voltage matches that of the cell region. In the structure without a boundary region, reducing the mesa width can improve breakdown voltage, but it does not reach the breakdown voltage of the cell region.-For mesa width down to $1.3~\mu m$, the depletion layer does not extend to the edge of the termination region, resulting in an increase in breakdown voltage. However, when the mesa width is reduced to $1.1~\mu m$, the depletion layer reaches the edge of the termination region, causing the electric field to concentrate at the edges of the cell and termination regions, which decreases the breakdown voltage [10].

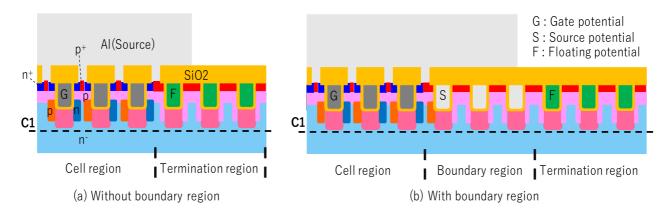


Fig. 3. Schematic cross-sectional view of structures with and without boundary region

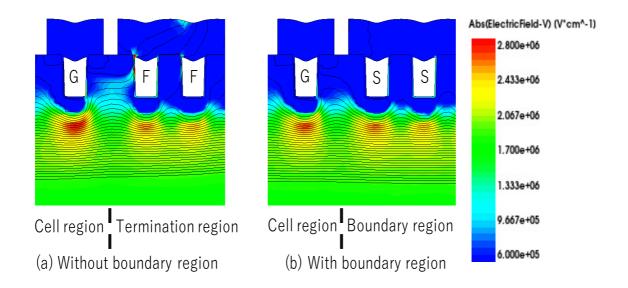


Fig. 4. Electric field distribution and voltage equipotential lines under 1.35 kV based on simulation (boundary and termination mesa width is 1.3 μm)

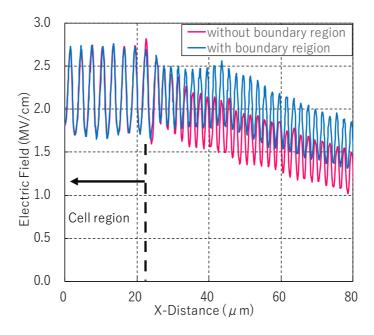


Fig. 5. Electric field profile applied at 1.35 kV at the C1 point (boundary and termination mesa width is 1.3 μm)

Figure 7 shows the impact ionization rate at the time of avalanche breakdown for mesa widths of $2.3~\mu m$ and $1.3~\mu m$ for structures with and without a boundary region. For structures with the boundary region, avalanche breakdown occurs at the edge of the boundary region with a mesa width of $2.3~\mu m$ but occurs inside the cell region with a mesa width of $1.3~\mu m$. In contrast, for structures without the boundary region, avalanche breakdown does not occur inside the cell region regardless of the mesa width. As described, achieving the cell breakdown voltage can be accomplished by reducing the mesa width and incorporating a boundary region in the edge-termination structure using an oxide film along the trench surface.

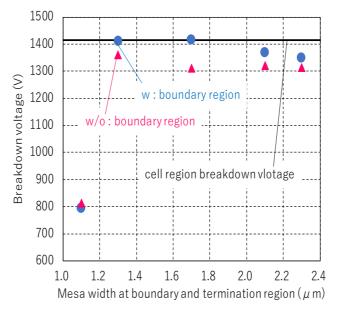


Fig. 6. Dependence of the simulated breakdown voltage on mesa width for structures with and without a boundary region (the number of trenches in the termination region is constant)

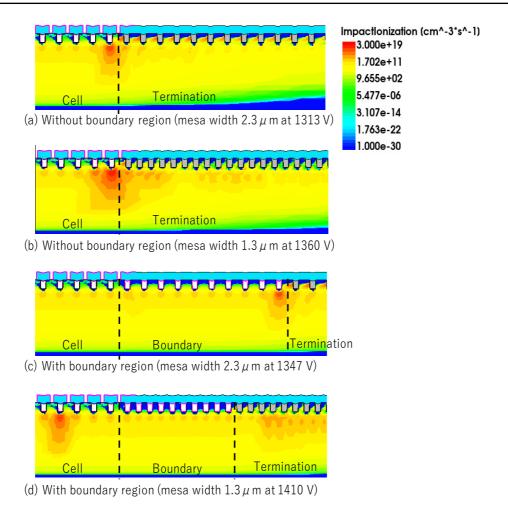


Fig. 7. Impact ionization rate at the time of avalanche breakdown for mesa widths of 2.3 μm and 1.3 μm

Summary

In this study, we conducted TCAD simulations to analyze the breakdown characteristics of the edge-termination structure using an oxide film along the trench surface. By utilizing the trench structure as a guard ring, we eliminate the need for a separate guard ring process, thereby reducing the number of process steps. Our observations indicate that with the boundary region, when the mesa width is $1.7~\mu m$ or less, the breakdown voltage of the termination region matches that of the cell region. The lateral electric field relaxation is separated from the electric field concentration on the trench sidewalls, which helps suppress the decrease in breakdown voltage. We plan further optimization the edge-termination structure and verify its robustness.

References

- [1] H. Yano, H. Nakao, H. Mikami, T. Hatayama, Y. Uraoka and T. Fuyuki, Appl. Phys. Lett. 90, 042102 (2007).
- [2] K. Sugawara, Y. Fukui, R. Tanaka, K. Adachi, Y. Kagawa, S. Tomohisa, N. Miura, E. Suekawa and Y. Terasaki, PCIM 2021, pp. 504–508.
- [3] T. Kimoto and J. A. Cooper, Fundamentals of Silicon Carbide Technology (2014)
- [4] P. Godignon, J. Montserrat, J. Rebollo and D. Planson, Mater. Sci. Forum 2022, 1062, 570–575.

- [5] Y. Fukui, K. Sugawara, R. Tanaka, H. Koketsu, H. Hatta, Y. Miyata, H. Suzuki, K. Taguchi, Y. Kagawa, S. Tomohisa and N. Miura, ICSCRM 2019, pp. 764-769.
- [6] D. C. Sheridan, G. Niu, J. N. Merrett, J. D. Cressler, C. Ellis and C. C. Tin, Solid-State Electronics 44 (2000) 1367-1372
- [7] V. A. K. Temple, IEDM Technical Digest (1977), pp. 423–426.
- [8] R. Tanaka, K. Sugawara, Y. Fukui, H. Hatta, H. Koketsu, H. Suzuki, Y. Miyata, K. Taguchi, Y. Kagawa, S. Tomohisa and N. Miura, ICSCRM 2019, pp. 770-775.
- [9] V. A. K. Temple and M. S. Adler, IEEE Transactions on Electron Devices, Vol. ED-22, pp. 910-916. (1975)
- [10] X. Deng, Y. Guo, T. Dai, C. Li, X. Chen, W. Chen, Y. Zhang and B. Zhang, Materials Science in Semiconductor Processing 68 (2017), pp. 108–113.