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SiC Schottky-Barrier Diode Without Ion-Implanted P-Type Regions

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Abstract. This paper shows results of SiC Schottky diodes fabricated without ion-implanted P-type regions. Diodes with blocking voltages up to 4,500 V are demonstrated utilizing an epitaxial P-type ring with sloped edges for the edge termination. Reverse-bias currents at temperatures higher than 60°C, and at nominal blocking voltages of 650 V, 1200 V, and 1700 V, are shown to match the theoretical values based on the two fundamental current mechanisms: tunneling and thermionic emission. In comparison to JBS and MPS diodes, the whole anode area is active, which enables homogeneous current flow and comparable isothermal characteristics without the usual wafer thinning. In addition, the non-thinned wafer results in larger thermal capacitance, allowing for higher repetitive peak surge currents for the same junction temperature within the maximum operating temperature of 175°C.

Introduction

Reverse-bias current and forward surge-current capability of SiC Schottky diodes are two important parameters that motivated a departure from pure SiC Schottky-barrier diodes (SBD). The predominant modifications in commercial SiC Schottky diodes, which address observed issues with these two parameters, include the junction barrier Schottky (JBS) diode for reduced reverse-bias current, and the merged $P^{+}N$ Schottky (MPS) diode for improved non-repetitive surge current [1]. A key feature of both structures is the integration of implanted P-type regions, with specific geometric properties, to achieve the desired forward and reverse characteristics. The P-type regions in both JBS and MPS diodes require the use of ion implantation, along with precise photolithography to achieve designed width of and spacing between the P-type regions [2].

This paper discusses a patented design and summarizes the results of a modern SiC SBD without any ion-implanted P-type regions. The following sections discuss the performance of these diodes with respect to three specific parameters: edge termination, reverse-bias current, and surge-current capability.

Edge Termination

When ion-implanted P-type regions are used for edge termination, their depth and the spacing between them can be used to reduce electric-field crowding at the edge of the diode [3]. Without ion-implanted P-type regions, an epitaxial P-type layer can be used with sloped edges to create tapered density of negatively charged acceptors with the aim of reducing the field crowding. This approach was attempted in the mid-1990's by applying a silicon-nitride mask and oxidation of the top P-type layer to create a P-type ring with sloped edges around the N-type active area of the Schottky diode [4]. However, the breakdown voltages remained below 600V. The SBD structure shown in Fig. 1 has enabled reverse-bias voltages higher than 4,500 V, as shown by the reverse-bias characteristics in Fig. 2. This was achieved by reducing the angle of the P-type ring to 12° and depositing 7.5 µm of SiO_2 as surface passivation. Figure 3 shows that this edge termination and surface passivation almost eliminated the perimeter.

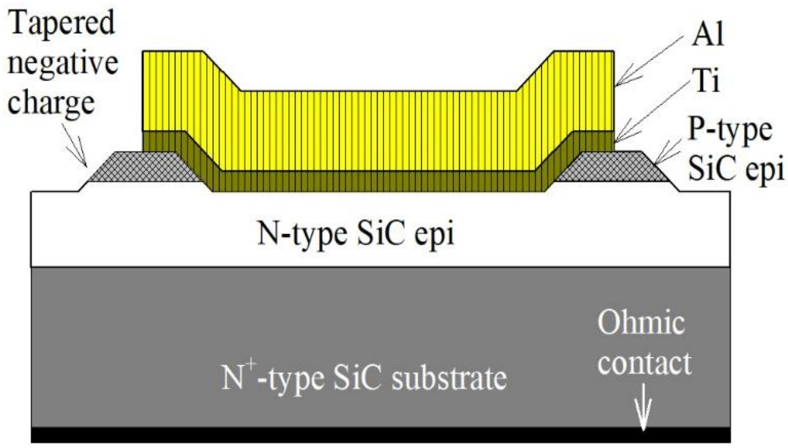

Fig. 1. Cross-section of patented SiC Schottky diode without ion-implanted P-type regions [5]. The recess etching needed to define the edge-termination ring was performed by plasma etching for all diodes reported in this paper.

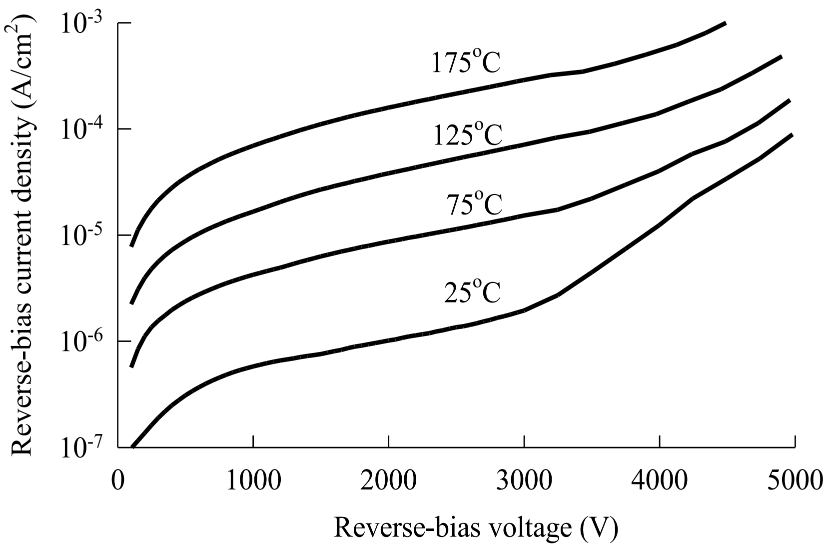

Fig. 2. Reverse bias characteristics of an SBD with the edge termination shown in Fig. 1 and with N-type drift region designed for blocking voltage of 4,500 V (N_D=1.7x10^{15} cm^{-3}, t_d=38 µm)

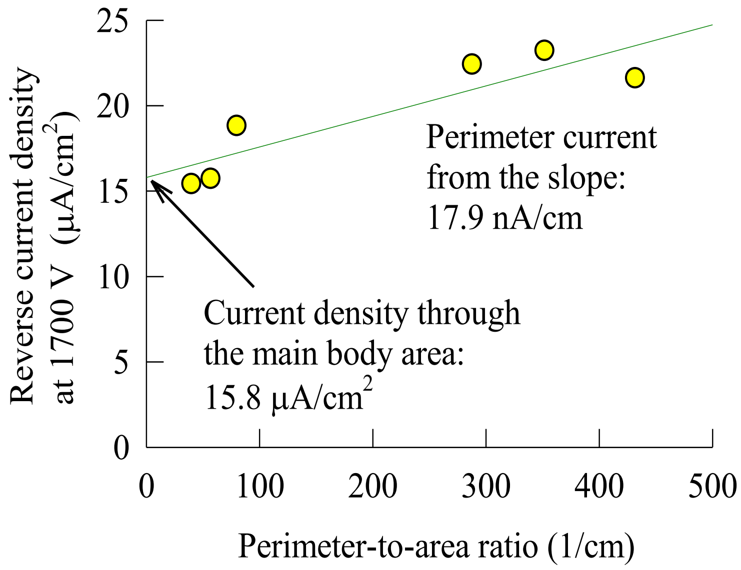

Fig. 3. Measured reverse-bias current densities (symbols) for diodes designed for 1700 V blocking voltage with different perimeter-to-area ratios. The slope of the linear-regression line shows that the perimeter current is negligible in comparison to the current through the main body.

Another important feature of the structure in Fig. 1 is that the anode metal and the P-type ring form a Schottky diode rather than Ohmic contact. The advantage of this feature is that the Schottky diode to the P-type ring is reverse biased when the main Schottky diode with the N-type drift region is forward biased. Consequently, the associated reliability issues with forward-biased P–N junctions at high current densities, resulting from carrier injections and recombination in SiC [3, 6-9], is eliminated.

Reverse-Bias Current

Implanted P-type pockets are used in JBS diodes to protect the metal–semiconductor contact by setting the maximum electric field away from the interface [1, 6]. These P-type pockets are densely spaced so that the depletion layers that they create with the N-type region are merged at high reverse voltages [1, 6]. When a JBS diode is forward biased, the current flows between the P-type pockets. This means that the active metal–semiconductor area of the diode is reduced. Figures 4, 5, and 6 show the current–voltage characteristics of SBDs with homogeneous Ti–SiC contacts in the active area, with N-type drift layers designed for three blocking voltages: 650 V (N_D =8x10^{15} cm^{-3}, t_{dr} =5.5 µm), 1200 V (N_D =5x10^{15} cm^{-3}, t_{dr} =9.5 µm), and 1700 V (N_D =4x10^{15} cm^{-3}, t_{dr} =14.5 µm). The edge termination shown in Fig. 1 was the same for all blocking voltages.

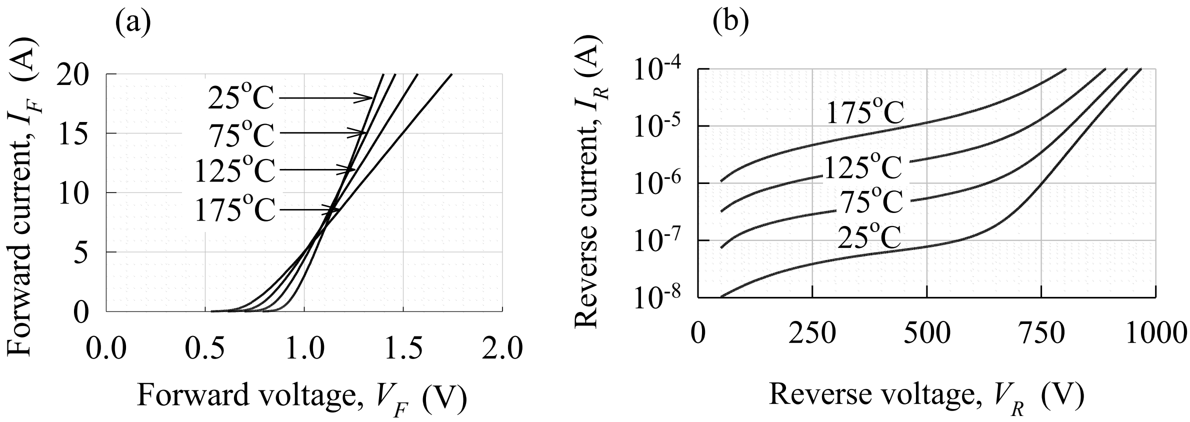

Fig. 4. Forward (a) and reverse (b) current–voltage characteristics of 650 V/20 A diode

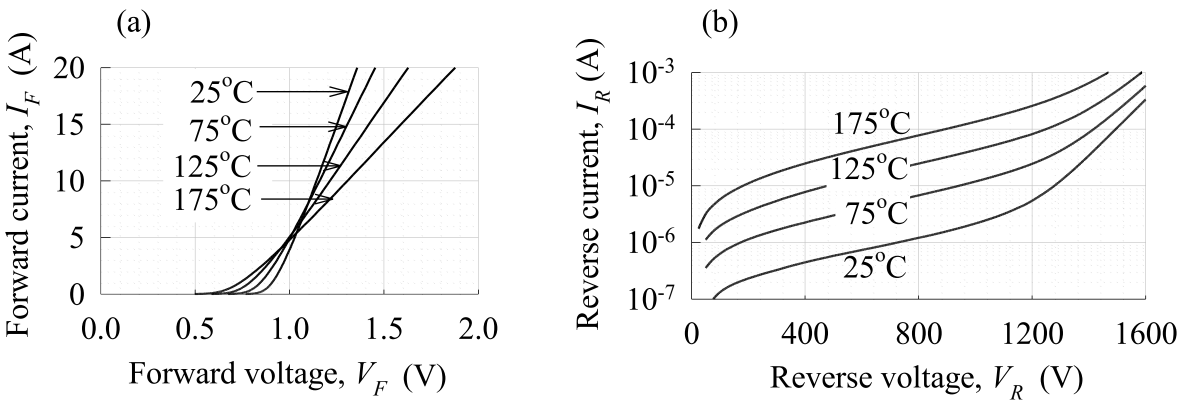

Fig. 5. Forward (a) and reverse (b) current–voltage characteristics of 1200 V/20 A diode

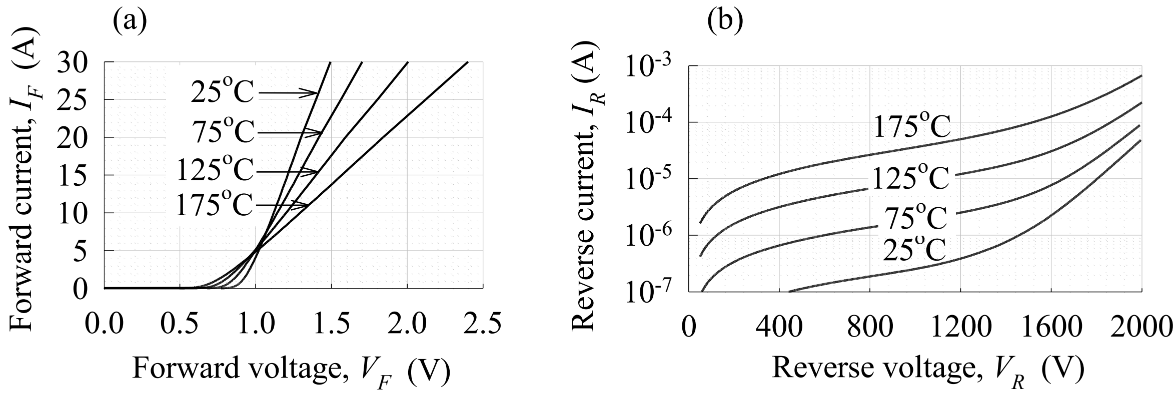

Fig. 6. Forward (a) and reverse (b) current–voltage characteristics of 1700 V/30 A diode

A study of this type of homogeneous SiC Schottky diode showed that the reverse-bias current at junction temperatures above 60ºC is due to the two fundamental current mechanisms: (1) tunneling and (2) thermionic emission [10]. Consequently, there is no diode-to-diode variation in the reverse current above 60ºC, and the measured currents match the theoretical model based on these two fundamental current mechanisms without fitting parameters [10]. Measured reverse currents at room temperature exhibit some device-to-device variation and they are higher than the theoretical currents. This indicates that the reverse currents at room temperature include variable leakages through defects at the metal–semiconductor contact, which could be a topic for a future study and confirmation.

Surge-Current Capability

The forward surge-current capability of SiC Schottky diodes is usually classified in two ways: (1) repetitive and (2) non-repetitive peak current of either 10 ms or 8.3 ms half sine waves to correspond to either 50 Hz or 60 Hz sinusoidal voltage, respectively [11-39]. The non-repetitive peak surge current is usually determined by applying single half sine wave pulses with increasing peak-current amplitudes until a diode failure [11-14], and then de-rating the peak current to about 70% of the value that causes failures. To increase the non-repetitive surge current capability in diodes utilizing ion implantation of P-type layers, P-N junctions are created with Ohmic contact to the P-type regions and with areas designed to turn on the P-N junctions when a certain forward voltage is reached. This way, both the Schottky diode and the P-N junction diodes conduct the surge current, resulting in a reduced forward voltage and a reduced power dissipation [6]. With this effect, the non-repetitive surge current of MPS diodes is typically higher than in the case of homogeneous SBD's. However, the integrated P-type regions reduce the area of Schottky contact. To compensate for the increased *on* resistance due to the reduced Schottky-contract area, the SiC substrate in both JBS and MPS diodes is thinned. In terms of thermal characteristics, this thinning reduces both the thermal resistance and the thermal

capacitance. The positive effect of the reduced thermal resistance is well established but there is a negative effect of the reduced thermal capacitance that is not well understood.
The negative effect of the reduced thermal capacitance by wafer thinning relates to the maximum junction temperature during surge-current pulses, which is relevant for the repetitive surge-current capability of Schottky diodes. To show this effect, we used the method of junction-temperature measurement during a surge-current pulse that is illustrated in Fig. 7.

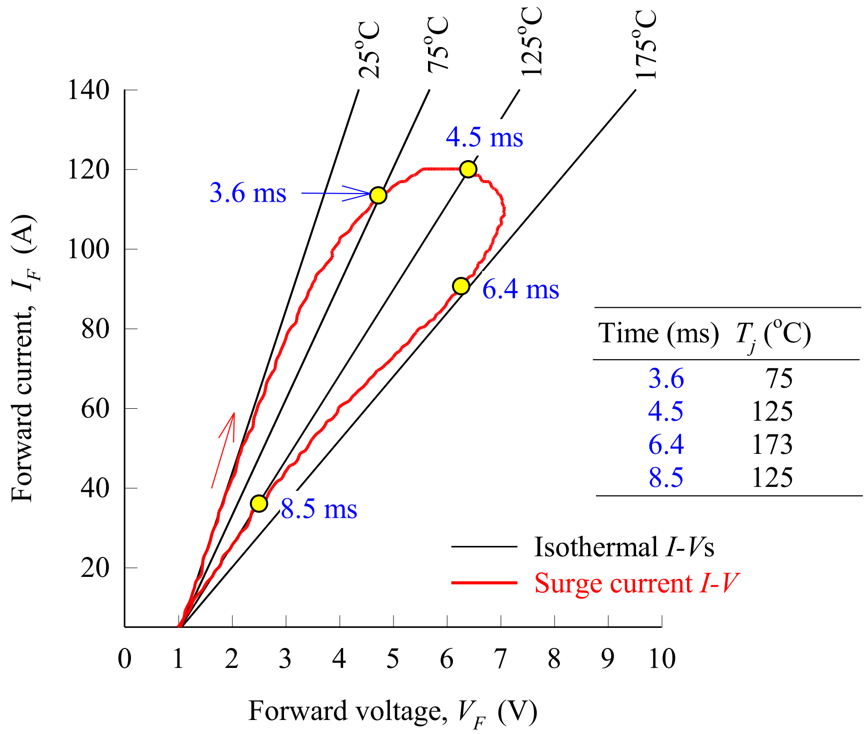

Fig. 7. Illustration of the method applied to measure the junction temperature during a surge-current pulse, T_j, by matching a surge-current *I-V* loop to isothermal *I-V* characteristics (data from [40]).

The results shown in Fig. 8 compare a commercial thinned MPS and a non-thinned homogeneous SBD, both rated at 20 A and 1200 V, for the case of a relatively small peak surge current: 80 A, which is four times higher than the nominal current. The chip areas of these two diodes are similar because the gain in Schottky-contact area due to the removal of the P-type regions in the case of SBDs is needed to compensate for the higher specific resistance of the non-thinned substrate and, therefore, to match the turn-on voltage of these diodes. Importantly, the thermal capacitance of the homogeneous SBD is about three times larger because of the larger chip thickness. The power dissipation in these diodes is also similar, given that the P-N junctions in the MPS diodes are not turned on at this surge-current level and the forward *I-V* characteristics of the turned on Schottky diodes are similar. The difference is due to the larger thermal capacitance of the non-thinned homogeneous SBD, which absorbs the dissipated heat at lower junction temperatures, as shown in Fig. 8 and analyzed in detail in [40].

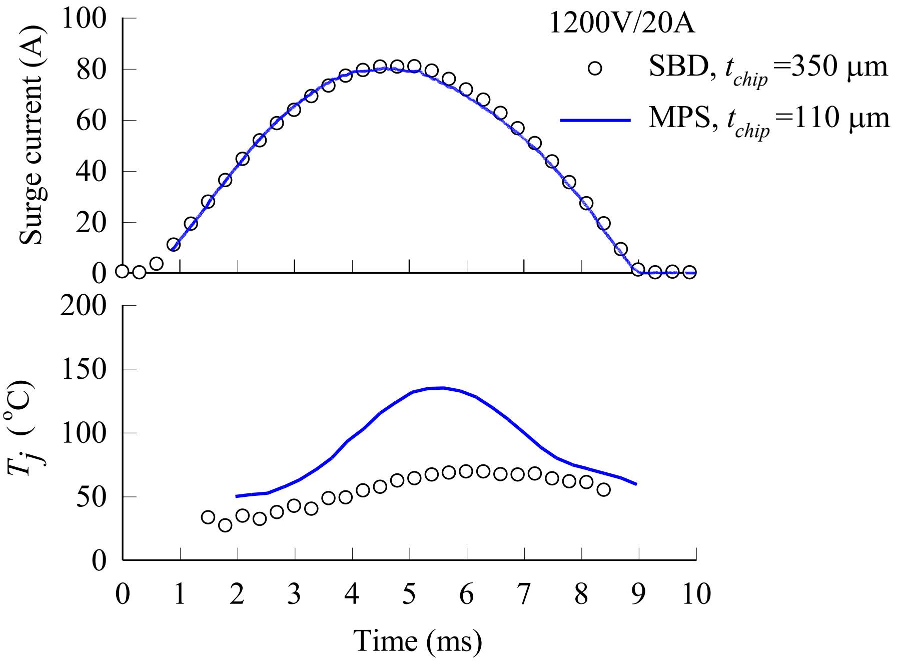

Fig. 8. Comparison of the junction temperatures of a thinned MPS diode and non-thinned homogeneous SBD during a surge current pulse with the peak value of 80 A, which is four times higher than the nominal current (data from [40]).

Figure 9 shows that the junction temperature of the non-thinned homogeneous SBD remains below the maximum operating junction temperature of 175°C for the peak surge current of 120 A, which is six times higher than the nominal forward current. In comparison, the junction temperature of the thinned MPS diode reaches the maximum operating junction temperature with the peak surge current of 100 A, which is five times higher than the nominal current.

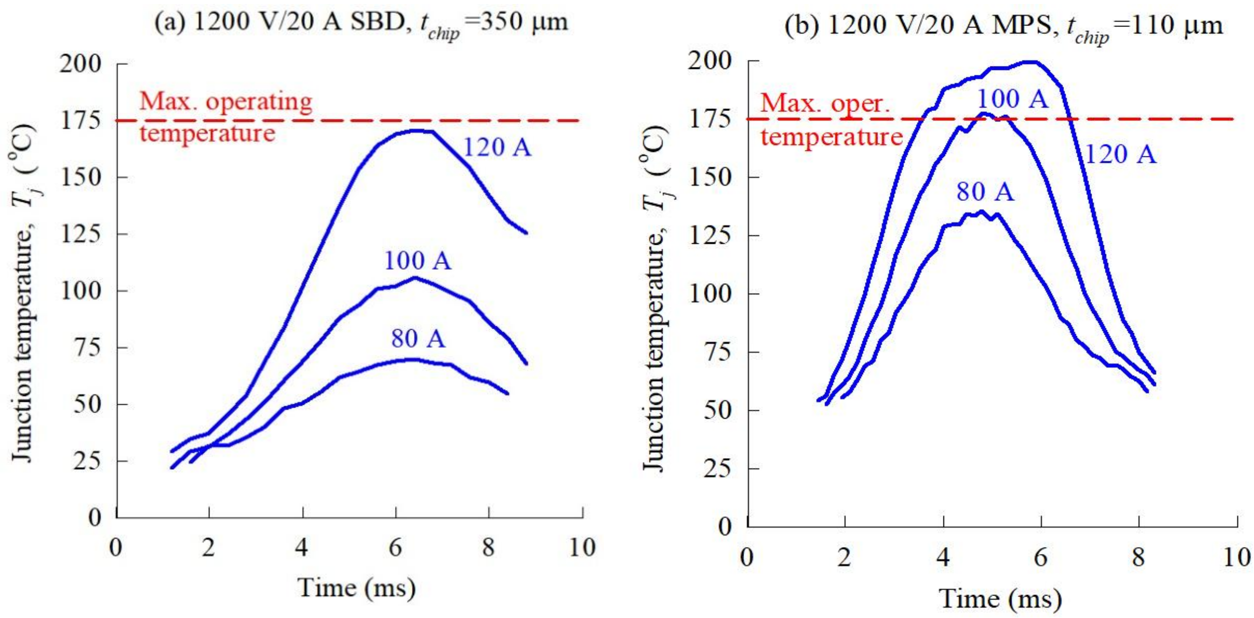

Fig. 9. The effect of the larger thermal capacitance of the non-thinned homogeneous SBD is that the junction temperature remains below the maximum operating junction temperature for larger peak surge currents (a) in comparison to the thinned MPS diode (b) (data from [40]).

Summary

In this paper, we present a homogeneous SiC SBD that has been fabricated without ion-implanted P-type regions, with a summary of the results relating to three key performance parameters: edge termination, reverse-bias current, and surge current capability. Regarding the edge termination, the electric field crowding is reduced by utilizing an epitaxial P-type ring with sloped edges. With a reduction in the angle of the P-type ring to 12º, the perimeter current at the edge termination is essentially eliminated, which enabled reverse-bias voltages higher than 4,500 V. In addition, a study of the homogenous SBD with nominal blocking voltages of 650 V, 1200 V, and 1700 V, demonstrated that the reverse-bias current at junction temperatures above 60ºC is due to the two fundamental current mechanisms of tunneling and thermionic emission. Regarding the surge current capability, the SBD illustrated higher repetitive peak surge currents than the MPS diode for the same junction temperature, within the maximum operating temperature of 175°C. This result is because the SBDs were fabricated without wafer thinning and with similar areas to MPS diodes, which corresponds to higher thermal capacitance that absorbs more heat dissipation at the same temperature.

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