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Three Level Pulses to Investigate Gate Switching Instability

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Abstract. We use novel three-level pulse sequences, where the intermediate level is either above or below the threshold voltage, to investigate gate switching instability (GSI) in 4H-SiC-MOSFETs. Results with sequences with an intermediate level above the threshold voltage (V_{th}) seem to falsify the hypothesis that trapped holes remaining at the interface after switching to the on-state, are the root cause for GSI, as was described in [1, 2]. Fast switching applications may cause negative transient pulses on the gate electrode during the off-state. Results with sequences with an intermediate level below threshold show that such transients may cause an increased V_{th}-drift. Introducing a delay between the transient and the turn-on of the transistor in such pulse sequences, does not mitigate the effect of a negative transient on the V_{th}-drift.

Introduction

Gate switching stress (GSS) using a gate voltage sequence as shown in Fig. 1a causes a positive threshold voltage drift that scales with number of cycles rather than stress duration, as this drift is largely independent of frequency. The V_{th}-drift increases for lower V_{OFF} as indicated by some exemplary results shown in Fig. 1b and also known from literature [3-6]. Two common theories to explain both the strong dependence on the minimum voltage level of the stress sequence and the scaling with number of switching cycles are local field enhancement and recombination induced interface degradation [3-5]. Both theories assume that electrons are expelled from interface traps during the low-level interval. Note, that this is equivalent to capturing of holes in interface traps. Local field enhancement assumes that a significant number of trapped holes remain at the interface after switching the gate to a positive voltage. Eventually these trapped holes will recombine with inversion layer electrons, but until then, they give rise to an internal electric field which adds up to the external field causing enhanced electron trapping. GSI has been shown to follow a power law up to at least 2 MHz with 50% duty cycle [3]. Therefore, internal field enhancement must assume that a significant number of holes recombines within 250 ns. Otherwise, the enhancement would be constant during the on-state, shifting the Vth-drift dependence on number of pulses towards a dependence on total duration of the high level.

Recombination induced interface degradation assumes that the energy released by recombination at interface traps causes reconfiguration of atomic bonds at the interface that result in electron traps. We propose a stress sequence using three voltage levels with intermediate level higher than the threshold voltage that largely avoids internal field enhancement to check the validity of that theory.

Gate switching instability is usually investigated using a gate driving circuit that switches between a negative low level and a positive high level to generate the gate switching stress. To assess the expected threshold voltage drift in an application, a sensible choice would be to take V_{ON} and V_{OFF} as used in the application for the positive and negative voltage level in GSS. However, overshoots at the rising or falling edge of the gate voltage signal may significantly increase the V_{th}-drift [2]. Overshoots typically happen when using a small gate resistor to allow a high gate current for fast switching. The induced overshoot voltage may be estimated by multiplying the inductance of the gate connection with the maximum of the time derivative of the gate current. Even with modules optimized for low inductance of the gate connection, some overshoot may need to be accepted to minimize the switching

losses. To account for the significant effect of overshoots, the JEDEC guideline JEP195 proposes to test two-level GSS for worst case conditions in the application, by setting the high level at least as high as the peak of the overshoot and the low level at least as low as the peak of the undershoot [7].

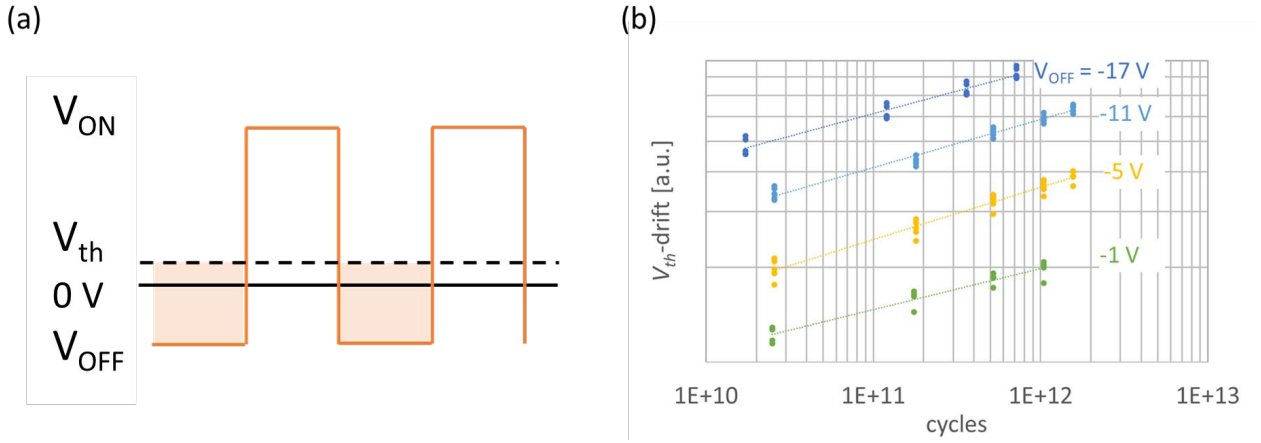

Fig. 1. (a) Gate voltage sequence for gate switching stress, where the shaded area represents the region below the threshold voltage. (b) Exemplary results that show the increase of threshold voltage drift with lower V_{OFF}.

Apart from overshoots due to the combination of gate inductance and fast gate switching, there are also transients on the gate voltage signal from capacitive coupling to the drain connection. Fig 2a shows a typical half bridge including some parasitic components and Fig 2b shows schematic drain voltage and gate voltage curves of the low side. Consider the case that the high side is switched off while the low side was already off and assume that the load will pull the output to ground in a short time. The drain voltage of the low side will then suddenly drop to ground and the capacitance between the gate and drain of the low side will couple this negative voltage slope into the gate electrode, resulting in an undershoot and some oscillations during the off-state as indicated by V_1. When the high side is turned on, while the low side is already off, we have a similar process. The fast rise of the drain voltage of the low side will couple in the gate electrode of the low side, risking an accidental turn-on (also called parasitic turn-on) of the low side, when gate voltage exceeds V_{th}. The oscillations after this fast rise of the gate voltage may cause oscillations with corresponding undershoot as indicated by V_2.

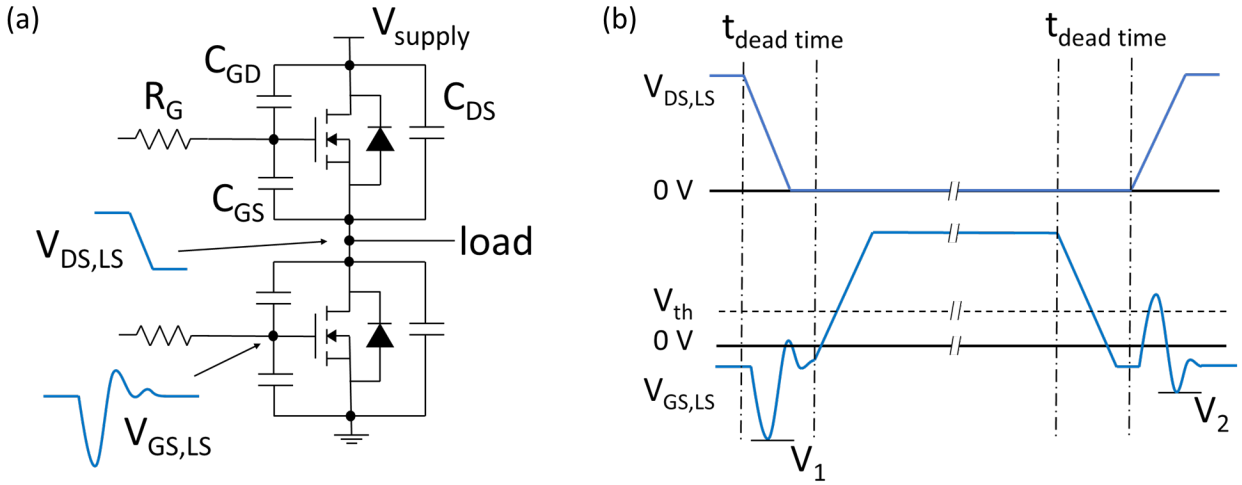

Fig. 2. (a) Schematic representation of a half bridge including parasitic capacitors between the terminals, showing how a fast voltage slope at the drain may couple into the gate connection of the parasitic gate drain capacitance. (b) Schematic drain voltage curve of the low side switch and the gate voltage curve of the low side switch with some indicated voltage levels of different undershoots and oscillations due to coupling with the drain connection.

Depending on module design, the different kind of undershoots may reach a voltage far below V_{OFF} and following the reasoning of the JEDEC guideline described above, we should take the lowest transient peak voltage as the low level in a two-level GSI experiment to obtain worst case conditions. As transients may be very short in time and may also have a delay before switching, it will be interesting if this reduces the V_{th}-drift compared to worst case conditions with a constant low level. We therefore propose a stress sequence using three voltage levels with intermediate level at negative voltage to check the effect of a delay between a transient and the switching time-point for the on-state on the V_{th}-drift.

Experimental Setup

We designed a setup to generate the three level gate stress sequences proposed in the previous section, with a relay to switch between stress phase and measurement phase. During the stress phase, source and drain are shorted and driven by a gate driver IC with 20% duty cycle at 500 kHz. The gate is driven at the same frequency and duty cycle by a second independent channel of the IC. The effective gate-source voltage is thus the difference between the voltage supplied to the gate and the voltage supplied to the source-drain connection. Voltages and delay between the driver channels are set such that we obtain the gate stress voltage sequence shown in Fig. 3. The sequences in Fig. 3b and Fig. 3c use V_{max} = +20 V, V_{min} = -18 V and +4 V for the intermediate voltage, which is higher than the threshold voltage and thus causes inversion at the interface. The sequences in Fig. 3d and Fig. 3e use V_{max} = +20 V, V_{min} = -18 V and -3 V for the intermediate voltage, which avoids inversion at the interface. We used commercially available devices (IMBG120R234M2H) with a small gate capacitance to allow fast switching without oscillations despite the relay in the drive path. Both stress and measurements were done at room temperature. To separate the V_{th}-drift due to GSI from the V_{th}-drift originating from the interface traps with time constants shorter than a few seconds, we included an aggressive preconditioning before each V_{th}-measurement by applying –18 V for 1 s and then applying +20 V for 1 s, repeating that preconditioning sequence five times. The V_{th} was measured with gate and drain shorted and forcing -0.9 mA at the source contact.

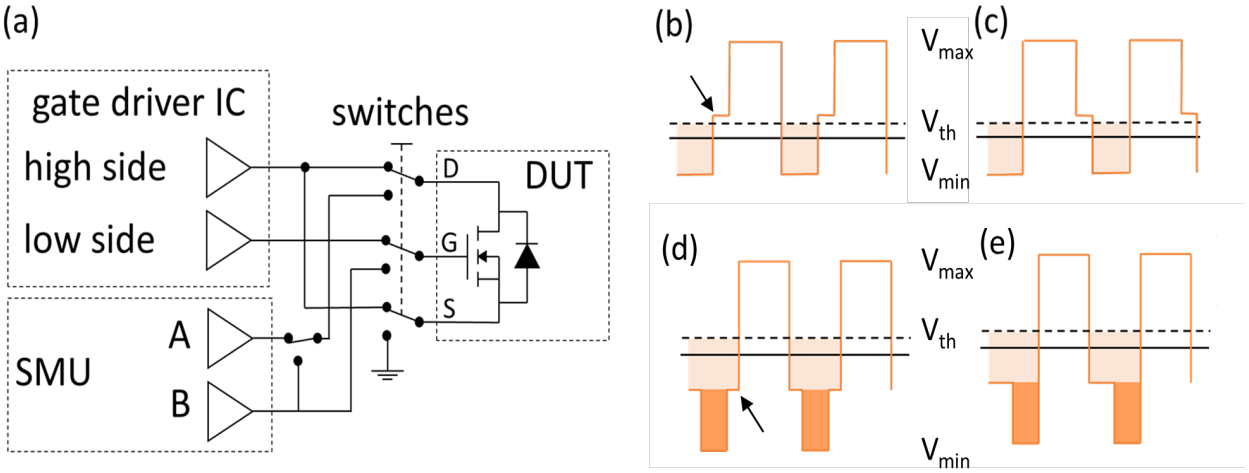

Fig. 3. (a) Schematic representation of the experimental setup to generate three-level waveforms with independent drivers for gate and source/drain and switches for intermediate measurement of V_{th} including aggressive preconditioning. (b) Three-level stress sequence with area below V_{th} indicated by light shading and intermediate level higher than V_{th}. The intermediate level defines a delay between V_{min} and V_{max}, as indicated by the arrow. (c) Same as before, but without delay. (d) Three-level stress sequence with area below the intermediate level indicated by darker shading. The intermediate level defines a delay between V_{min} and V_{max}, as indicated by the arrow. (e) Same as before but without delay.

Results of Three-Level Stress with Intermediate Level Higher than the Threshold Voltage

Fig. 4a shows measured oscilloscope traces of a single cycle based on the gate voltage sequences of Fig. 3b and Fig. 3c, with the intermediate level at +4 V. The traces differ in the delays, listed in the legend, between the end of the lower level and the beginning of the upper level. Fig. 4b shows two-level sequences used as references. The V_{th} measured with positive pulse sequence from Fig. 4b does not show any drift, whereas the curve from the negative pulse sequence shows a significant drift, as shown in Fig. 5a. The three level stress pulse sequences all show very similar V_{th}-drift curves. A close-up of these curves in Fig. 5b shows that the V_{th}-drift slightly increases with reduction of the delay.

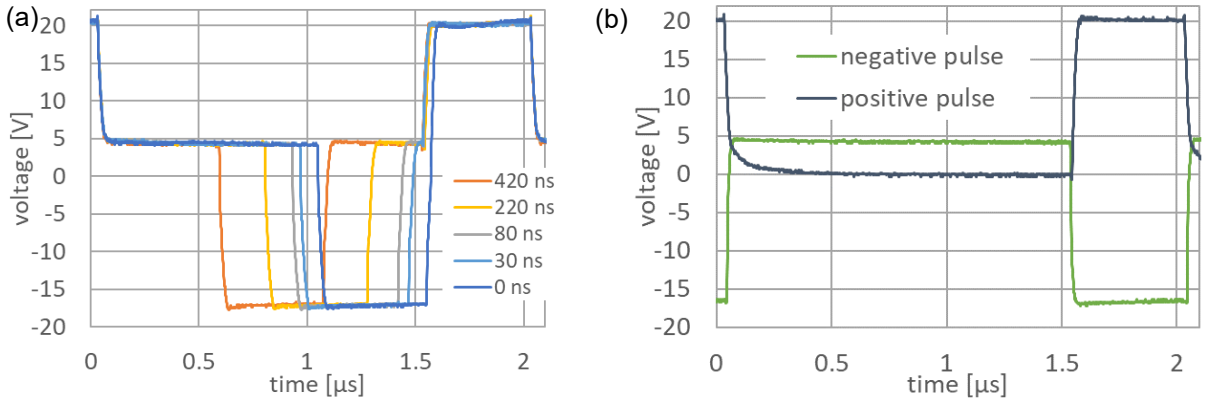

Fig. 4. (a) Oscilloscope trace of a single cycle of the applied voltage sequences. Three level sequences with different delays between the end of the lower level and the beginning of the upper level. (b) Reference sequences with only two levels.

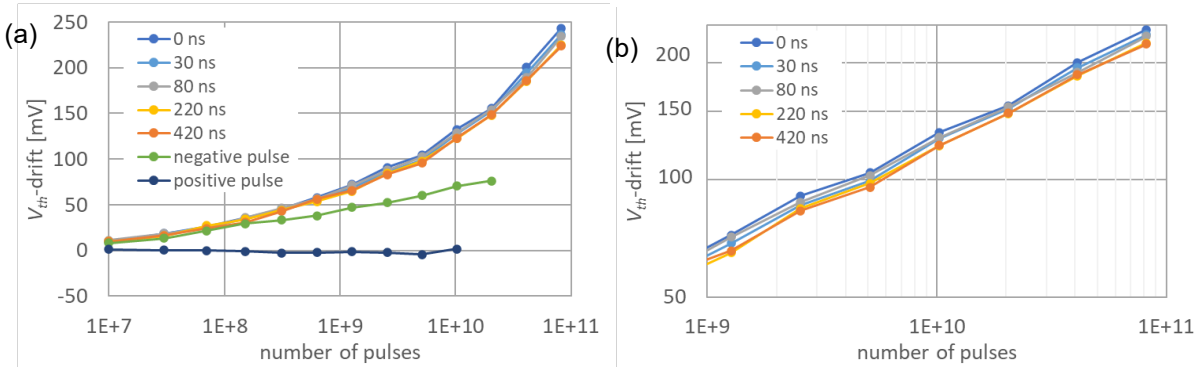

Fig. 5. (a) V_{th}-drift due to gate switching stress with the stress voltage sequences of the previous figure. Lin-Log plot. (b) Log-Log plot of the three level pulse sequences at high number of sequence cycles.

Results of Three-Level Stress with Intermediate Level At Negative Voltage

Fig. 6a shows the oscilloscope traces of the applied stress voltage sequences to investigate the effect of a negative pulse during the off-state. The trace without negative pulse is used as a reference. Fig. 6b shows that the negative pulse significantly increases the V_{th}-drift and that the delay between the end of the lower level and the beginning of the upper level, does not make a significant difference.

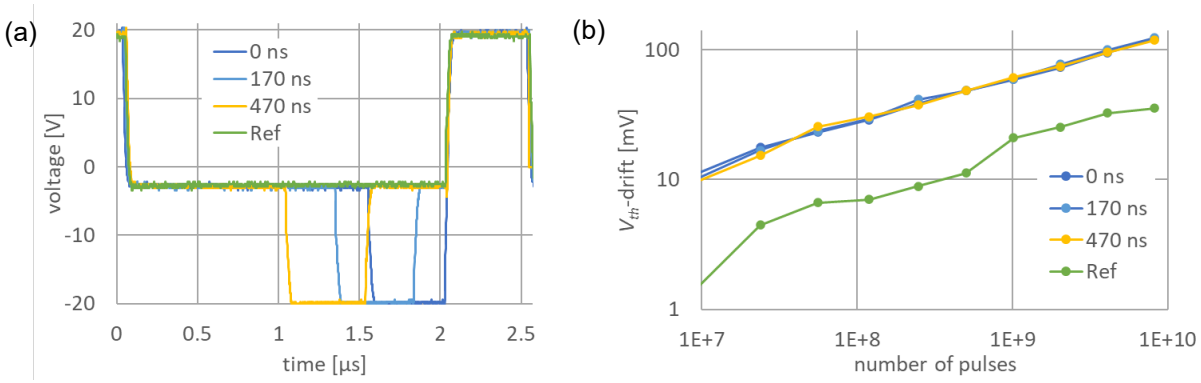

Fig. 6. Experiment to test the effect of a negative pulse during the off-state. (a) Oscilloscope traces of a single cycle of the applied gate stress voltage sequence with different delays between the end of the lower level and the beginning of the upper level. (b) Resulting V_{th}-drift after a high number of cycles.

Discussion

The V_{th} measured with the positive pulse sequence shown in Fig. 4b, believed to avoid GSI, does not show any drift in Fig. 5a, indicating that the preconditioning is sufficient to avoid V_{th}-drift from interface traps with trapping time constants shorter than a few seconds. The V_{th} measured with the negative pulse sequence shown in Fig. 4b, shows significant drift in Fig. 5a, indicating that even with low positive voltages, GSI is triggered effectively. Therefore, the V_{th}-drift curves shown in this paper are believed to be due to GSI.

The three-level stress sequences with intermediate level higher than the threshold voltage, as shown in Fig. 3b and Fig. 3c, were used to test the hypothesis based on internal electric field enhancement. We use the intermediate level above the threshold voltage to force the majority of the holes, trapped at the interface during the off-state, to recombine with channel electrons. As explained in the introduction, we expect that a significant number of holes recombine within 250 ns. Thus, when switching to the on-state, we largely avoid internal field enhancement. Fig. 5 allows a comparison of the curve without an intermediate level, i.e. no delay, before turn-on and thus with internal field enhancement, with the curve with an intermediate delay of 420 ns, where we would not expect significant field enhancement. We do see a slight increase for the curve without delay, which may be due to internal field enhancement. However, it is unlikely that increasing the delay would reduce the V_{th}-drift such that we end up at the combined V_{th}-drift of the reference curves with the positive and negative pulse in Fig. 4b, which would correspond to the case where we do not have GSI. The hypothesis for internal field enhancement as the root cause for GSI seems therefore unlikely. If we assume electron-hole recombination as the driving force for GSI, then the V_{th}-drift only depends on V_{max} and V_{min} and would be independent of the delay, matching the results much better.

As explained in Fig. 2, real applications may have large negative transients during the off-state and the curves in Fig 6. indicate that such transients may significantly increase the V_{th}-drift. This may be due to the additional hole accumulation during the negative transient as indicated by the dark shaded area in Fig. 3(d)-(e). The delay between the transient and switching on the transistor does not significantly change the V_{th}-drift. It seems that there is no “relaxation” after a transient curve to mitigate the effect of a negative transient on the V_{th}-drift.

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