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TCAD Model Parameter Calibration Strategy for 1200V SiC MOSFET

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Abstract. We present an accurate calibration strategy for TCAD model parameters of a 1200V vertical Silicon-Carbide (SiC) MOSFET, considering key physical characteristics of SiC such as trap distribution along the SiC/SiO_2 interface, mobility degradation, and Schottky contact for the p-type region. Initially, static characteristics are used to calibrate the SiC/SiO_2 interface traps and mobility model parameters in the low electric field region after matching the simulated doping profile with SIMS. Subsequently, capacitance-voltage (C-V) characteristics are calibrated by considering both the capacitance in periphery and the Schottky effect for the p-type well (PWell) region. Finally, the calibrated model was used to evaluate SC withstand time using mixed-mode TCAD simulation. The simulated static and dynamic performance, including short-circuit (SC) withstand time, are in good agreement to the measurements with an error rate of less than 10%. In summary, we propose a TCAD model parameter calibration method for highly accurate simulation of 1200V vertical SiC MOSFETs, which will contribute to finding process and design solutions that consider both static and dynamic characteristics.

Introduction

SiC MOSFETs are highly desirable due to their lower on-resistance (R_{ON}), higher breakdown voltage, and stronger high temperature performance compared to silicon devices in medium power applications [1-2]. The faster switching and higher power density inherent in these applications present new challenges for SiC MOSFET device designers. An accurate set of model parameters in a device simulator is essential to perform reliable simulations, as the absence of full simulation support requires costly fabrication-based design cycles. However, TCAD simulations for SiC often lead to inaccurate results primarily due to insufficient information on interface properties, as well as bulk/interface mobility degradation resulting from variations in manufacturing batches, processes, and application conditions. Previous studies have primarily focused on calibrating interface traps only, which limits their applicability across a wide voltage range [2-3]. This limitation arises because the device performance is also significantly influenced by other properties such as bulk traps, mobility degradation, and Schottky barrier effects. In this study, we present an accurate calibration strategy for TCAD model parameters of a 1200V vertical SiC MOSFET by considering the overall physical model parameters including trap distribution along the SiC/SiO_2 interface, mobility degradation, Schottky contact characteristics, and periphery dimensions. The proposed method has demonstrated enhanced predictive performance for current-voltage (I-V) (V_d=0~5V, V_g=0~20V), C-V characteristics (V_{ds}=0~800V), and SC performance (V_d=800V).

Simulation and Results

Fig. 1 shows the cross-sectional view of the conventional 1200V vertical SiC MOSFET along with its resistance model, which is used to calibrate the static characteristics. The proposed calibration method is based on the default model parameters of 4H-SiC from the latest version of Sentaurus TCAD [4]. This model utilizes a wide-bandgap material featuring high critical electric field,

saturation velocity, and thermal conductivity. However, it characterizes zero interface/bulk trap density and ideal Ohmic contact, which are not realistic [4]. Consequently, as shown in Fig. 2, we propose a TCAD model parameter calibration flows to provide designers with more realistic and accurate simulation results.

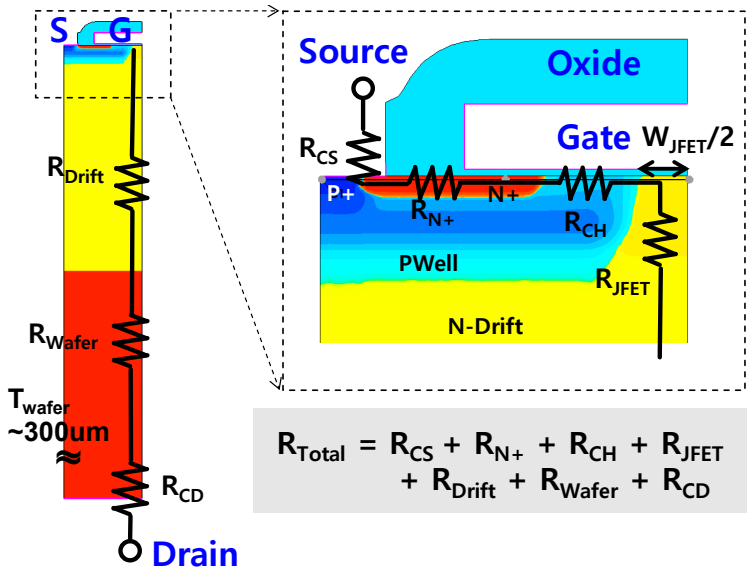

Fig. 1. The cross-sectional view of a 1200V vertical SiC MOSFET with a resistance model for I-V calibration (R_{Drift} = resistance in drift region (N-epi), R_{Wafer} = resistance in high doped wafer, R_{CS}, R_{CD} = resistances in source and drain contacts, respectively, R_{N+} = resistance in N-plus source, R_{CH} = channel resistance, R_{JFET} = resistance in JFET region, T_{Wafer} = thickness of highly doped wafer, W_{JFET} = JFET width).

The process calibration of the device structure and doping profiles is crucial as the initial step in device calibration. We compared the SIMS profile with the process simulation results and calibrated the Monte-Carlo model parameters in TCAD as the first step (not shown in here). For the device model parameter calibration, the static characteristics, especially the current-voltage (I-V) characteristics, are considered as the second step to apply the appropriate mobility models and the SiC/SiO_2 interface characteristics. Since the density of states (D_{it}) at the SiC/SiO_2 interface is more than two orders of magnitude higher than at the Si/SiO_2 interface [5], resulting in reduced channel mobility and device reliability issues, estimating the accurate interface trap density in this step is the most important. In the resistance model depicted in Fig. 1, only the channel resistance (R_{CH}) varies with gate bias, and it is high enough in the subthreshold (SS) region which means the total resistance (R_{Total}) can be set to R_{CH}. Since the SS slope is mainly affected by the interface trap density, once the oxide capacitance and channel doping concentration are determined, estimating the order of D_{it} can be simplified without requiring C-V measurements that necessitate a lateral MOSFET structure. V_T is adjusted by applying a fixed charge in SiO_2, which does not impact gate controllability. And the upper V_T region, which is affected by the remaining resistances as well as R_{CH}, is adjusted by changing the mobility/Schottky model parameters for the JFET/Drift/N+ regions.

For the dynamic characteristics, the main feature is the C-V characteristics. Each capacitance indirectly represents the accuracy of doping concentration, device structure, and area. Since the doping concentration of the simulation is calibrated with the actual SIMS profile, it is essential to consider device dimension factors to understand C-V characteristics. For the input capacitance (C_{iss}) and output capacitance (C_{oss}) calibration, both active (cell) and peripheral (ring and gate-pad (Fig. 3(a))) areas are taken into account because gate-source capacitance (C_{gs}) and drain-source capacitance (C_{ds}) are the primary capacitances in the peripheral area as shown in Fig. 3(b). In addition, since the reverse transfer capacitance (C_{rss}) characteristic according to the drain voltage is the main characteristic of the switching overshoot characteristic, it is crucial to ensure model consistency by considering the Schottky barrier because P-plus typically has a large Schottky barrier in SiC [6].

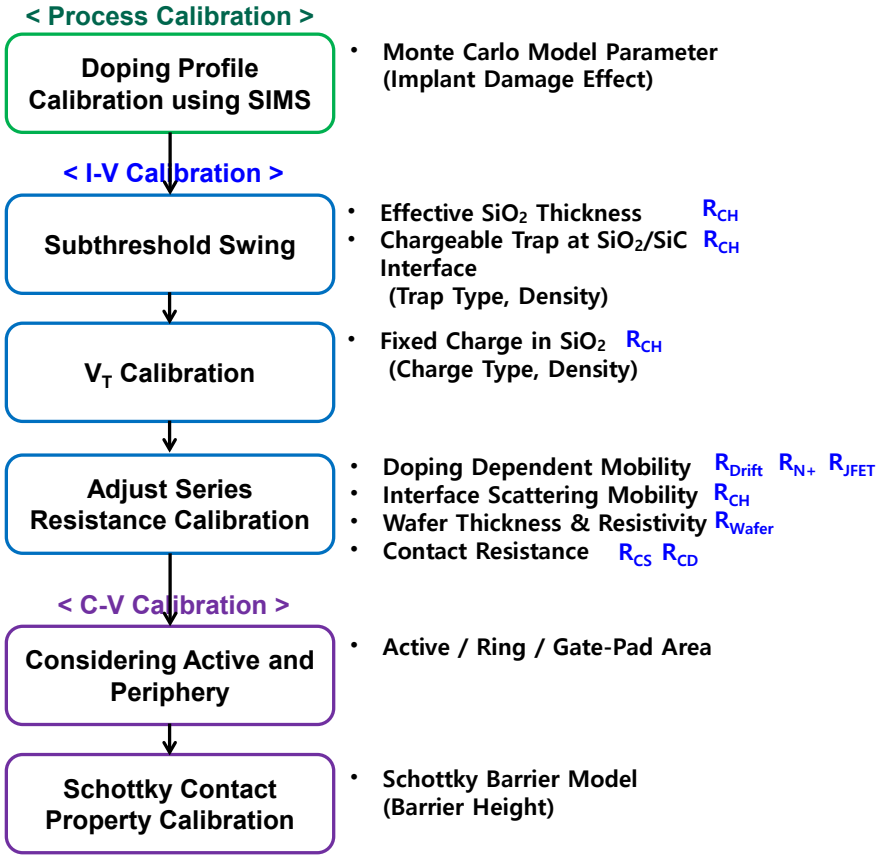

Fig. 2. The proposed TCAD calibration flow for the SiC MOSFET, including its relevant model parameters within Sentaurus workbench and the resistances shown in Fig. 1.

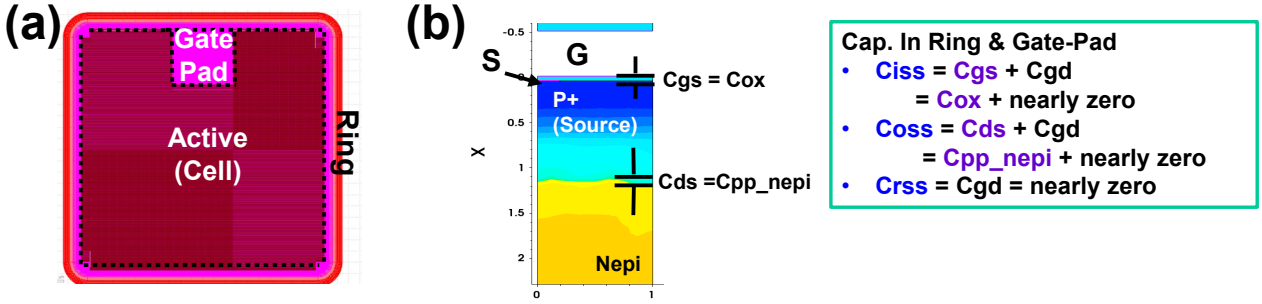

Fig. 3. (a) Top view of the SiC MOSFET device. (b) Vertical structure and its capacitance model in the ring and gate-pad regions. C_{gs} & C_{ds} are the main capacitances in this area. Gate-drain capacitance (C_{gd}) is nearly zero due to the source-connected P-plus (P+) region blocking the gate.

Figure 4 shows the improved accuracy of the TCAD model created using the proposed calibration method as evidenced by its comparison with the I-V experimental data. A good matching is observed in all curves under various bias conditions (V_d and V_g). The I-V calibration achieved through the proposed procedure indicates that the calibrated set of model parameters operates on devices with different W_{JFET} (not depicted here). This suggests that the calibrated TCAD well models each component of the resistance in Figure 1, including mobility degradation in both bulk and interface regions, as well as parasitic resistance components in the wafer and contact regions.

Figure 5 compares the TCAD simulation with the experimental results of the C-V characteristics. Since the area of the ring and gate pad corresponding to the periphery constitutes more than 15% of the total chip area, C_{gs} and C_{ds} must reflect the impact of the ring and gate pad, as shown in Fig. 5 (a) and (b). Additionally, as shown in Fig. 3 (b), C_{rss} does not affect the periphery area. Since a certain area of PWell (Fig. 1) can function as floating nodes due to the Schottky barrier of the P-plus contact, the floating node effect of PWell is considered in C_{rss} calibration, resulting in good matching with the

experimental data shown in Fig. 5(c). The proposed model exhibits an error rate of less than 5% for SS Slope, V_T, R_{ON}, and capacitances.

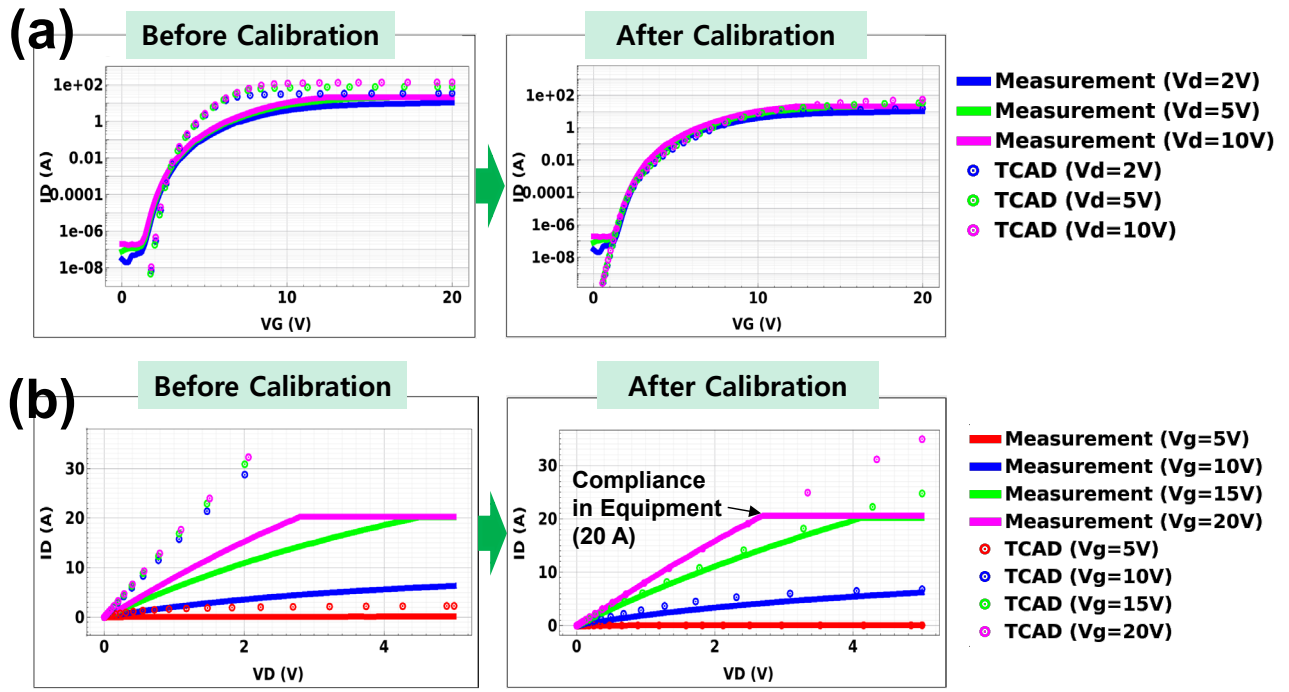

Fig. 4. Measured vs. TCAD (a) I_D-V_G with changing V_D and (b) I_D-V_D with changing V_G before and after calibration, respectively.

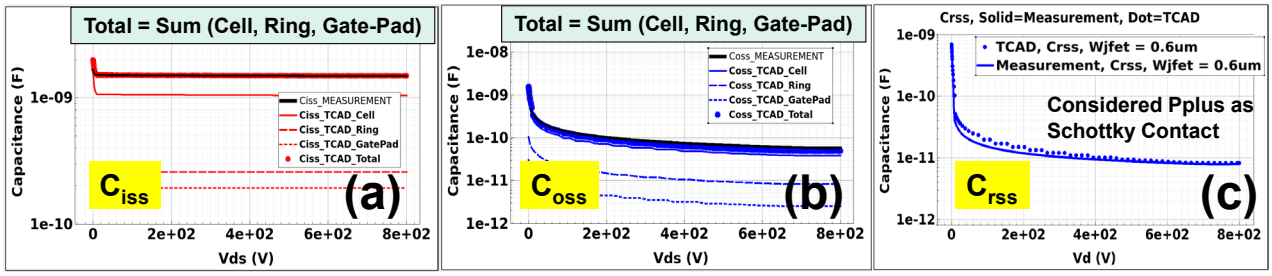

Fig. 5. Measured data vs. calibrated TCAD simulation results of C-V characteristics (f=1 MHz) ((a) $C_{iss} = C_{gs}+C_{gd}$, (b) $C_{oss} = C_{ds}+C_{gd}$, (c) $C_{rss} = C_{gd}$).

Finally, the calibrated model parameters were used to evaluate the most important characteristic of SiC MOSFETs: SC withstand time using mixed-mode TCAD simulation. The SC test circuit is shown in Fig. 6. Besides the calibrated model parameters, all other physical model parameters for thermal characteristics in 4H-SiC supported by Synopsys have been applied in the SC simulation. During the simulation, after the gate voltage turns off, the total current does not reach zero due to carrier generation induced by the high lattice temperature, as shown in Fig. 6 (d). This leakage current increases the lattice temperature, leading to further increase in leakage current through a positive feedback loop. The generated holes flow through the PWell to Pplus, increasing the electrostatic potential in PWell and reducing the energy barrier, as shown in Fig. 6 (d), resulting in parasitic BJT turn-on in the vertical direction under PWell. The pattern of the SC failure characteristics after Vgs turns off in TCAD matches the measurement results. The simulated SC withstand time was very similar to the measurements with an error rate of less than 10%.

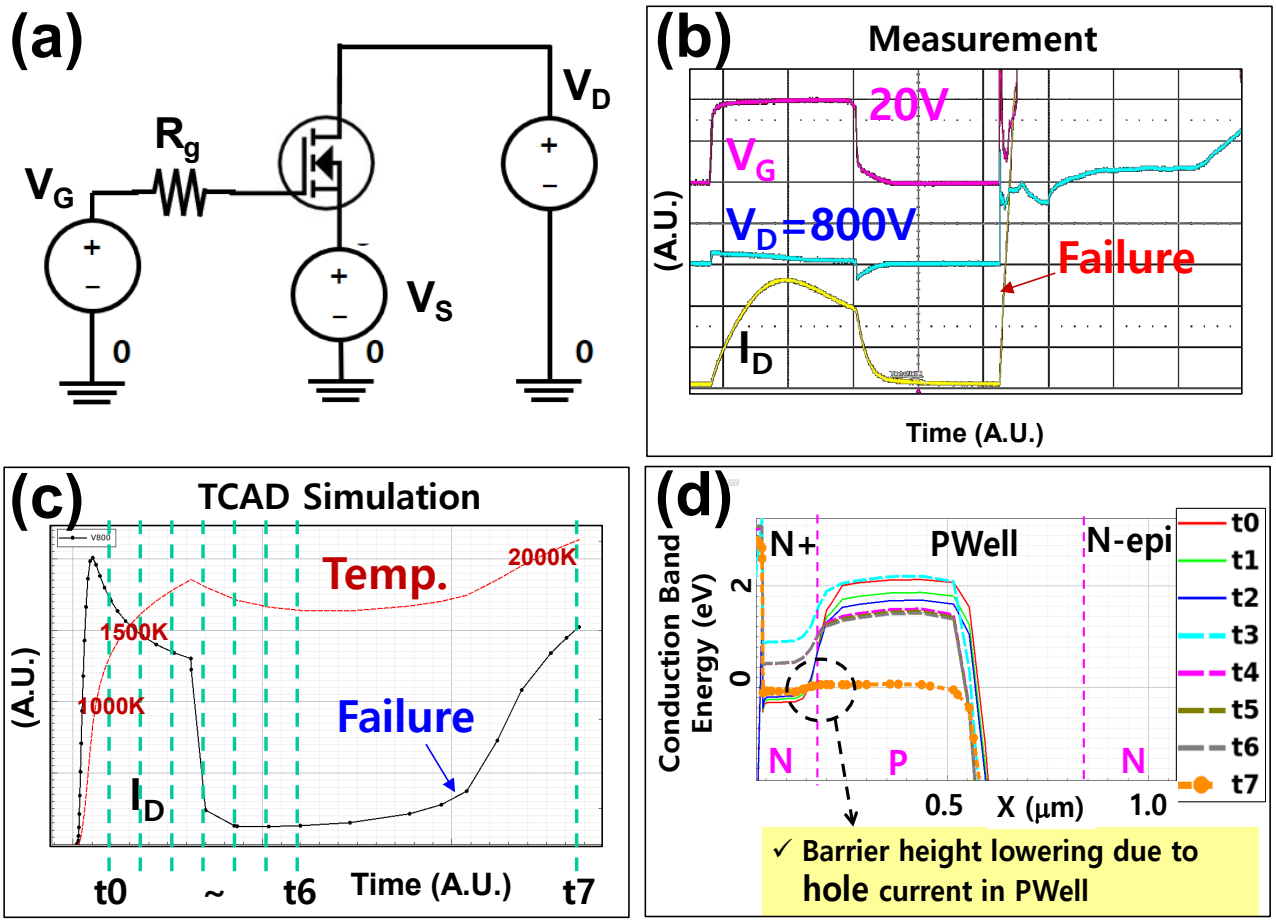

Fig. 6. (a) Circuit diagram for SC test (V_D = 800V, V_G = 20V, V_S = 0V). (b) Measurement and (c) TCAD results of the SC test under the failure condition, respectively. Failure in simulation is determined when the maximum lattice temperature exceeds 1900 K and the drain current increases again after the gate turns off. (d) Simulated vertical conduction band diagram at each time in Fig. 6 (c).

Conclusion

In summary, we have proposed a TCAD model parameter calibration method for highly accurate simulation of 1200V vertical SiC MOSFETs. This method will contribute to finding process and design solutions that consider both static and dynamic characteristics. The calibrated model parameters can be used to analyze 2D/3D cell design to improve R_{ON}-BV trade-off characteristics, process modifications, or other dynamic characteristics such as reverse recovery, gate charge, unclamped inductive switching, etc.

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