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Lifetime Modeling of MOS Based SiC Vertical Power Devices under High Voltage Blocking Stress

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Abstract. Robustness under blocking is an important reliability metric for MOS based SiC power devices. Accelerated reverse bias (ARB) stressing, which typically employs multiple V_{DS} stress values beyond the rated drain bias but below the avalanche voltage, is considered as the best practice for measuring the device lifetime in the blocking mode. However, generating enough failure statistics within a reasonable timeframe in ARB tests can be challenging, especially for devices which are designed such that avalanche breakdown occurs at a lower drain voltage than is necessary to induce gate oxide wear-out failures in a tractable duration. In this paper we propose a simplified modeling approach where qualification-like high temperature reverse bias (HTRB) or ARB test at a single stress voltage for a reasonable stress duration can be used to project gate oxide lifetimes under blocking.

Introduction

Owing to its wider bandgap 4H-SiC allows fabrication of unipolar power switches with voltage ratings more than ten times higher than is feasible for Si unipolar devices, with the same specific on-resistance. Hence during off state while blocking high voltage, the electric fields experienced by SiC and the gate dielectric (typically SiO_2) are much higher in SiC vertical power MOSFET devices as compared to their Si counterparts [1]. As a result, reliability under blocking has become a hot topic for MOS based SiC power devices and is discussed in detail by industry standard bodies such as JEDEC. Although running only a single point high temperature reverse bias (HTRB) qualification test at or near maximum rated drain bias and at maximum rated junction temperature can fulfill the qualification requirements for blocking reliability, it does not provide information regarding device lifetime prediction for SiC-MOS devices during high voltage off-state stress. Like gate bias mediated TDDB, under high drain bias stress failures are typically due to gate oxide wear-out in the JFET region of the power device. In order to enable blocking lifetime extrapolation at operating condition, a modeling approach consistent with the E-model for gate oxide (G_{OX}) lifetime can be used for accelerated reverse bias (ARB) stressing. For ARB stressing one would typically employ multiple V_{DS} stress values beyond the rated drain bias but below the avalanche voltage [2-5]. However, generating enough failure statistics within a reasonable timeframe in ARB tests can be challenging, especially for devices which are designed such that avalanche breakdown occurs at a lower drain voltage than is necessary to induce gate oxide wear-out failures in a tractable duration. In this paper we propose a simplified alternative modeling approach that can be used from ARB/HTRB test data from one stress drain voltage and reduced stress time, to project device lifetime under blocking at lower drain voltage values.

Experimental Data on Accelerated Reverse Bias (ARB) Test

SiC power MOSFETs are designed with a safe margin between rated voltage and avalanche voltage which enables the accelerated reverse bias (ARB) test to be performed above the rated drain voltage, but below the avalanche voltage of the device. This margin is critical as it determines how much voltage acceleration can be generated above the rated voltage. In this regime of drain stress,

oxide electric field in the JFET gap can induce gate oxide wear-out failures. Figure 1 shows the results of an ARB test where three sets of Wolfspeed 1200 V rated packaged parts were stressed with $\boldsymbol{V_{DS}}$ values of 1310V, 1380V and 1450V at 175°C for nearly one year to gather failure statistics. The devices show relatively low gate and drain leakage until abrupt drain to gate/source short failure occurs, with little to no precursor signal, similar to what happens in a constant bias time dependent dielectric breakdown (TDDB) test.

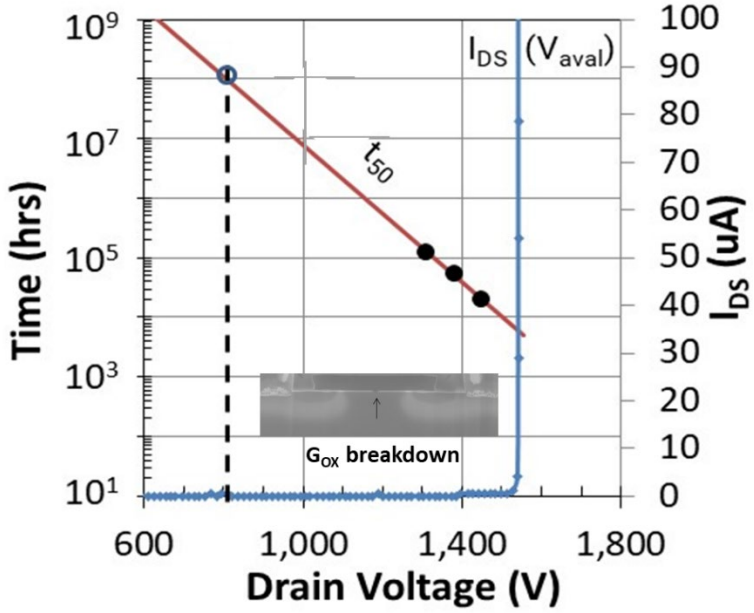

Fig.1. MTTF lifetime projection of 1200 V rated SiC MOSFETs under ARB condition from three groups of stressed parts at 175°C. Inset shows a cross-sectioned device with a gate oxide rupture after ARB stress right at the highest field point, in the center of the JFET region.

Failure analysis confirms that the ARB failure mechanism is gate oxide breakdown at the center of the JFET gap (inset in Fig. 1). This is expected because that is the location of the highest gate oxide electric field in an ARB test. There is no evidence of edge termination or SiC breakdown, which demonstrates that gate oxide wear-out is the primary failure mechanism. Therefore, from the failure distribution which followed Weibull statistics, lifetime projection at operating voltage is then performed by extracting fitting parameters via maximum likelihood estimation and employing a "linear E-model". The median time to failure (MTTF) plot is derived from the ARB dataset and indicated as $\boldsymbol{t_{50}}$ in Fig. 1.

Lifetime Modeling for ARB

Although the above mentioned method is the best possible approach to model ARB data, it has been extremely time consuming to take a certain percent of population to failure for all different drain bias values V_{DS} such that lifetime can be projected with a sufficiently high confidence level. Simply from the perspective of test-duration, conducting an ARB test similar to the one presented Fig. 1 for every qualification of a new product is not feasible. Therefore, we propose a modeling approach that allows one to project blocking lifetime within a reasonable amount of test duration while maintaining a high confidence level. Figure 2 portrays this alternative approach for off-state lifetime modeling utilizing the "linear E-model" and a single stress voltage failure data set obtained from a qualification type HTRB or ARB test running for a certain duration (preferably 1000 hours or more). Considering that a certain percentage ($\boldsymbol{p}$%) of the population failed after $\boldsymbol{V_{DS}}$ is applied for $\boldsymbol{t_p}$ hours, with a known Weibull slope ($\boldsymbol{\beta}$), MTTF or any other failure time percentile ($\boldsymbol{q}$%) can be extrapolated ($\boldsymbol{t_q}$) at that $\boldsymbol{V_{DS}}$ condition as given by Eq. 1. From this test result, according to "linear E-model" a blocking lifetime curve can be drawn for any drain bias using Eq. 2.

$$t_q/t_p = [ln(1-q)/ln(1-p)]^{(1/\beta)} \quad (1)$$

$$TTF = C + \gamma V_{DS} \quad (2)$$

However, such an estimation will still need the knowledge of either voltage acceleration γ or intercept C. Estimation of γ is non-trivial and equally challenging as constructing lifetime curves from multiple drain biases. Conversely, the intercept C represents the lifetime of a device when V_{DS} is extrapolated to 0. At zero gate or drain bias the GOX lifetime is likely determined by the physics of diffusion and subsequent degradation mechanism. Hence the conjecture that $C_{blocking} \sim C_{TDDB}$ at $V_{DS}, V_{GS} = 0$ for a given device technology (identical oxide thickness, drift thickness, cell design etc.) and temperature likely should hold at least for a first order approximation. By using this argument, we propose to extract C_{TDDB} value by conducting TDDB test on the devices from the same product family with multiple V_{GS} voltages. Thus, the knowledge of C value from a TDDB test, along with a known Weibull slope (β) likely can be utilized to construct a blocking lifetime curve for any failure percentile from a single drain bias stress test data.

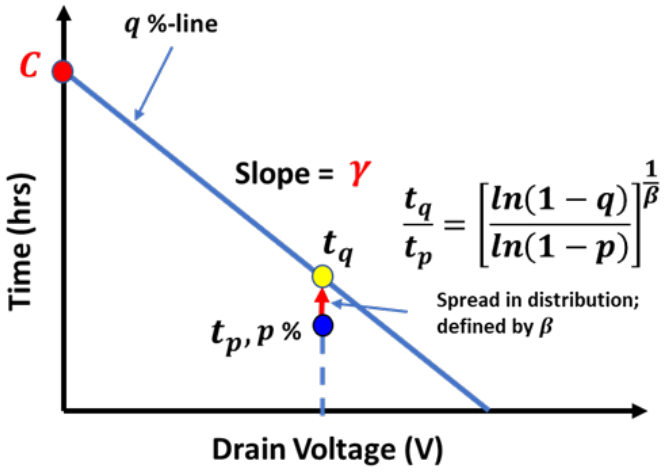

Fig. 2. Schematic representation of blocking lifetime plot construction from a single V_{DS} stress for t_q hours. Estimation of failure time t_q for any failure percentage (q%) from stress time t_p with a certain failure percentage (p%) and the knowledge of C_{TDDB} provides a means to construct the TTF extrapolation line.

Analysis of TDDB data for C_{TDDB}

In the previous section, we argued at $V_{DS}, V_{GS} = 0$ gate oxide lifetime should solely be determined by the physics of diffusion at a particular temperature and thereby making $C_{blocking}$ comparable to C_{TDDB}. A relevant question can be whether experimental data supports this claim. To address this, we extracted C_{TDDB} values from a significant number of TDDB tests conducted at multiple gate voltages (V_{GS}) on different sets of devices with similar voltage ratings, all with comparable gate oxide thicknesses. By extracting fitting parameters via maximum likelihood estimation and employing a "linear E-model", MTTF lifetimes for different products are plotted in Fig. 3. C_{TDDB} values projected from TDDB data fall within the range of 10^{13}-10^{14} hours. Notably, $C_{blocking}$ value (~10^{13} hours) extracted from the year-long ARB test (as shown in Fig. 1) closely matches with the value obtained from TDDB testing on similar devices at 175°C, further corroborates this assumption.

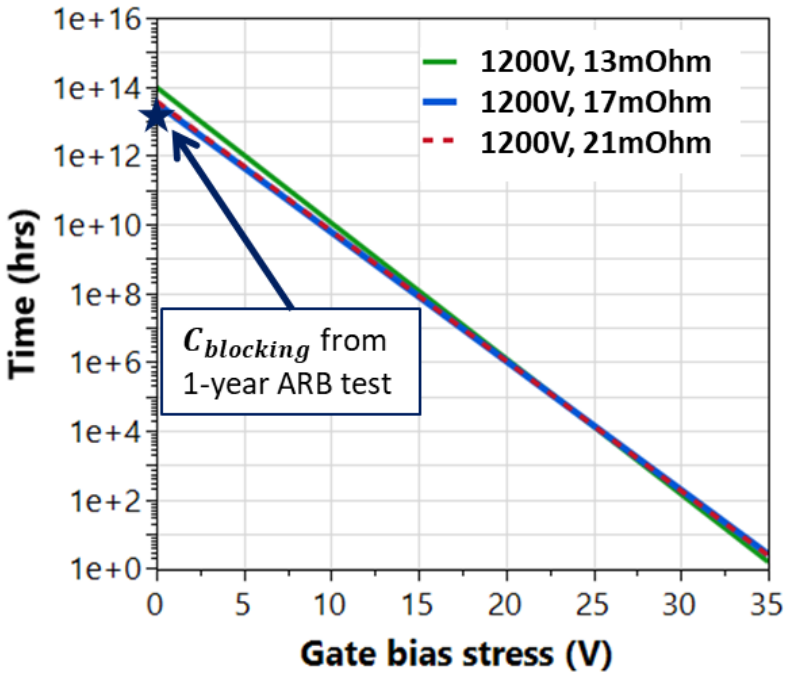

Fig. 3. MTTF (q = 0.5) lifetime plots for TDDB tests on different products having similar gate oxide thickness and similar voltage and resistance ratings.

Discussion of Different Scenarios under ARB Test

Fig. (4a-d) presents hypothetical scenarios of projecting MTTF from a 1200 V rated product, assuming zero failures after 1000 hours of stressing, for different V_{DS}, C, sample size and β values. In Fig. 4(a), C values are varied from 10^{11} to 10^{14} hours with a β value of 1 and a sample size of 240. In case of 0 failures out of 240, the failure percentage (p%) at the stress condition is calculated using equivalent failure rate at a 60% confidence level ($\chi^2/2$), yielding a failure rate of p =0.38%. Substituting the value of p and stress time t_p = 1000 hours into Eq. 1, $t_q = t_{50}$ is obtained, as indicated by the yellow circle. MTTF lines are drawn by connecting the yellow circle to different C values. A higher C_{TDDB} value from positive gate bias TDDB suggests a longer intrinsic GOX lifetime, and thus a longer intrinsic GOX lifetime under used blocking condition (e.g. 800V) therefore can be achieved, as indicated by the red arrow. It is recommended that C_{TDDB} should be extracted by conducting TDDB tests at multiple V_{GS} voltages on the same group of devices whenever possible. Fig. 4(b) predicts MTTF for various stress voltages, V_{DS} values ranging from 1200 V to 1400 V with a C value of 10^{13} hours and a β value of 1. With no failures in any of the three voltage scenarios (0/240), t_{50} values are extracted using Eq. 1, as shown by the yellow circles at 1200V, 1300V and 1400V. MTTF lines are drawn by connecting the C value to the yellow dots. The model predicts that devices with no failures at 1400V will have a longer MTTF lifetime under operating conditions compared to those with no failures at 1200V, as indicated by the red arrow. Figure 4(c) illustrates the effect of increasing sample size on the lifetime plot, assuming zero failures in all cases. It is important to note here that a higher sample size does not necessarily lead to a proportionate increase in lifetime estimate under operating condition, as C values remain constant at 10^{13} hours in this scenario. Finally, Fig. 4(d) shows the impact of different Weibull β values, ranging from 1 to 2, on lifetime projections. In case of ARB, the Weibull β value should be validated with a longer test, as the β value under blocking conditions may differ from that of gate bias-mediated TDDB test, especially since hot holes could contribute to the failure mechanism under ARB, as mentioned in Ref. [4].

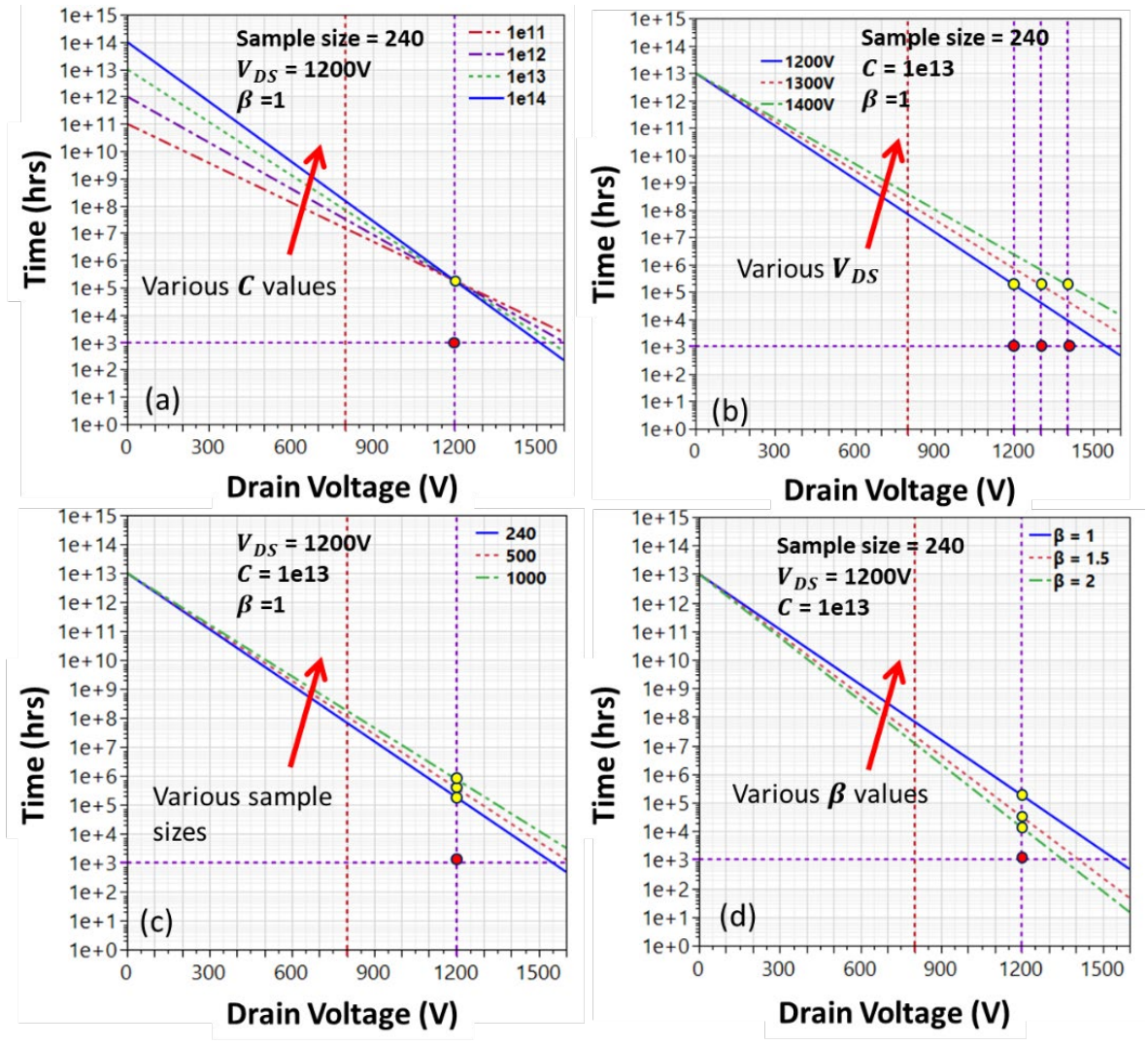

Fig. 4. MTTF (q = 0.5) lifetime plots are presented based on assumptions that 0 fails have been encountered after 1000 hours of stressing with (a) C varying from 10^{11} to 10^{14} hours, V_{DS} = 1200 V, β = 1, sample size =240 parts (b) three different V_{DS} stress conditions ranging from 1200-1400 V, C = 10^{13} hours , β = 1, sample size = 240 parts (c) variable sample sizes ranging from 240 to 1000, C = 10^{13} hours, V_{DS} = 1200 V, β = 1, (d) β varying from 1 to 2 while V_{DS} = 1200 V, C = 10^{13} hours and sample size = 240.

Shortcomings of this Method

Fig. 5 shows certain shortcomings of this technique to project Gox lifetime under blocking from a single point V_{DS} data set. Consideration has been given to scenarios where blocking lifetime estimated from TDDB extracted C value predicts favorable TTF numbers, but lifetime extracted from multiple V_{DS} stress voltages is influenced by an alternative failure mechanism, as shown in Fig. 5(a). In such cases, relying on a single data point may yield an overly optimistic off-state lifetime estimate. However, in such cases the dominant blocking failure mechanism likely will be unrelated to intrinsic Gox breakdown and should be tackled in a way beyond the scope of this study. This could be proven by appropriate failure analysis. Conversely, if the TDDB lifetime is adversely affected by a mechanism other than intrinsic Gox failures, then by virtue of lower C value, the blocking lifetime estimation might get impacted and will project a rather pessimistic value. So, it is imperative to make sure that the C value estimated from TDDB represents true intrinsic Gox failure mechanism. Interested readers may review Ref. [4] for a modeling work where extrinsic defects have been introduced to perform a defect mediated lifetime modeling under blocking conditions. Finally, this

paper focuses on the off-state reliability under $\boldsymbol{V_{DS}}$ stress with gate grounded. Similar analysis is possible for scenarios where negative (for n-channel MOSFET) $\boldsymbol{V_{GS}}$ works in tandem with $\boldsymbol{V_{DS}}$ for assessing blocking reliability.

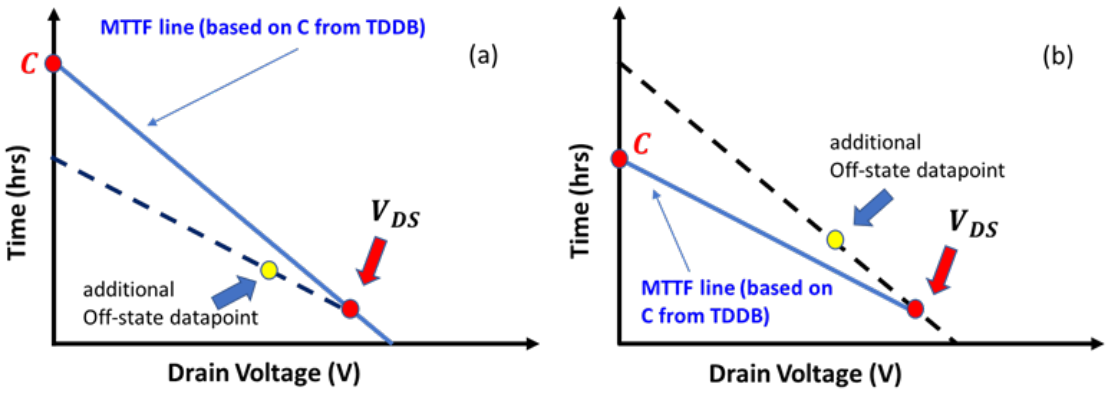

Fig. 5. Scenarios when using $\boldsymbol{C}$ values from a TDDB test. a) Failure mechanism not related to intrinsic GOX breakdown, in which estimated lifetime is overly optimistic compared to full analysis with multiple stress voltages, b) Poor $\boldsymbol{C}$ value estimated from TDDB for failures likely not related to intrinsic GOX breakdown can result a rather pessimistic blocking lifetime prediction.

Summary

In conclusion, we present a novel alternative modeling technique to project MOSFET intrinsic GOX lifetime under blocking from a single drain bias stress dataset with the aid of TDDB results done on a similar group of devices at the same temperature which is otherwise extremely time consuming or even impossible to model.

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