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SiC MOSFETs C-V Capacitance Curves with Negative Biased Drain

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Abstract. There are some technological issues in SiC MOSFETs that are still unsolved. One of the main problems is the high density of traps/defects at the SiC/SiO_2 interface. Traps distribution at such interface is complex and it affects the overall performance of the device. The high-density of defects at the SiC/SiO_2 interface is a relevant problem since it can influence the overall performance of the device, causing detrimental impacts on threshold voltage stability, channel mobility and leakage current amplitude. Due to the fundamental importance of the SiC/SiO_2 interface characterization, several techniques have been employed to investigate defects properties related to this region. In this work non-classical C-V measurements are performed. Capacitance is measured between Gate and Source terminals while a fix DC voltage is imposed on the Drain. This latter is considered among positive values in the first case, while it is chosen as a negative voltage in the second case. The arising capacitances in both cases show an unexpected behavior which can be related to interface properties. To this aim numerical analysis is performed in Sentaurus TCAD environment.

Introduction

Silicon Carbide (SiC) MOSFETs are gradually replacing Silicon (Si) MOSFETs due to the excellent properties of SiC material. High thermal conductivity and high bandgap [1] are indeed properties of such material. These devices technology has undergone a great development in last decades. However, there are still some issues that are not completely solved. Among these it worth to be mentioned that the density of defects arising at the SiC/SiO_2 interface is orders of magnitudes higher with respect to Si/SiO_2. These defects can affect some crucial properties of the overall device [2] such as the channel mobility[4] and threshold voltage instability [3]. Given the key role played by the quality of the mentioned interface, several techniques have been considered to characterize the defect/traps interface density. Among these, the most used methods are based on the measurement of impedance, and more in detail capacitance varying with voltage. These techniques are widely used in various applications ranging from semiconductor devices and solar cells [5]-[13] to batteries [14]. This method is non-destructive, and it allows a fast characterization procedure. In literatures, most part of the studies for power devices are carried out on MOS structure where it is possible to rely to low-high frequency capacitance method [15]-[19]. The capacitance behavior in MOS structure changes drastically with varying frequency [20] and this variation can give information about the defects/traps in the device under test. In fact, the inversion charge is able to follow the applied stimulus only if the frequency is sufficiently low, due to the low thermal carrier generation in the depletion region. This means that in the inversion region the behavior of the capacitance is mainly described by the inversion charge not able to follow the high frequency of the applied stimulus. The last statement holds true only in the case of MOS structure. In MOSFETs, the situation is different since the channel is refilled with carriers coming from the Source and Drani regions in the inversion region. Thus, capacitance behavior in the inversion region results not varied for low and high frequency and the low-high frequency method cannot be used in this case [21]. From the foregoing, it is clear the necessity to accurately analyze the capacitance arising from a MOSFET device. This

can be performed by means of numerical environments which enable to characterize the SiC/SiO_2 interface properties [22]-[26]. The mentioned capacitance is usually measured at the Gate terminal and connecting Drain and Source terminals [27]-[29]. In previous works [25],[30]-[33], we investigated a non-classical C-V measurements on commercially available planar SiC MOSFETs. In these studies, experimental data are obtained by applying the AC small signal on the Gate, while a fix DC bias is applied on the Drain and the Source terminal is grounded. The so obtained capacitance shows an unexpected peak in the inversion region, which can be related to the interface properties and the channel region. In this work, the capacitance trend is investigated when the applied fix Drain voltage assumes negative values. Experimental results are shown and supported by numerical analysis. The presented model is built in Sentaurus TCAD environment. An unexpected peak in capacitance behavior is found in both experimental and numerical results.

Experimental Results

Capacitance is measured on commercially available planar SiC MOSFETs, as shown in Fig. 1. The excitation signal consisting of a DC voltage ranging from -10 V to 10 V with a superimposed AC small signal, Fig. 1ii, is applied on the Gate of the device under test. A fix DC bias, Fig. 1iii is applied on the Drain, while the Source is connected to ground. The Gate capacitance measured when the Drain is biased with fix positive values is presented in Fig. 2. Capacitance has classical behavior, i.e. the case when $V_{DS} = 0$ V (dotted line), in the accumulation and depletion region. In the inversion region the situation drastically changes when $V_{DS} \neq 0$ V. A sharp peak arises, and its height is higher as V_{DS} increases. The experimental curves obtained when a positive Drain voltage is applied show a non-negligible peak centered at a voltage close to the threshold voltage. The arising peak appears more prominent as the applied Drain voltage increases. In previous works, the peak shape was associated to traps in the channel region [22] under the SiC/SiO_2 interface. The experimental data collected when the applied Drain voltage is negative are presented in Fig. 3 and Fig. 4. Such curves exhibit a different behavior from the previous case. These capacitances show a sudden decrease between the depletion and inversion region, highlighted region in the mentioned figures. The capacitance reaches its minimum for a Gate voltage which is decreasing with higher negative Drain bias. After such behavior, the capacitance increases, showing a peak in the inversion region.

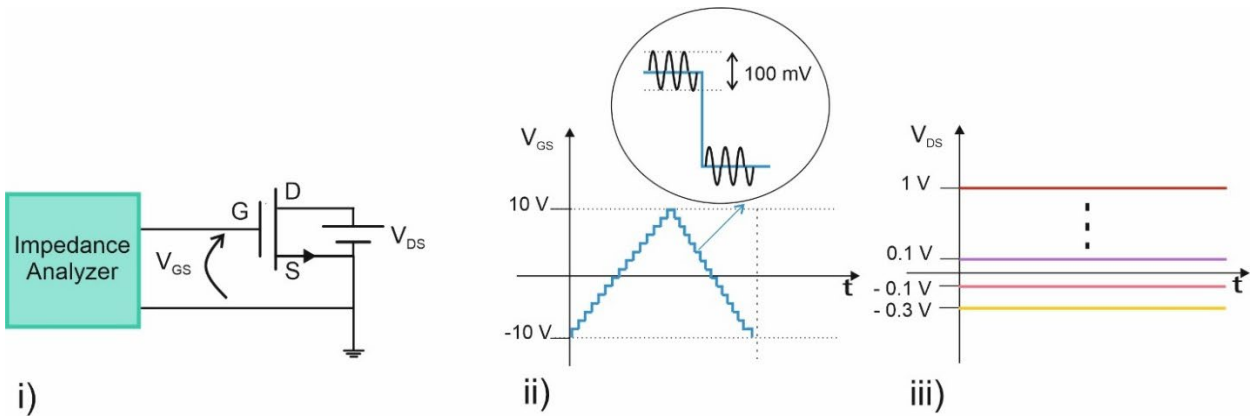

Fig. 1. i) Experimental setup; ii) Gate imposed voltage; iii) Drain applied voltage.

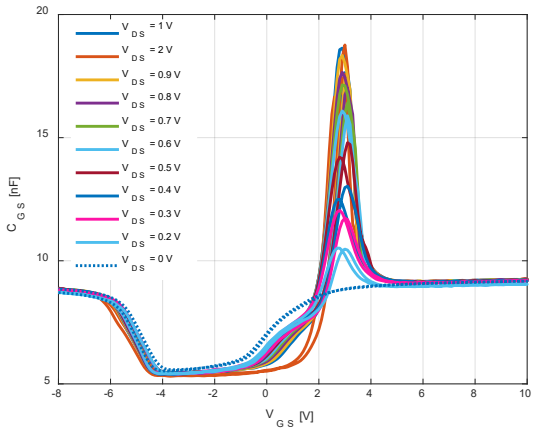

Fig. 2 Experimental C-V curves obtained from a commercial device with positive V_{DS}.

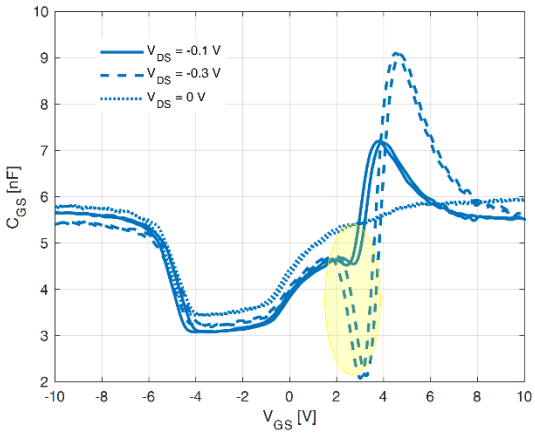

Fig. 3 Experimental C-V curves obtained from a commercial device with negative V_{DS}.

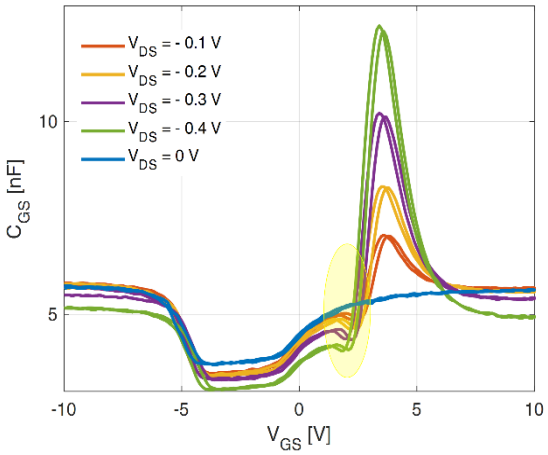

Fig. 4 Experimental C-V curves obtained from a commercial device with negative V_{DS}.

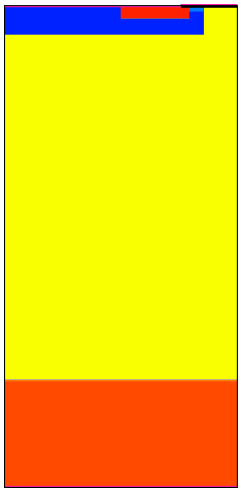

Fig. 5. Sketch of the TCAD structure.

Numerical Setup

A numerical framework has been developed in Sentaurus TCAD tool by Synopsys. The structure under test is presented in Fig. 5. The performed analysis consists in an AC small signal analysis which allows to investigate the capacitance behavior [23]. Numerical results obtained by considering both negative and positive Drain voltages are reported in Fig. 6. More in detail, the values considered for V_{DS} range from 1 V to -1 V in steps of 0.1 V. The Gate voltage has been swept from -10 V to 10 V. The AC superimposed signal has been chosen with a magnitude of 100 mV and a frequency of 100 kHz. The presented curves show similar trends to the experimental collected data. For positive Drain voltage, the capacitance peak is higher as the voltage increases, while the curves obtained with negative Drain voltage exhibit a decrease after which the behavior starts to increase again. Also, referring to the numerical results in the case of negative Drain bias, the capacitance shows a minimum at a lower Gate voltage as negative Drain voltage increases. The dependence of capacitance from interface traps when Drain is negatively biased has also been considered. More in detail a uniform traps distribution along the SiC/SiO_2 interface has been described. In the first case only acceptors traps have been considered. The capacitance trend obtained is presented in Fig. 7, for a Drain voltage V_{DS} = -0.5 V. Acceptors modify the capacitance behavior in the inversion region and, more in detail, the capacitance decreases more as traps concentration increases. The influence of donor traps has also been investigated. Numerical capacitance trends are shown on Fig. 8 for the case V_{DS} = -0.5 V. Those results show as donors modify the right part (i.e. the accumulation and depletion regions) of the capacitance curve.

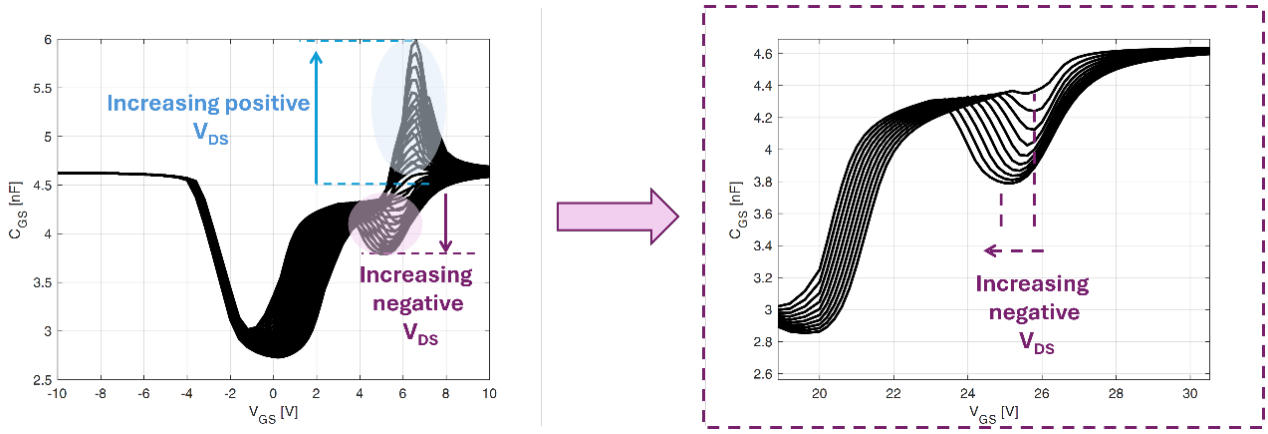

Fig. 6 Numerical C-V curves obtained with negative and positive V_{DS}.

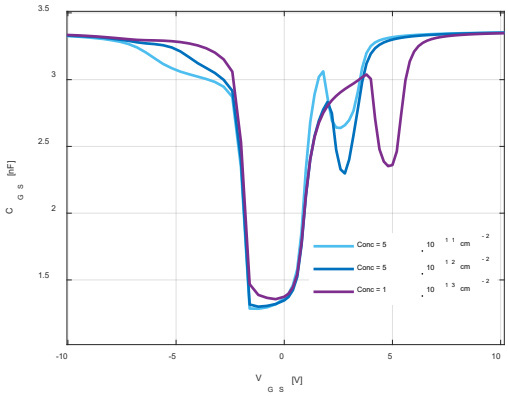

Fig. 7. Numerical C-V curves obtained with a trap distribution of acceptors.

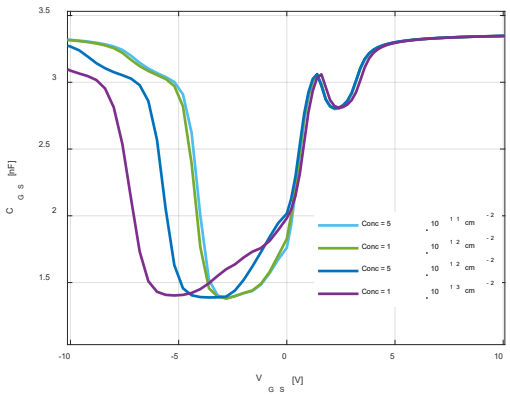

Fig. 8. Numerical C-V curves obtained with a trap distribution of donors.

Conclusions

In this work, we exploited a non-classical C-V measurement with different types of Drain biasing. More in detail, Gate capacitance is measured when a fix bias is imposed on the Drain. The Drain voltage imposed is considered both positive and negative. The resulting curves exhibit a sharp peak near the threshold voltage in either case. Experimental data are supported by numerical analysis performed in Sentaurus TCAD. Numerical results have shown similar trends to those obtained in experiments. Numerical analysis has also shown how capacitance curve measured with negative biased Drain modifies when a distribution of acceptors/donors traps is described at SiC/SiO_2 interface.

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