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A Physics-Based SPICE Model for a SiC Vertical Power MOSFET

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Abstract. Wide-bandgap silicon carbide (SiC) devices have shown great promise in power control systems due to its high efficiency and thermal stability. However, the absence of predictive compact models for SiC MOSFETs has hindered the validation of these benefits in power electronics applications through circuit simulations. To address this challenge, we introduce a physics-based SPICE model (PbSM) for SiC vertical power MOSFETs. This model is composed of basic subcircuit components that represent various regions in the MOSFET structure, which are physically modeled using a technology computer-aided design (TCAD) tool. By incorporating parasitic resistors into the PbSM, we incorporate the body effect within the MOS channel model with four terminals, thereby enhancing the capability of SPICE simulations. We include theoretical output (C_{oss}) and reverse transfer capacitances (C_{rss}) to simulate transient simulations based on a double-pulse test (DPT) setup. SPICE simulation results for static and dynamic characteristics have excellent agreement with the measured characteristics of a SiC MOSFET device, confirming the capability of the model in switching characteristics with voltage distribution across the multiple components. The PbSM shows the impact of parameter variations in switching performance, which promises valuable insights for modeling of the corner cases. Finally, the PbSM is computationally efficient, showing meaningful competitiveness compared to existing SPICE models for SiC power MOSFETs.

Introduction

Silicon carbide (SiC) has garnered significant attention in various applications due to its unique physical and electrical properties, including use in heat to electricity conversion [1], high power radio-frequency electronics [2], and power MOSFETs for switching applications [3-5]. Particularly, in the realm of sustainable energy resources, SiC power MOSFETs offers efficient power delivery with distinct advantages such as low leakage current, high efficiency, and electrical stability at high temperatures. A DMOSFET structure facilitates unipolar current operation with the source and drain electrodes vertically across a free-standing SiC substrate [6]. However, the asymmetric structure between the electrodes shows the non-linear potential distribution within the vertical structure, which poses challenges to the applicability of the equations in lateral MOSFET structures.

While empirical compact models can represent device switching behaviors in acceptable manner [7, 8], their reasonability in simulation results remains questionable due to the lack of consideration for the non-linear distribution. This limitation restricts the applicability of these models in SiC power MOSFET circuits, such as DC(AC)-DC converters [9] and motor drives [10].

In this work, we introduce a physics-based SPICE model (PbSM) that includes sub-circuit component models representing the MOS channel, junction field-effect transistor (JFET) region, p-i-n body diode, capacitors, and parasitic resistors. Using a technology computer aided design (TCAD) tool, we developed the component model structures for the distinct components within a SiC power MOSFET. The MOS channel is modeled using BSIM3 [11], which addresses short channel effects observed in sub-micron channel length (L_{ch}). The JFET is represented as a simple resistor, with its resistivity range estimated by considering the junction depletion width (W_{junc}) as a function of gate and drain biases. The higher resistivity of p-type SiC compared to p-type Si necessitates the inclusion of p-well resistors in the PbSM, thereby enhancing reverse recovery predictions affected by the body

effect in the MOS channel model. Input, output, and reverse transfer capacitances (C_{iss}, C_{oss}, and C_{rss}, respectively) are modeled based on bias-dependent W_{junc}. The PbSM is validated by comparing static and dynamic behaviors with the measurements from a SiC MOSFET device. Finally, the PbSM demonstrates the capability to simulate and predict circuit behaviors with varying model parameters used in the components.

Results and Discussion

Low- and High-drain Voltage Operation of a SiC power MOSFET.

Figure 1a) describes the simplified schematic of a SiC power MOSFET, modeled using a TCAD suite. The arrows illustrate the flow of electrons at a turn-on bias condition, passing through the MOS channel, spread (dashed-line arrows), drift (straight solid-line arrows), and substrate. The space charge region (SCR) is generated at the p-n junction, and the W_{junc} is expressed by:

$$W_{junc} = \sqrt{\frac{2\varepsilon_{SiC}\varepsilon_0}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)\left(\phi_{bi}+V_j\right)}, \quad (1)$$

where q is the electric charge, ε_{SiC} is the relative permittivity of SiC (9.7), ε_0 is the permittivity of vacuum, N_a and N_d are the carrier concentration in p- and n-type regions, ϕ_{bi} is the built-in potential, and V_j is the bias dropped at the junction. The W_{junc} mainly relies on V_j, which critically controls the conductivity of the spread region, where the current is distributed to the SiC substrate. Under reverse bias to the junction, the expansion of W_{junc} to the substrate reduces the depth of the drift region (t_{drift}). Thus, both the spread and drift regions are affected by the W_{junc}, being retreated as a JFET region. The substrate is far away from the edge of W_{junc}, thereby acting as a free-standing resistor. Overall, the electrons travel from the source to drain across different regions, implying that native MOSFET models in SPICE, which traditionally target symmetric planar MOSFETs, are not compatible with the vertical DMOSFET structure.

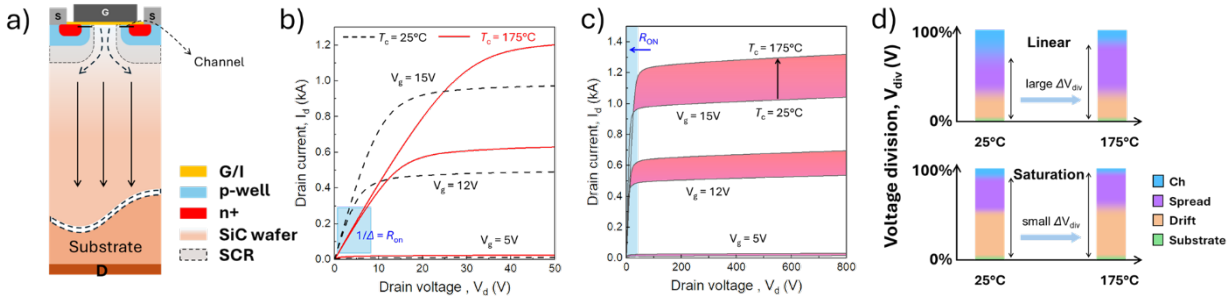

Fig. 1. a) Cross-section for a SiC power MOSFET. The arrows indicate the flow of electrons when the MOS channel is turned on. G/I: Gate insulator, SCR: Space charge region. b) TCAD simulations for I_d-V_d characteristics under 25°C and 175°C. The gate voltage (V_g) varies from 5 to 15V. The blue box indicates the region of $R_{ds,on}$. c) I_d characteristics with V_d extended up to 800V. The color-shaded regions indicate the enhanced I_d via the increase of temperature in the saturation region. d) Illustration of voltage division (V_{div}) in linear (top) and saturation (bottom) regimes across different regions of MOS channel (Ch), spread, drift, and substrate.

Figure 1b) represents the simulated I_d-V_d characteristics using the TCAD structure. The gate voltages (V_g) range from 7V to 15V, and the cell temperatures (T_c) vary from 25°C to 175°C. At V_d < 10V, the applied voltage is primarily dropped across the spread and drift regions. The reciprocal of the slopes determines the on resistance (R_{on}). As T_c increases, R_{on} also rises due to the increased resistivity in the spread and drift regions. This leads to a positive shift in the boundary between linear and saturation regions. Figure 1c) shows the simulation with V_d extended up to 800V. In the saturation regime (out of the blue box), I_d is proportional to T_c due to the increase in field-effect mobility (μ_{FE}) in the MOS channel, which is dominated by the Coulomb scattering near the interface of SiO_2/SiC [12]. The slope of the curve is influenced by channel length modulation (*CLM*) and JFET conductivity.

A steeper slope indicates lower output resistance, $r_o = 1/(\lambda I_d)$ (λ is the parameter related to the early voltage), resulting in higher sensitivity of ΔI_d to ΔV_d. It affects the operating points and the sharpness of switching on/off states. Thus, understanding *CLM* and JFET conductance at high V_d is critical for analyzing the transient responses of the MOSFET. Based on the I_d-V_d characteristics, Figure 1d) shows the distribution of applied V_d (assuming strong inversion in the MOS channel) across the multiple regions in linear (top) and saturation (bottom) regimes. The ratio of voltage division (V_{div}) across the different regions is strongly dependent on T_c and the operation modes (linear versus saturation), highlighting the importance of interpreting the non-linear voltage distribution in SiC MOSFETs for analyzing their physics-based electrical characteristics.

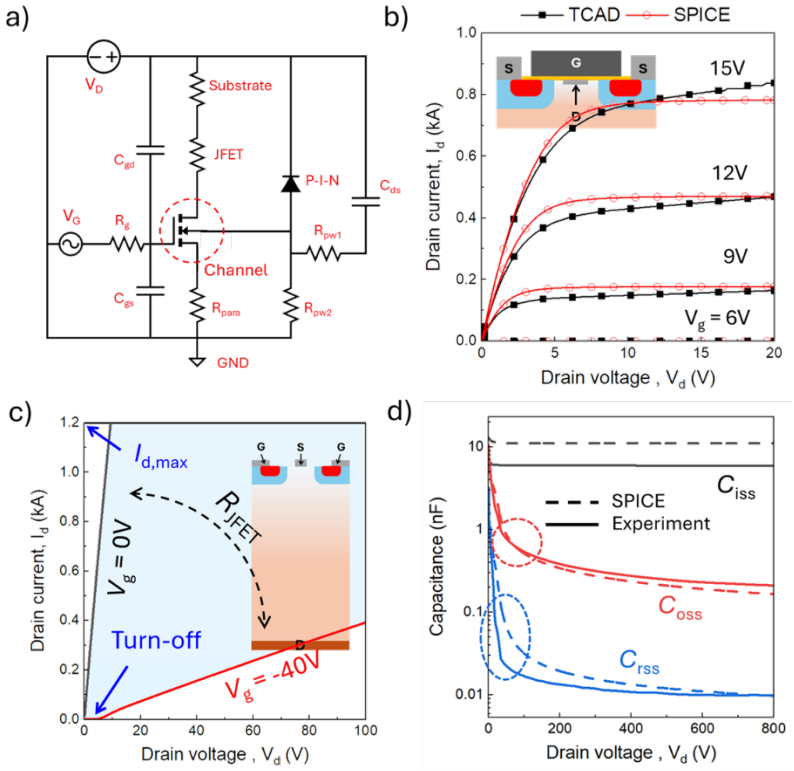

Fig. 2. a) Schematic of the physics-based SPICE model (PbSM). b) Simulated I_d-V_d characteristics of the MOS channel model using the SPICE and TCAD. c) Simulated I_d-V_d characteristics of the JFET model using the TCAD. V_g varies from 0 to – 40V, corresponding to the estimated V_{div} in the MOS channel. The dashed arc arrow indicates the possible resistance (reciprocal of the slope) variation window. The 'turn-off' means zero I_d when the spread region is pinched-off. d) Input (C_{iss}), output (C_{rss}), and reverse transfer (C_{rss}) capacitance models. The capacitances were calculated based on doping concentration and effective device area.

SPICE Model with Sub-circuit Components.

Figure 2a) shows the schematic of the PbSM. The MOS channel is modeled using BSIM3, integrated with parasitic resistors (R_{para}) associated with metal contacts and n^+-doped region. A JFET resistor (R_{JFET}), representing the spread and drift regions, is connected to the MOS channel. The substrate, with relatively high carrier concentration, is modeled as a resistor (R_{sub}), which does not significantly influence the impedance of the circuit. The three capacitances – C_{gs} (gate to source), C_{gd} (gate to drain), and C_{ds} (drain to source) – are connected between the electrodes. The p-i-n diode is modeled by the Compact Model Coalition (CMC) diode model [13]. The gate resistor (R_g) is connected to the gate and governs the interaction between the gate capacitance and parasitic inductance.

The components in the circuit are modeled using sub-circuit device models derived from a TCAD analysis performed on the SiC power MOSFET structure shown in Fig. 1a). Figure 2b) compares the I_d-V_d characteristics of the four-terminal MOS channel device simulated using the TCAD and SPICE tools. The body bias was set to zero. The inset shows the schematic of the TCAD-based MOS channel

structure. The linear region is closely matched between the two models, indicating that the MOS channel model in the SPICE fits the transconductance (g_m) to the TCAD results. The *CLM* is sensitive to V_d, contributing to short channel effects such as drain-induced barrier lowering (DIBL), which are captured using key model parameters in BSIM3, as outlined in Table 1.

Table 1. BSIM3 model parameters with the effect on current-voltage characteristics.

Parameters	Effect
ETA0	DIBL effect coefficient at the subthreshold region
U0, Ua, Ub	Coefficients for the field-effect mobility shape
RDSW	Effect of a parasitic resistance at low V_d
DELTA	Smoothness of the curvatures at non-linear region in I_d-V_d
PCLM	Regulation of the early voltage due to channel length modulation
etc.	Other parameters such as VTH0 and doping-relevant values are estimated from the TCAD simulation.

In the saturation region, the $\Delta I_d/\Delta V_d$ is controlled by the model parameters of DELTA and PCLM. Modeling of this variation is important for representing the output conductance ($g_{ds}=\partial I_{ds}/\partial V_{ds}$) of a SiC MOSFET at high V_d. The threshold voltage (V_{th}) is defined using a model parameter, VTH0, in BSIM3. Physically, V_{th} is expressed by:

$$V_{th} = V_{FB} + \phi_s + \frac{Q_{dep}+Q_{fix}}{C_{ox}}, \tag{2}$$

where V_{FB} is the flat-band voltage and ϕ_s is the surface potential, Q_{dep} and Q_{fix} are the depletion and fixed charges in the MOS channel and gate oxide, respectively. BSIM3 has the limitations in modeling Q_{fix} and interface traps, which affect the subthreshold region and not fully represented in BSIM3.

Figure 2c) presents the I_d-V_d characteristics of the JFET, with the inset showing a schematic of the TCAD-based JFET, including its electrodes of gate, source, and drain. In this JFET, the potential difference between the source and gate corresponds to the voltage drop across the MOS channel (V_{ch}) in the SiC power MOSFET. The TCAD simulation estimates that the V_{ch} can reach up to 40V. Accordingly, the JFET simulation varies V_g from 0V to -40V, resulting in the arc-shaped variation in I_d curves. The amplitude of I_d is limited to less than 1.2 kA, reflecting the meaningful maximum operating current of the SiC power MOSFET, as shown in Fig. 1c). In the SPICE model, the R_{JFET} is simplified as the reciprocal of the slope corresponding to V_g = 0V in the JFET. However, it is worth noting that using a variable R_{JFET} could improve the accuracy of the voltage division in the SPICE simulation.

Figure 2d) illustrates the modeled C_{iss}, C_{oss}, and C_{rss}, which are compared to experimental results using a SiC MOSFET device. As V_d increases, the neutral portion of the spread area is reduced due to the expansion of the W_{junc} by the Eq. (1), leading to a general decrease in C_{oss} due to the reduction of the C_{gd} and C_{ds}. C_{ds} is simply modeled using the Eq. (1). The C_{gd} is composed of the gate oxide (C_{ox}) and SiC (C_{SiC}) capacitances in parallel, expressed as:

$$C_{gd} = C_{ox} || C_{SiC} = \frac{C_{ox} \cdot C_{SiC}}{C_{ox}+C_{SiC}}, \tag{3}$$

where C_{SiC} forms across the spread, drift, and substrate. When the W_{junc} becomes large enough to fully occupy the spread and drift regions, kink regions, marked by circles, appear. These kinks are caused by the addition of C_{junc} into C_{gd}, as well as non-linear doping profile across the C_{SiC} regions. The overlapped regions between electrodes remain fixed during the simulation. For simplicity, C_{gs}

was set to a constant value, assuming strong inversion in the MOS channel. In a real MOSFET, V_{gs} reaches the threshold voltage, then C_{gd} becomes more crucial in determining the switching performance of the MOSFET, particularly during the gate voltage plateau period [14]. Currently, using a constant C_{gs} does not significantly impact the switching simulation.

SPICE Model Generation for a SiC MOSFET.

Figure 3a) represents the I_d-V_d characteristics with V_g ranging from 9V to 15V, simulated by the SPICE model (red-dashed lines), and compared to TCAD results (solid lines) and measurements (symbols) for a SiC power MOSFET. The results align closely without significant discrepancies, although the subthreshold region, which is governed by traps at the gate oxide interface, is not yet accurately modeled. Figure 3b) extends the I_d-V_d characteristics into the saturation regime, with V_d up to 800V. Due to power dissipation at high voltage and high current regions, measurements were not performed at this high V_d range and TCAD simulation results were used instead of experimental values. The I_d is unipolar and identical to the current flowing through the MOS channel model. Therefore, the slope at high V_d corresponds to the saturation mode in the MOS channel mode, and balancing the voltage division in the PbSM is important for controlling the operation points. It is important to note that $\Delta I_d/\Delta V_d$ in the saturation region determines the sensitivity of g_{ds} and the sharpness of the transient response. This indicates that the modeling of R_{JFET} as a function of V_{ch} remains a topic for future work. Figure 3c) shows the I_d-V_d at the third quadrant, where the current paths through the body diode or MOS channel are precisely modeled to match the measurements. As discussed earlier, the subthreshold region in the MOS channel is not properly modeled yet, resulting in the mismatch at a $V_g = 5$V. In addition, the reverse recover charges (Q_{rr}) and time (t_{rr})are empirically modeled [13] at a $V_g = -4$V.

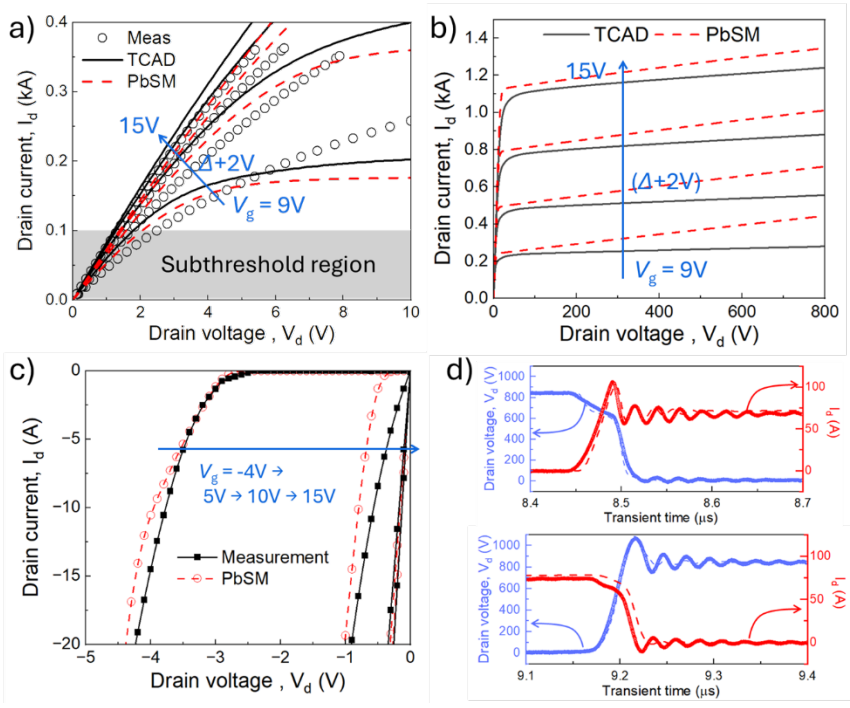

Fig. 3. a) Simulated I_d-V_d characteristics using the PbSM in the linear region, compared to the TCAD and measurements using a SiC MOSFET. b) Simulated I_d-V_d characteristics of the PbSM with the extended V_d up to 800V, compared to the TCAD. c) Simulated I_d-V_d characteristics of the PbSM, compared to the measurement. d) Double-pulse test (DPT) simulations (dashed lines) compared to measurements (symbols). The top and bottom graphs indicate the turn-on and turn-off status, respectively.

Figure 3d) presents the transient performance of turn-on (top) and turn-off (bottom) from the SPICE simulation (solid line) and measurement (symbols) using the MOSFET. The dynamic switching behavior was characterized through a Double-Pulse Test (DPT) [15]. The DPT simulation was conducted using a circuit that includes the MOSFET SPICE model along with the parasitic components from the DPT setup [16]. The SPICE results closely match the measurements, including the increase in drain current with each subsequent gate pulse. The *di/dt* and *dv/dt* values are very well-matched, meaning the reasonable design of key factors such as g_m, C_{gd}, and C_{ds}. The measurement was conducted at 25℃, with the effect of reverse recovery considered negligible.

SPICE Corner Models via Parameter Variations.

Figure 4a) illustrates the generation of several SPICE models based on device parameter variations implemented in the PbSM. The turn on/off regions are particularly sensitive to these variations and the voltage division ratio among the different components. Figure 4b) shows the impact of device parameters on E_{on} and E_{off}. For example, a reduction of C_{oss} shortens the charging time, resulting in faster switching characteristics and decreased energy losses. An increase in V_{th} requires a higher V_g and lowers the switching speed, leading to an increase in E_{on}, but conversely, a decrease in E_{off}. These are directly influenced by manufacturing processes such as gate oxide thickness, ion implantation, and other critical dimensions. The PbSM captures the trend of energy loss variations based on these process variations. Using the DPT method, Figure 4c) demonstrates the turn-on (top) and turn-off (bottom) characteristics. It assumes the variation of the width in the spread region (W_{sp}), changing C_{oss} with an arbitrary variation range of ±20%. Compared to the turn-on, the discharging amount between the drain to source and gate becomes more important in the turn-off, and it results in the noticeable positive or negative shifts.

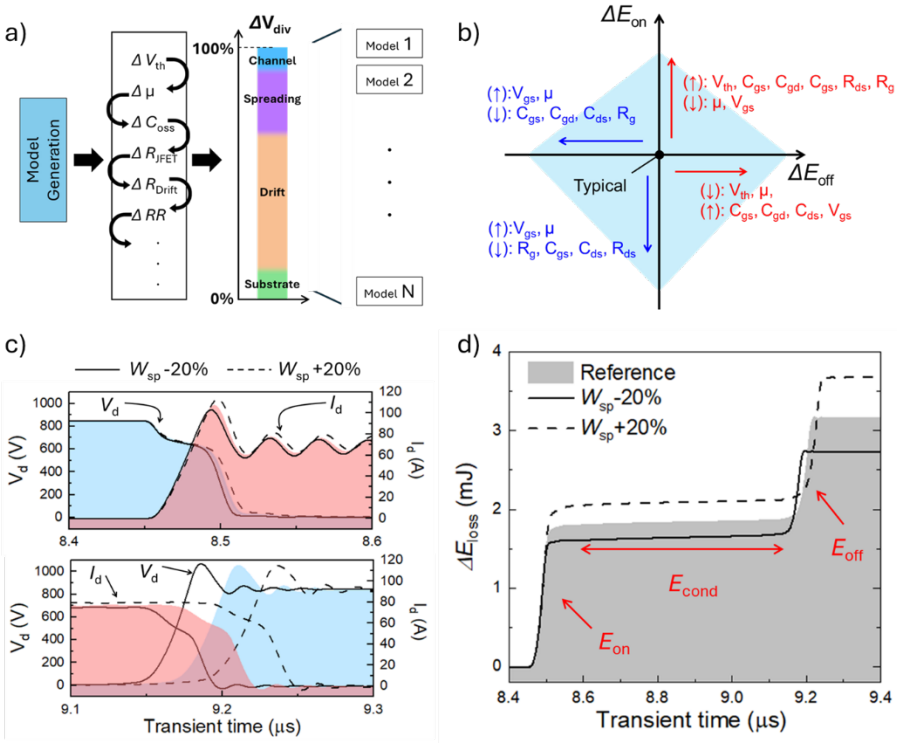

Fig. 4. a) Illustration of the impact of device parameter variations in the V_{div} and different model generations. b) Impact of the parameters on E_{on} and E_{off}. c) Example of switching performance variations via the change (±20%) in the width in the spread region (W_{sp}). The simulation used the same DPT method in Fig. 3c), which are represented by the color contours. d) Change of the relative energy loss (ΔE_{loss}) during the transient time in c). The arrows mean the regions of on, conduction, and off status.

Figure 4d) illustrates the change of the relative energy loss (ΔE_{loss}) during the transient time. It intuitively indicates reduced energy loss with a lower W_{sp}. The PbSM shows high sensitivity via individual parameter variations on switching performance. However, the relationships between different parameters are uncertain (can be strongly correlated or orthogonal), which can either amplify or counterbalance the min-max ranges in corner cases. Therefore, analyzing statistical data from manufacturing is crucial to reveal the correlations between device parameters and to project the corner models using the PbSM for SiC MOSFETs.

Evaluation of Computational Efficiency.

Table 2 presents a performance comparison between the existing model currently available on Wolfspeed website [17], which is more behavioral with empirical fitting , and the PbSM a SiC for power MOSFET. The test circuit is a 100 kHz, 10 kW interleaved boost converter, and transient simulation analysis was performed with a total circuit run time of 50 milliseconds using LTSpice. The circuit details are provided in the previous result [18]. Compared to the existing model, the iteration numbers for transient analysis decreased by approximately 6%. The total number of transient points evaluated increased by about 11%. Therefore, the computation points were not significantly different between the models. Notably, the clock time for the PbSM is only about 50% higher than the behavioral model, indicating a relatively small computational penalty for additional capability of representing physical variability of the PbSM.

Table 2. Comparison of SPICE simulation computation between a previous model and PbSM.

Test items	PbSM	Existing model [18]
Total number of Newton iterations	219,313,034	299,618,943
Iteration numbers for transient analysis	219,313,024	299,618,933
Transient points evaluated	105,924,496	109,740,265
Clock time	5.1 hours	3.2 hours

Summary

This work presents a SPICE model, named PbSM, for SiC power MOSFETs, designed using physics-based sub-circuit components such as the MOS channel, JFET, and parasitic resistors. The sub-micron L_{ch} is primarily modeled using BSIM3, which controls the onset of Miller plateau region. The JFET, representing the spread and drift regions, is currently modeled as a constant resistor, which does not compromise accuracy of switching simulations. The PbSM effectively distributes the applied voltage across the different components, aiding in the understanding of key model parameters that determines the I_d-V_d characteristics. Physics-based C_{oss} and C_{rss} closely match measurements from a SiC MOSFET device, which are important for designing turn-on/off states. The PbSM simulations depict I_d-V_d characteristics, with the linear region validated through comparison with measurements. Though the saturation region falls beyond the scope of validation, we identify that *CLM* and JFET conductivity are critical for regulating $\Delta I_d/\Delta V_d$. A DPT circuit, designed using the PbSM, simulates switching behaviors that align closely with measurements across the turn on, conduction, and turn off regions. The PbSM is capable of tracking trends in physics-based variations of energy losses via parameter changes, paving the way for the generation of corner models that accounts for manufacturing process variations. Finally, we propose this model with the enhanced representations of device physics, providing a powerful tool for further investigation of SiC power MOSFET applications.

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