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A Novel 'Ladder' Design for Improved Channel Density for 1.2kV 4H-SiC MOSFETs

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Abstract. A novel topological layout was developed to enhance the channel density of 1.2kV 4H-SiC MOSFETs. The innovative "Ladder" MOSFET incorporates an additional JFET and channel region, arranged orthogonally within the layout. To ensure a fair comparison, identical design rules were applied to both the Nominal and Ladder MOSFETs, resulting in calculated channel densities of 0.30 and 0.41, respectively. Comparative analysis was conducted using Synopsys Sentaurus TCAD simulations, where three dimensional (3D) structures for both designs were generated under the same implantation and process conditions, followed by simulations of static electrical characteristics. The results indicate that the Ladder MOSFET achieved approximately 10% reduction in specific on-resistance ($R_{on,sp}$) compared to the Nominal MOSFET. Both MOSFET designs were subsequently fabricated, packaged, and evaluated, with the Ladder MOSFET demonstrating a 12.94% reduction in $R_{on,sp}$ when comparing the best-performing devices from each design.

Introduction

4H-SiC's superior material properties enable thinner, more heavily doped drift layers that can withstand high breakdown voltages, resulting in lower specific on-resistance ($R_{on,sp}$) and making unipolar devices more viable compared to silicon-based counterparts. Consequently, 4H-SiC MOSFETs have emerged as a promising alternative to Si IGBTs, primarily due to their low $R_{on,sp}$ and rapid switching capabilities [1]. The adoption of 4H-SiC MOSFETs can enhance converter efficiency and reduce cooling requirements, facilitating high-frequency operation [2]. However, the anticipated reduction in $R_{on,sp}$ for SiC MOSFETs has not fully materialized, largely due to poor channel mobility caused by high interface state density (Dit). Despite significant improvements in channel mobility through post-oxidation annealing in nitric oxide (NO) ambient [3] and the use of accumulation mode channels [4], the typical channel mobility in the SiC industry remains around 20-30 $cm^2/V{\cdot}s$ for planar MOSFETs. As a result, channel resistance continues to be the dominant limiting factor for 1.2 kV 4H-SiC MOSFETs [5].

Increasing the channel density is an effective strategy in reducing the total channel resistance within the MOSFET, by increasing the number of current pathways during the on-state. As a result more current is allowed to flow, reducing the total $R_{on,sp}$ of the device. Modifying the channel density is primarily achieved through innovative topological designs within the active region of the MOSFET. These designs have evolved considerably from the traditional stripe pattern, leading to several novel approaches. One approach involves isolating the P+ implanted region by placing it periodically in the orthogonal direction in the unit cell layout. This allows for an overall reduction in cell pitch, and thus a reduction in $R_{on,sp}$ due to the increased channel density [6]. Other approaches include using non-linear cell designs such as the square, hexagonal, or octagonal cell layouts which further increase channel density by using non-linear geometries [7]. However, these non-linear designs can lead to geometries within the unit cell that can negatively impact device performance. [8]. In this paper, a novel 'Ladder' design is presented which increases the channel density while maintaining a linear layout to prevent degradation with other device characteristics.

Device Design

The proposed Ladder MOSFET incorporates an additional JFET and channel region, inserted orthogonally within the layout, as illustrated in Fig. 1. The key benefit of this additional JFET and channel region is the large increase in channel density. The channel density is calculated by dividing the area of the gate overlap over the channel and N+ region, and dividing it by the total unit cell area. The resulting channel density was calculated to be 0.30 for the nominal MOSFET and 0.41 for the ladder MOSFET. In order to fairly compare the Nominal and Ladder layouts the same design rules were used, with a channel length (L_{ch}) of 0.5 µm and a half JFET width (W_{JFET}) of 0.6 µm. However, the ladder layout requires an increase in the half contact width (W_C) from 0.7 µm to 0.9 µm to maintain the same JFET design.

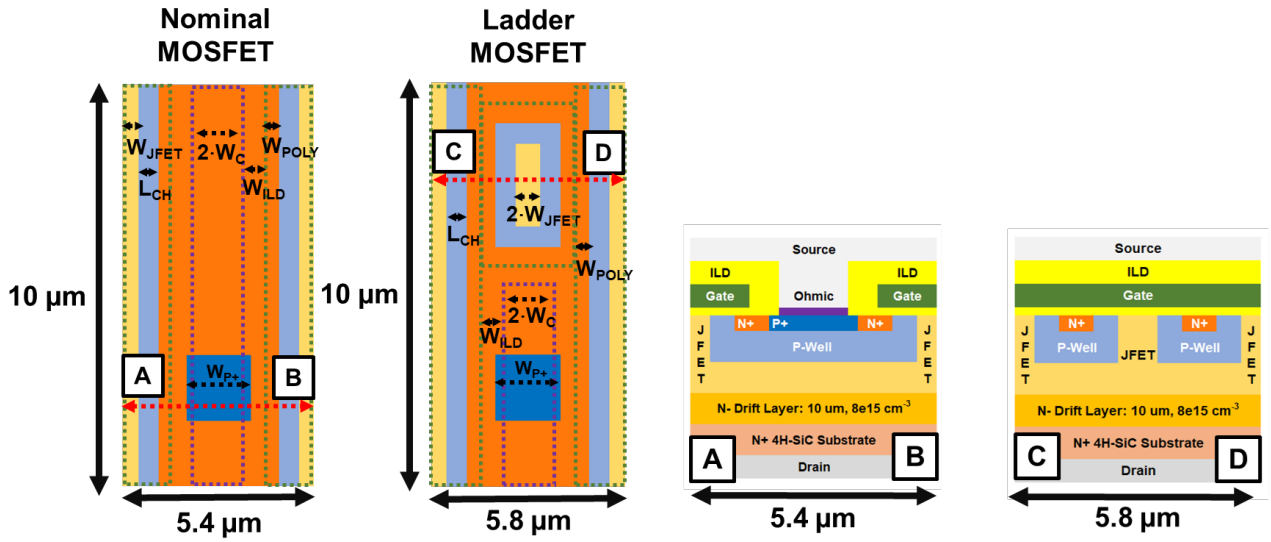

Fig. 1. Comparison of Nominal and Ladder MOSFET layout designs, with W_C of 0.7 µm and 0.9 µm and cell pitches of 5.4 µm and 5.8 µm, for the Nominal and Ladder MOSFETs respectively.

3D TCAD Simulations

3D Synopsys Sentaurus TCAD simulations were employed to conduct a comparative analysis between the Nominal and Ladder MOSFET structures, as it is not possible to fully compare these two different device types only using 2D simulations. 3D doping profiles were generated under identical implantation and process conditions using SProcess [9] as depicted in Fig. 2 for both the Nominal and Ladder MOSFETs. To obtain an accurate implantation profile, fine box meshing had to be applied near the interface. However, this kind of fine meshing cannot be used in SDevice as the simulation would have difficulty converging. Thus, a larger adaptive meshing was developed to prepare the devices for simulation, leaving finer meshing near the interface in the channel region, while increasing the mesh size further down in the MOSFET.

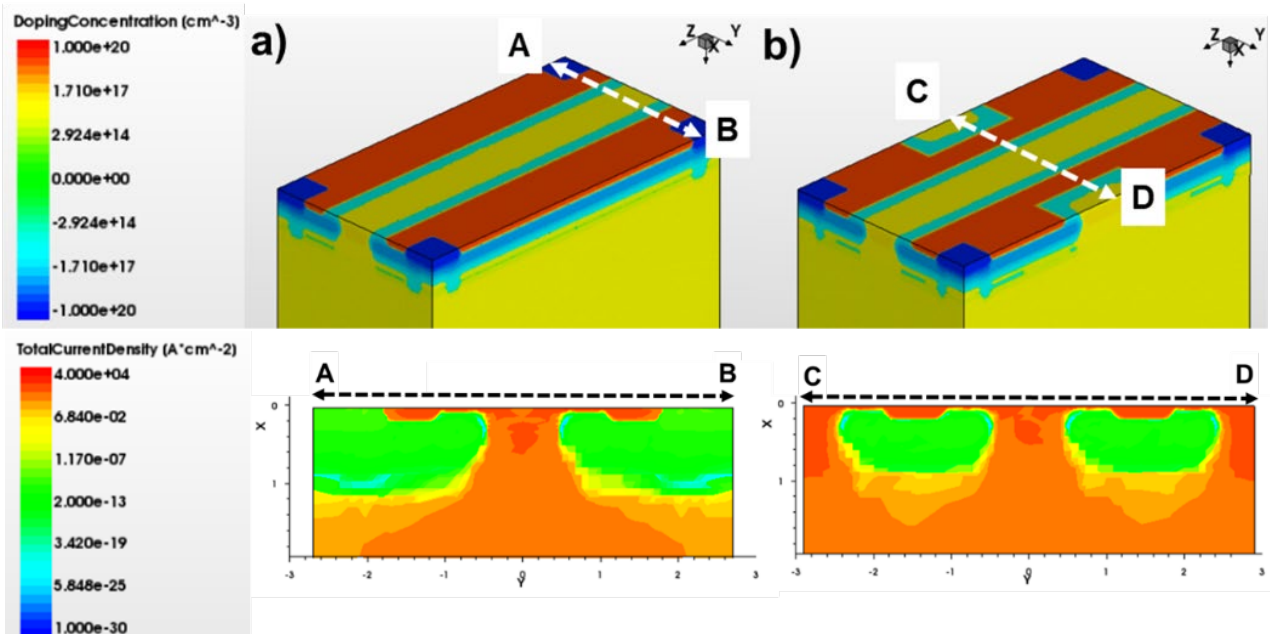

Fig. 2. 3D unit cell structures generated for the (a) Nominal and (b) Ladder MOSFETs, using the same implantation and process conditions. The current density distribution is plotted for cross-sections A-B and C-D at V_G = 20V and V_D= 1.5 V. Notably, cross-section C-D illustrates the utilization of the additional ladder region by the current, thus validating the Ladder Design.

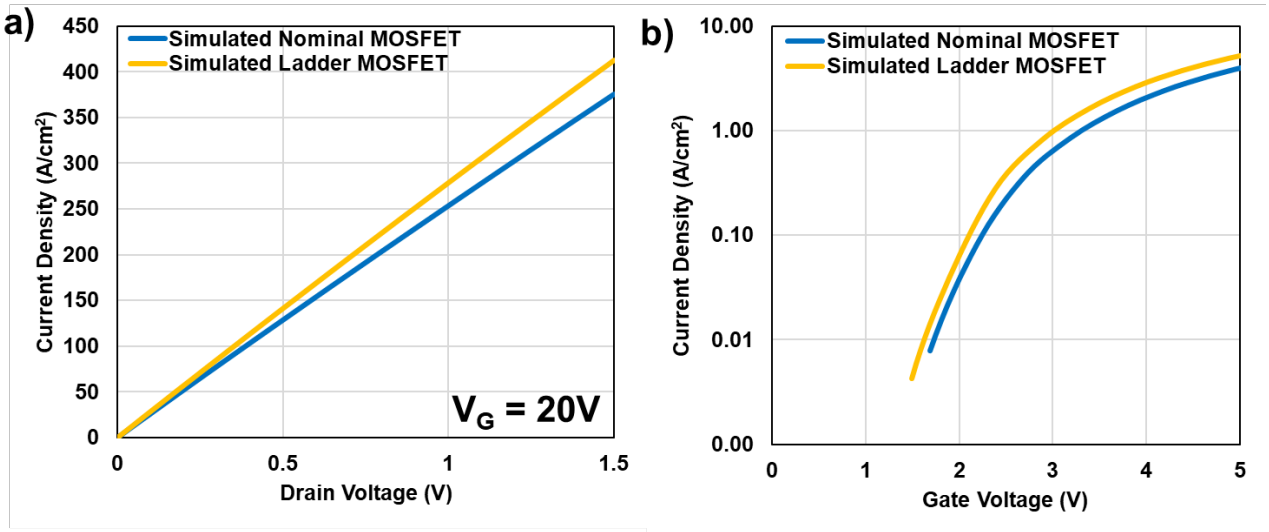

Fig. 3. Simulated (a) output and (b) transfer characteristics for the Nominal and Ladder MOSFETs.

Subsequently, forward and transfer characteristics were simulated using SDevice [10]. The forward characteristics were simulated by first sweeping the gate voltage (V_G) to 20 V and then sweeping the drain voltage (V_D) to 1.5 V. The specific on-resistance ($R_{on,sp}$) was calcualted to be 3.96 mohm·cm^2 and 3.60 mohm·cm^2 for the Nominal and Ladder MOSFETs, achieving a 10% reduction in $R_{on,sp}$ as seen in Fig 3 (a). In Fig 2. Cross sections A-B and C-D from the Nominal and Ladder MOSFETs, respectively, are shown with the total current density plotted at V_D = 20 V and V_D = 1.5 V. Cross-section C-D reveals that current flows through the additional conduction path created by the Ladder region. However, the current density is higher in the Ladder region's JFET compared to the nominal JFET because the Ladder's JFET region is shorter in the z-direction. The nominal JFET region extends continuously to the adjacent unit cell, while the Ladder region's JFET is only 2.0 µm long. Although the resistance of the Ladder JFET is greater due to the narrower opening, the Ladder region still reduces overall $R_{on,sp}$ because it provides a parallel current path to the nominal JFET. The threshold voltage (V_{th}) was found to be 2.53 V and 2.33 V for the Nominal and Ladder MOSFETs, respectively, when assessed at V_D = 0.1 V and I_D = 1 mA as seen in Fig 3 (b).

Experimental Results

Both Nominal and Ladder MOSFETs were fabricated on 1.2kV rated epi-layer with 360 µm 4H-SiC substrates at Clas-SiC Wafer Fab in the United Kingdom, employing identical process flows and implantation recipes. A self-align process was implemented to form the Pwell/Channel. No backside grinding was conducted to thin the substrate after fabrication. Subsequently, the wafers were diced, and from each, 15 Nominal and 10 Ladder MOSFETs were selected and packaged in TO-247s.

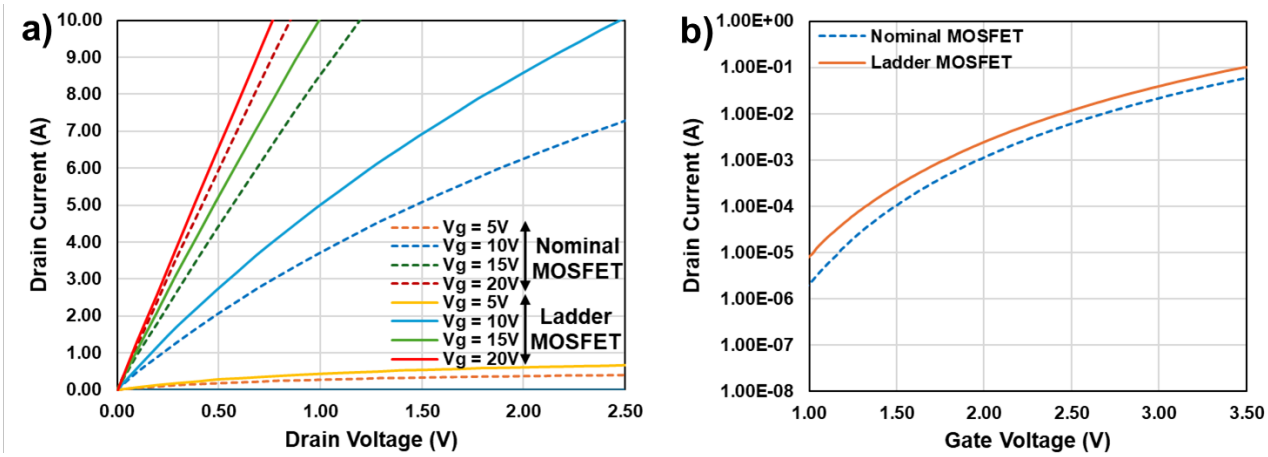

Fig. 4. Measured (a) output characteristics and (b) transfer characteristics for the fabricated Nominal and Ladder MOSFETs. The $R_{on,sp}$ is 3.84 and 3.40 mohm·cm^2 when measured at V_G = 20V and I_D = 15 A for the Nominal and Ladder MOSFETs, respectively. The V_{th} is 2.44 V and 2.20V when measured at V_G = V_D and I_D = 5mA for the Nominal and Ladder MOSFETs, respectively.

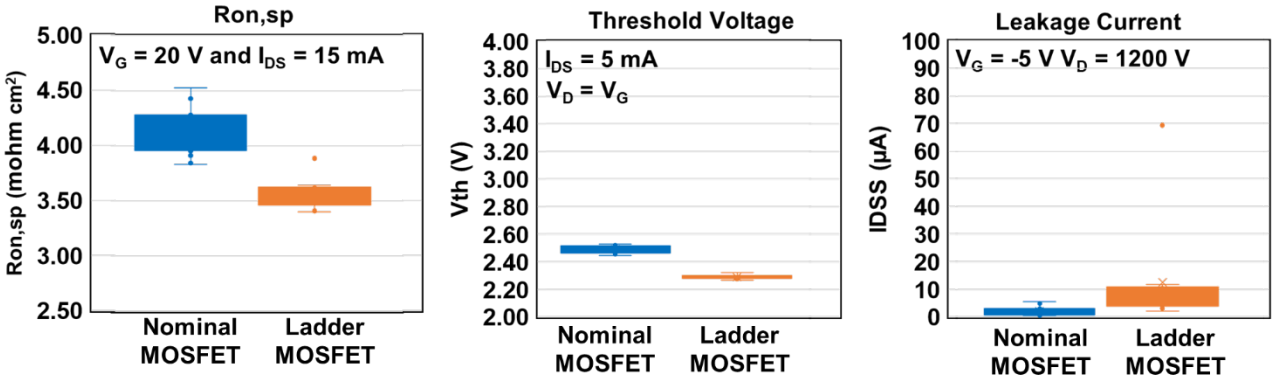

Fig. 5. A direct comparison of the Output, Transfer, and Blocking characteristics for 15 Nominal and 10 Ladder MOSFETs. The Ladder MOSFETs show a 15.39% reduction in the $R_{on,sp}$ with only a 8.81% reduction in V_{th}. The Ladder MOSFET shows only a marginal increase in leakage current compared to the Nominal MOSFET with same breakdown voltage of 1570V.

Comprehensive measurements of static electrical characteristics were conducted. At V_G = 20V and Drain Current (I_D) = 15 A the $R_{on,sp}$ for the best performing Nominal and Ladder MOSFETs was measured to be 3.84 mohm·cm^2 and 3.40 mohm·cm^2, showcasing a notable 12.94% reduction in $R_{on,sp}$ for the Ladder MOSFET. The typical output characteristics of these selected MOSFETs are illustrated in Fig. 4. Overall, Ladder MOSFETs exhibited an average reduction of 15.39% in $R_{on,sp}$ compared to their Nominal counterparts, as evidenced in Fig. 5. Additionally, the average threshold voltage (V_{th}) at I_D = 5mA and when V_G=V_D was measured to be 2.49 V and 2.29 V for the Nominal and Ladder MOSFETs, respectively.

The improvement of $R_{on,sp}$ achieved through the utilization of the Ladder MOSFET design is consistently sustained even at elevated temperatures, as depicted in Fig. 6. It is interesting to observe that the temperature coefficient of the Ladder MOSFET is smaller than that of Nominal MOSFET, which may be attributed to wider contact opening.

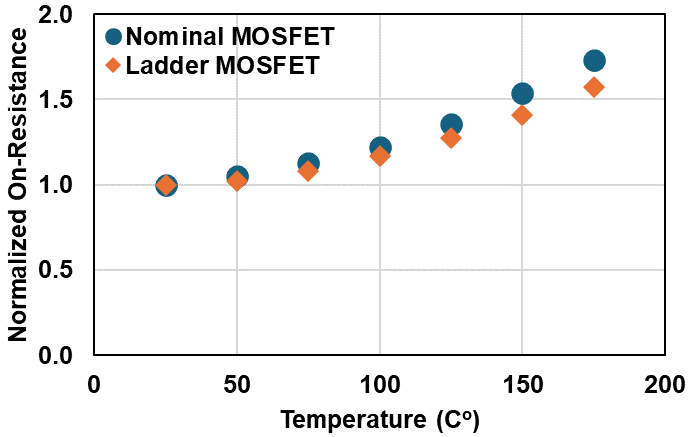

Fig. 6. Normalized on-resistance values at varying temperatures for a typical Nominal and Ladder MOSFET. The Ladder MOSFET exhibits a slightly better temperature coefficient.

Discussion

The Ladder MOSFET consistently outperforms the Nominal MOSFET in terms of $R_{on,sp}$ with both the simulated and experimental results, revealing that the Ladder layouts larger channel density results in a significant decrease in the $R_{on,sp}$. Fig 7. (a) depicts the current density at V_G = 20 V for both simulated and best-performing fabricated Nominal and Ladder MOSFETs. The transition to the Ladder design yields similar improvements in $R_{on,sp}$ for both sets of MOSFETs, with reductions of 10% and 12.94%, for the simulated and fabricated devices respectively. Similarly, the transfer characteristics also show a similar trend between the simulated and fabricated MOSFETs. Fig 7. (b) shows the current density for the transfer measurement when V_D = 0.1 V and I_D = 1mA. The V_{th} was found to be 2.53 V and 2.33 V for the simulated Nominal and Ladder MOSFETs and 2.46 V and 2.24 V for the best performing fabricated Nominal and Ladder MOSFETs.

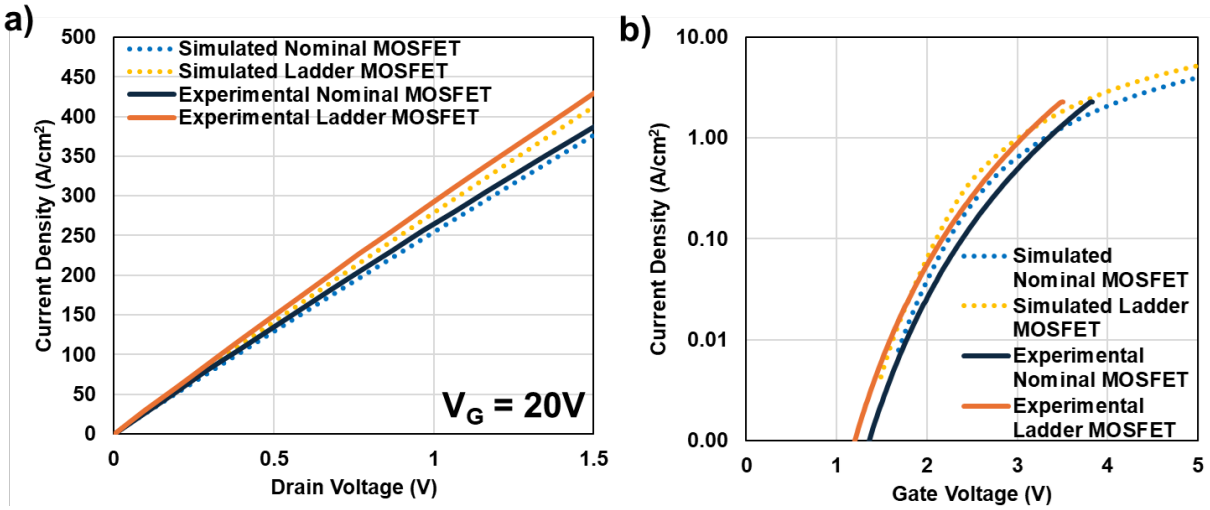

Fig. 7. (a) Output characteristics and (b) transfer characteristics compared for the simulated and fabricated Nominal and Ladder MOSFETs. A comparable improvement in $R_{on,sp}$ is observed with fabricated Ladder MOSFETs.

The 3D simulation results closely mirror the trends observed with the fabricated MOSFETs, confirming the value of 3D TCAD simulations for predicting performance in novel device designs. This breakthrough enables new device concepts to be quickly assessed and optimized prior to fabrication, avoiding the high costs associated with fabricating different device splits. This method also enables the elucidation of trends and the identification of potential flaws in the layout early on. Overall, the use of 3D TCAD simulations makes device design more efficient and cost effective.

Conclusion

This study presents a novel 'Ladder' MOSFET design for 1.2kV 4H-SiC MOSFETs. This new layout includes an additional JFET and channel region which significantly increases the channel density. Through both 3D TCAD simulations and experimental measurements, the Ladder MOSFET demonstrates superior $R_{on,sp}$ compared to the Nominal design. Providing another avenue for further improving the efficiency of SiC power devices. Further work should focus on further optimizing the Ladder design, exploring its effect on dynamic characteristics and reliability, and investigating its impact on lower voltage devices where the channel and JFET resistances make up a larger share of the overall $R_{on,sp}$.

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