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Single-Event-Burnout in 1.2kV 4H-SiC Lateral RESURF Power MOSFET

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Abstract. Extensive experiments and simulations indicate that Single-Event ion bombardment Effects (SEE) can trigger a Single-Event Burnout (SEB) in 4H-SiC vertical power devices at lower than half of the rated breakdown voltage. This paper investigates the SEB robustness of a 1.2kV 4H-SiC lateral RESURF MOSFET using a 3-D electrothermal device simulator (Sentaurus) with a reported heavy ion model based on high-fidelity radiation data. The maximum V_{SEB}/BV_{rate} ratio of 0.67 is 2.2 times higher than the reported V_{SEB}/BV_{rate} ratio of 0.3 for a 4H-SiC vertical DMOSFET with the same voltage rating. The reason is due to the reduced surface field at the drain terminal and the orthogonality of the heavy ion and impact ionization paths, resulting in less efficient excess carrier generation. This highlights the potential of lateral power devices for use in radiation-hardened environments.

Introduction

4H-SiC vertical power devices have long been favored in high voltage, high power applications due to the better voltage and current handling ability from the vertical architecture [1]. However, extensive experiments and simulations indicate that single-event effects (SEE) can trigger a second breakdown in 4H-SiC vertical power devices at lower than half of the avalanche breakdown voltage [2, 3]. This mode of device failure, caused by the so-called second breakdown, known as the Single-Event Burnout (SEB), is initiated by a high electric field and has been attributed to ion-induced mesoplasma formation deep within the semiconductor bulk, ultimately leading to catastrophic thermal failure (commonly known as thermal runaway) [3, 4]. Due to the fundamental differences in electric field distribution between lateral and vertical power devices, Single-Event Effects (SEEs) in lateral devices may exhibit unique characteristics. However, SEE effects in 4H-SiC lateral power devices have hardly been investigated. In this simulation-based study, we assess the SEB robustness of a 1.2kV 4H-SiC lateral RESURF power MOSFET and explore the SEEs originating from different heavy ion strike locations. We have found that the lateral RESURF MOSFET to be more robust than the vertical MOSFETs against SEB.

Target Device Modeling

The target 4H-SiC lateral power MOSFET, optimized for 1.2kV, incorporates the RESURF layer and field plate designs [5], as shown in Fig 1. It has 100 nm SiO_2 gate oxide and a 3μm lateral p-type channel connecting the source and RESURF region. An N-type RESURF region, featuring a dose of 5e12 cm^{-2} and a thickness of 0.5μm, is implemented between the channel and the drain to support the blocking voltage. The optimum RESURF dose for SiC with maximized breakdown voltage is 1e13 cm^{-2} [6]. It is decreased to 5e12 cm^{-2} to prevent gate oxide breakdown since it is limited by oxide breakdown instead of avalanching in SiC [5]. In addition, the dose of the p-type epitaxial region, which has a doping concentration of 5e15 cm^{-3} and a thickness of 10μm, must match the RESURF dose to balance the charges. The lateral diffusion length of source and drain implantation is 4μm. This gives the pitch of the device to be 31μm. The device width is set to equal to the pitch.

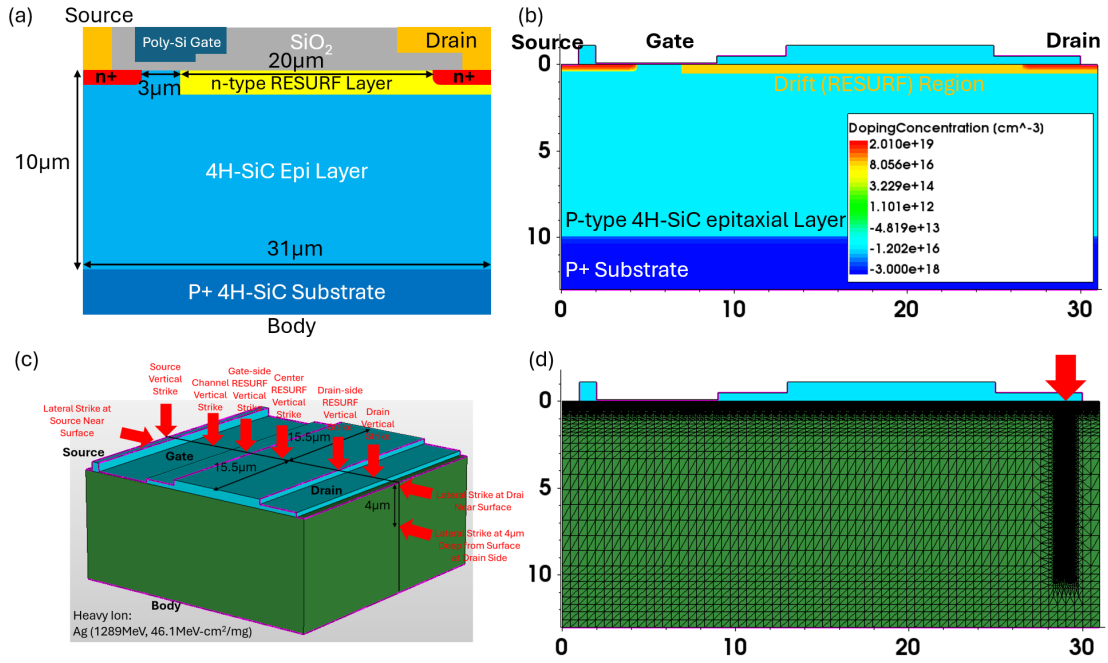

Fig. 1. (a) Structure of target 1.2kV 4H-SiC lateral RESURF MOSFET. (b) 2-D schematic cross-section of the device with doping profile. (c) Device 3-D model in Sentaurus. (d) Refined meshing for the vertical strike at drain.

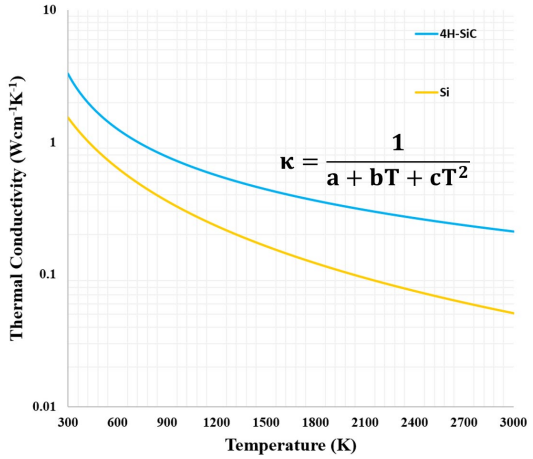

Fig. 2. Temperature dependent thermal conductivity of 4H-SiC used in simulations. Si thermal conductivity is added for reference.

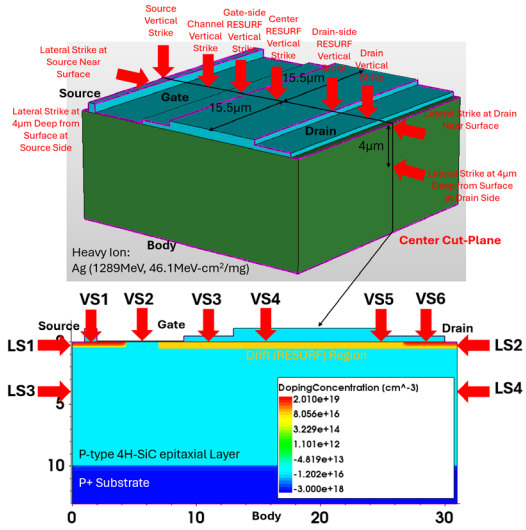

Fig. 3. Investigated vertical and lateral strike locations labeled on 3-D model and center 2D cut plane.

Modeling of Single-Event Burnout

SEB is inherently a highly localized thermal event resulting from the significant localized current generated by the ion-induced creation of electron-hole pairs as a heavy ion passes through the device. Hence, correct modeling of ion-induced electron-hole pairs spatial distribution is vital for accurate SEB simulations. The energy transfer of a single particle with sufficient energy to target the semiconductor lattice is defined as Linear Energy Transfer (LET), the amount of energy transferred per unit length of the particle path, and is a strong function of projectile energy, density, and ionization energy of the target semiconductor [7]. In the previous works [8, 9], the 4H-SiC Silver ion collision profile (Silver ion energy: 1289MeV, Linear energy transfer (LET): 46.1MeV-cm^2/mg) based on Monte Carlo approach from high fidelity radiation data has been interfaced into Sentaurus TCAD

3-D device simulator. The selection of silver ions with a LET value of 46.1MeV-cm^2/mg was explicitly intended to maintain consistency with established testing protocols for 4H-SiC power devices [10], facilitating comparative analysis. Further, prior SEB experiments [11] on 4H-SiC power devices reveal that SEB failure voltage is independent of heavy ion energy for high-energy particles with a LET value above 10 MeV-cm^2/mg.

Table 1. Important Simulation Parameters.

Parameter	Model	Value at 300K
Thermal Conductivity [13]	$\boldsymbol{\kappa(T) = \frac{1}{3.57 \cdot 10^{-3} + 3.93 \cdot 10^{-4} T + 1.86 \cdot 10^{-6} T^2}}$	3.46 Wcm^{-1}K^{-1}
Lattice Heat Capacity [14]	$\boldsymbol{C_L = 1.82 + 3.07 \cdot 10^{-3} T - 1.28 \cdot 10^{-6} T^2 + 2.16 \cdot 10^{-10} T^3}$	2.63 JK^{-1}cm^{-3}
Bandgap [15]	$\boldsymbol{E_g(T) = 3.342 - 3.3 \cdot 10^{-4} T}$	3.24 eV
Impact Ionization [16]	$\boldsymbol{\alpha_e(F) = 1.12 \cdot 10^6 \exp\left(-\frac{8.34 \cdot 10^6}{F}\right)}$	-
	$\boldsymbol{\alpha_h(F) = 2.35 \cdot 10^6 \exp\left(-\frac{8.9 \cdot 10^6}{F}\right)}$	-

Table 2. Simulated SEB threshold voltage, peak lattice temperature (@1200V), and mesoplasma location for various strike sites.

Strikes	SEB Threshold Voltage (V)	Peak Lattice Temperature (@1200V) (K)	Mesoplasma along Ion Path (Y/N)
VS1	1200	302	Y
VS2	1200	326	N
VS3	1200	347	N
VS4	1200	362	N
VS5	1200	2015	Y
VS6	700	3000	Y
	1200 (substrate floated)	1051	
LS1	800	3000	Y
LS2	800	3000	Y
	800 (substrate floated)	3000	
LS3	1200	2630	N
LS4	1200	1935	N

Due to the thermal nature of SEB failure, temperature-dependent models of important material parameters based on experimental data, extrapolated from room temperature to the decomposition temperature of SiC, which is approximately 3000K, are implemented in the simulation, summarized in Table 1. Among those parameters, thermal conductivity is the key factor of SEB failure due to the positive feedback from thermal generation and degradation of thermal conductivity [3]. Fig 2 shows the extrapolated degradation of SiC thermal conductivity up to 3000K.

Due to the 3-D nature of SEE, a 3-D electrothermal device simulation with adiabatic boundary conditions is necessary to simulate ion-induced SEB. To accurately capture the effects of heavy ions, a refined mesh along the ion path is generated (Fig 1(d)). Static blocking simulation was first performed on the target 3-D 1.2kV 4H-SiC lateral RESURF power MOSFET structure to obtain the solution of continuity equation of both electrons and holes in the off state when the drain of the device is under bias. This solution was then used as the initial boundary condition to the 3-D transient adiabatic simulation. Lattice temperature and carrier distributions during SEE were solved using the

continuity equation coupled with the temperature equation. Electrode contacts are set to 300K as the thermal boundary condition. Failure is identified when the peak local lattice temperature anywhere in the device exceeds 3000K, the decomposition temperature of 4H-SiC. SEE in device oxide is not investigated in this work.

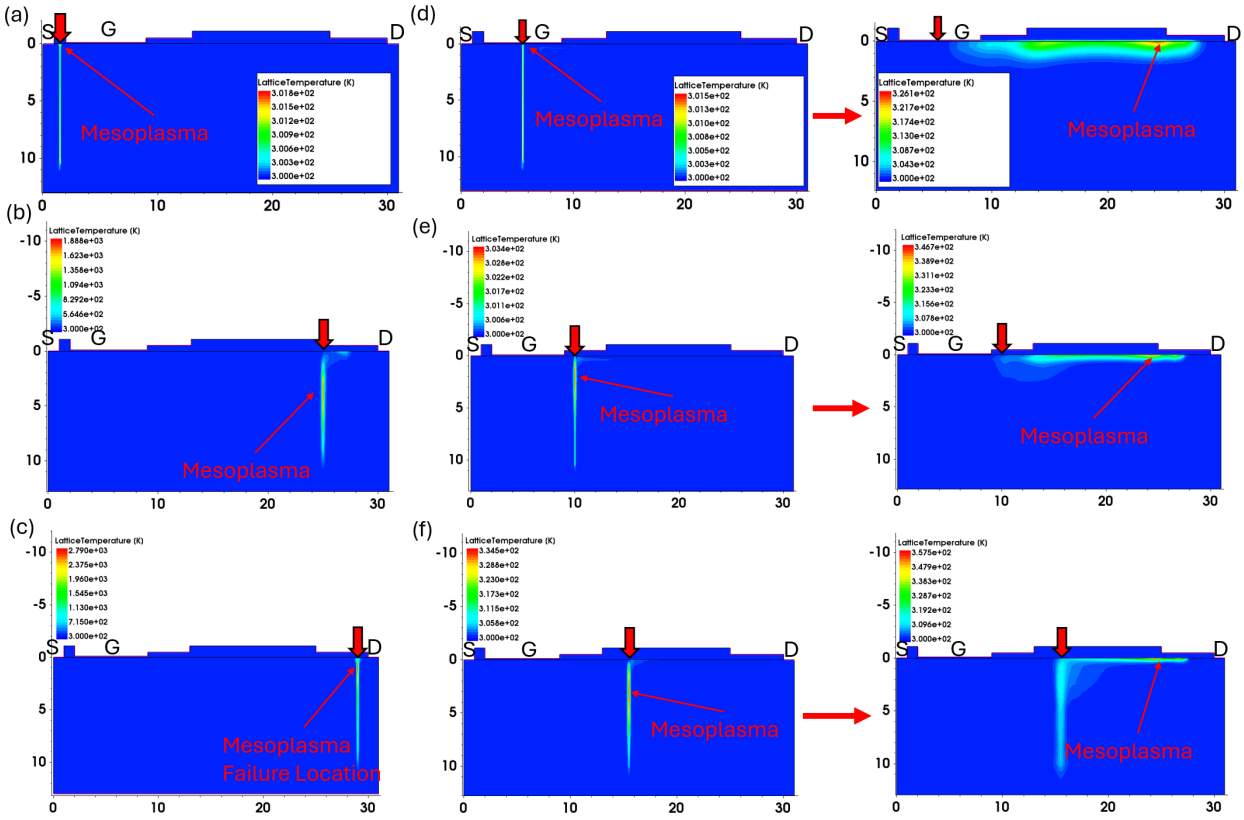

Fig. 4. 2-D lattice temperature cross-sections along ion path showing mesoplasma location at peak temperature/failure at 1200V for (a) VS1, (b) VS5, (c) VS6, (d) VS2, (e) VS3, and (f) VS4. The initial mesoplasma positions for VS2, VS3, and VS4 are also indicated in (d), (e), and (f), respectively.

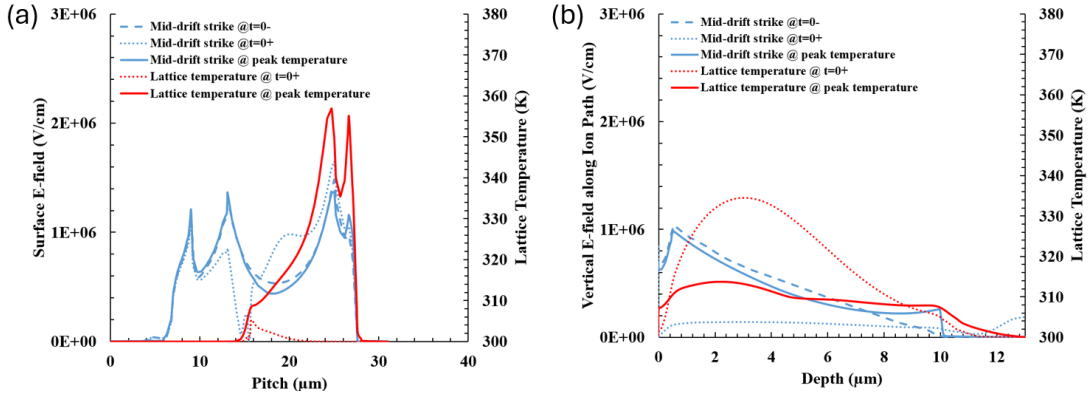

Fig. 5. Electric field (blue curves) and lattice temperature (red curves) time evolution for mid-drift region strike at 1200V (a) at the surface. (b) along the ion path.

Results

The SEB robustness of the 1.2kV 4H-SiC lateral RESURF MOSFET is comprehensively evaluated. As illustrated in Fig 3, various strike locations correspond to critical regions of the lateral MOSFET, including the source (VS1 and LS1), channel (VS2), drift region (RESURF) (VS3, VS4, and VS5), drain (VS6 and LS2), and mid epitaxial layer (LS3 and LS4).

Six vertical strikes at various sites from source to drain are studied. Table 2 summarizes the SEB threshold voltages and peak lattice temperature when the drain is biased at 1200V for the studied vertical strikes. From Table 2, the peak lattice temperature increases as the strike location approaches the drain side. SEB failure occurs during a vertical strike at the drain. The SEB threshold voltage for VS6 is about 700V (Fig 6 (a)), giving a V_{SEB}/BV_{rate} ratio of 0.58. This is almost twice the reported V_{SEB}/BV_{rate} ratio of 0.3 for the 1.2kV vertical DMOSFET [3]. In addition, as shown in Fig 4 (a)-(c), mesoplasma remains along the ion path in case VS1, VS5, and VS6, while it drifts away to 26.7μm (drift region/n+ drain well boundary) at SiC/oxide surface as the strike location is near the device terminals (Fig 4 (d)-(f)). This phenomenon is associated with lateral and vertical electric field interaction and is never seen in 4H-SiC vertical power devices.

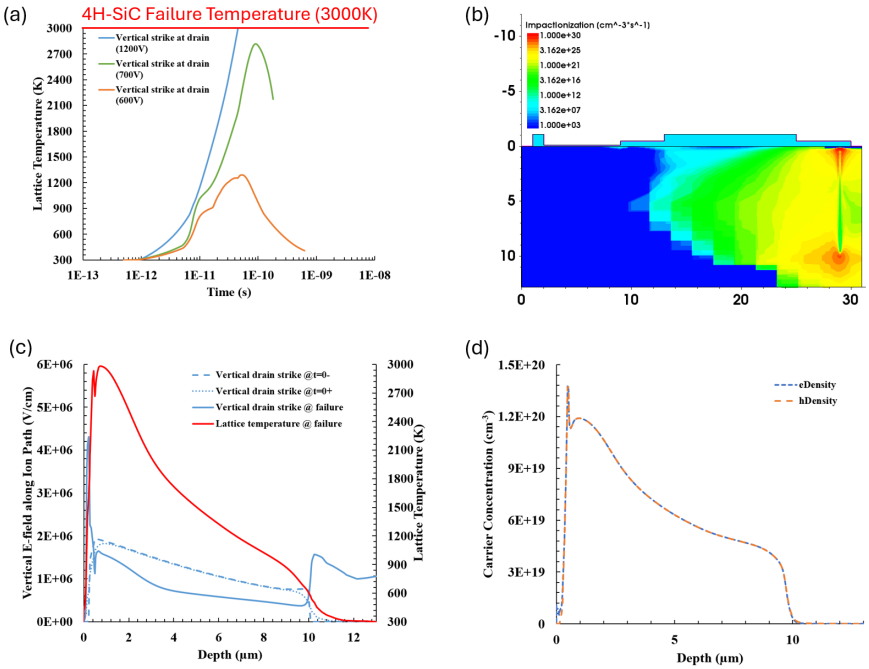

Fig. 6. (a) Peak lattice temperature transients for the vertical strike at the drain under applied drain voltages of 1200V, 700V, and 600V. (b) 2D cross-sectional view of impact ionization at the failure point. (c) Time evolution of the vertical electric field along ion path, with lattice temperature at failure overlaid. (d) Carrier concentration profiles along the ion path at failure for a vertical strike at the drain at 1200V.

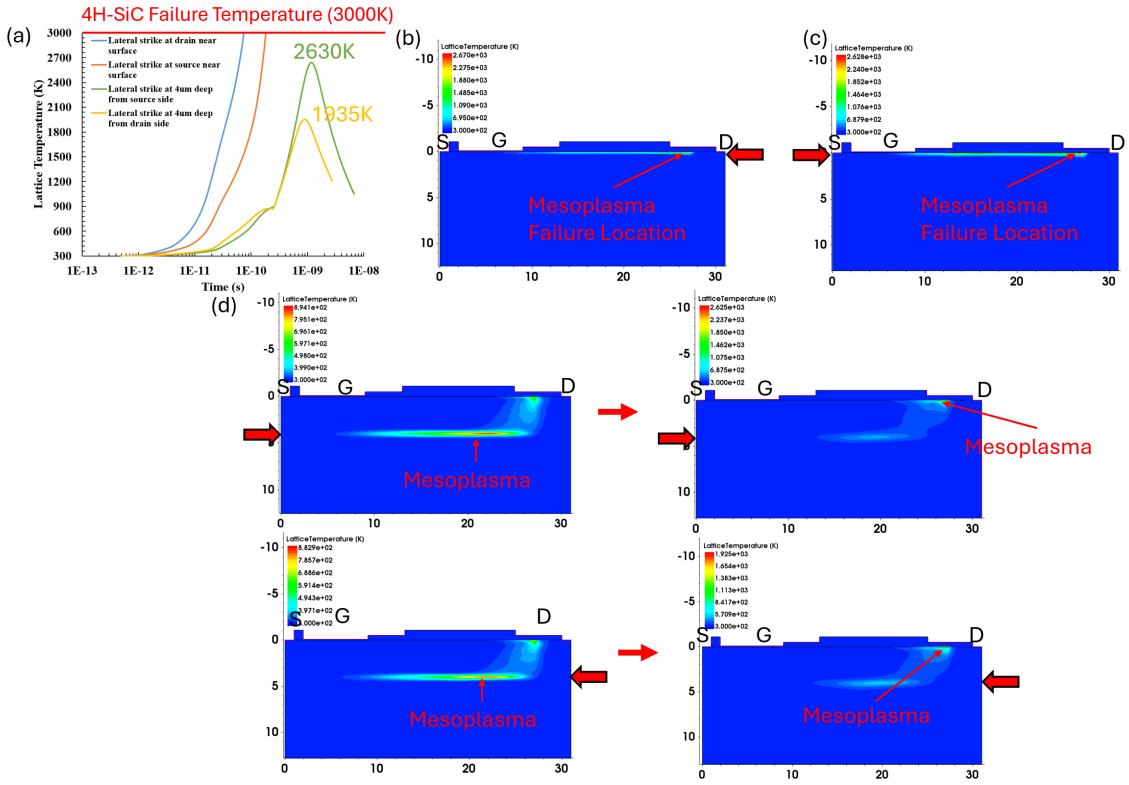

Fig. 7. (a) Peak lattice temperature transients for investigated lateral strikes at 1200V. 2-D cross-section of lattice temperature at failure for (b) LS2. (c) LS1. (d) LS3 and LS4. The initial mesoplasma positions for LS3 and LS4 are also indicated in (d).

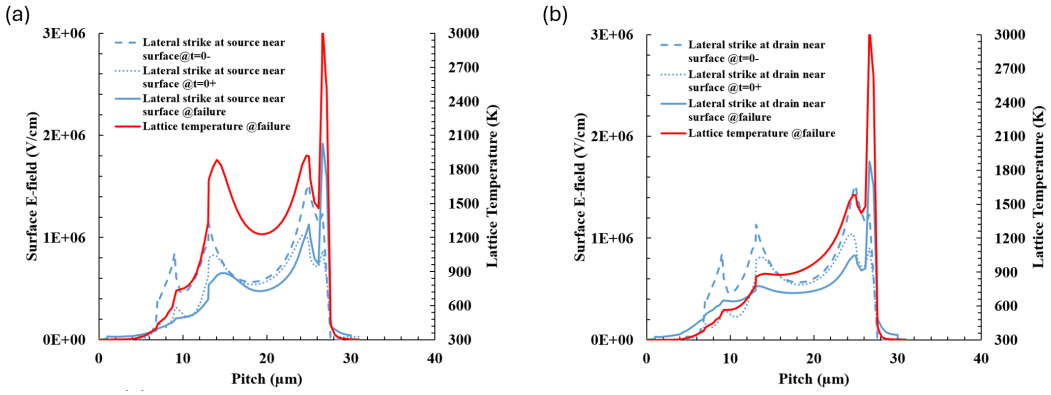

Fig. 8. Surface electric field time evolution with lattice temperature at failure overlaid for (a) LS1. (b) LS2.

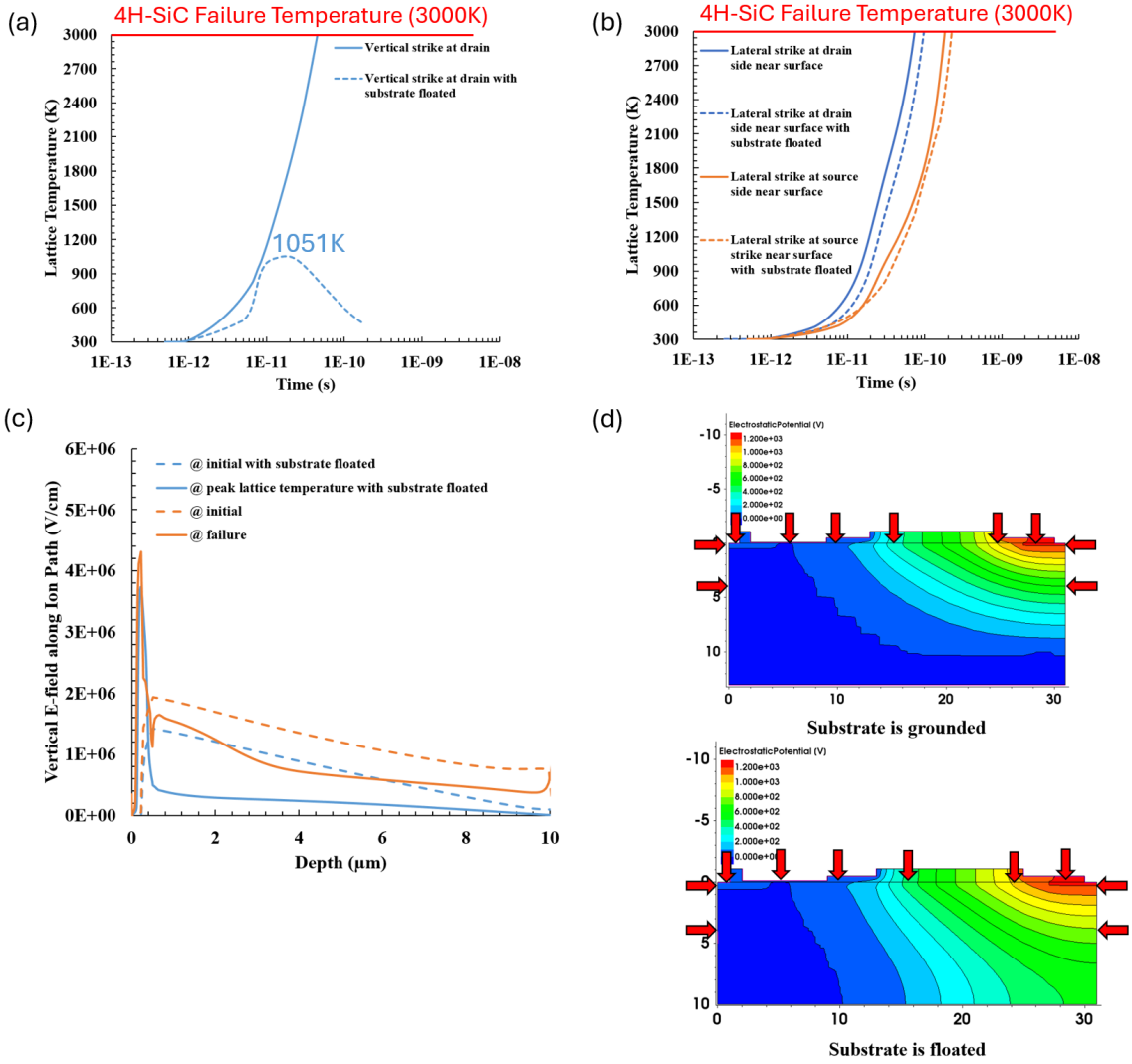

Fig. 9. Peak lattice temperature transients at 1200V for (a) vertical strike at drain (b) lateral strikes near the surface with substrate grounded or floated. (c) Electric field profile at initial and peak lattice temperature/failure along the ion path for vertical strike at drain at 1200V. (d) Electrostatic potential contours before strike at 1200V when substrate is grounded or floated. 100V for each contour.

The time evolution (Fig 5 (a) and (b)) of the surface and vertical electric field profiles along the ion path for the mid-drift region strike at 1200V is examined at three specific points in time: at t=0- (dashed blue curve), at t=0+ (dotted blue curve), and at the time of failure or peak lattice temperature is reached (solid blue curve). The surface electric field profiles (Fig 5 (a)) initially show a semi-rectangular shape instead of a triangular one due to surface field modulation from the RESURF region and field plates. Four noticeable electric field peaks from left to right are below the SiC breakdown field of 3MV/cm. These four electric field peaks, suppressed by gate and drain field plates, are associated with the high electric field regions at the gate and drain corners. On the other hand, the vertical electric field profile (Fig 5 (b)) initially shows a triangular shape with a peak location at the boundary of the n-type drift region and p-type epitaxial layer. At t=0+, a noticeable electric field dip can be seen at the strike location at 15.5µm due to the charge neutrality of generated electron-hole pairs. This leads to the collapse of the electric field in the lateral and vertical electric field profile after the strike. At t=0+, lattice temperature along the ion path (red dotted curve) peaks at 3µm from the surface where the electric field is low, indicating the mesoplasma location. As time progresses, the electric field (solid blue curve) recovers, followed by a drop in the lattice temperature (solid red curve). On the contrary, in Fig 5 (a), the surface electric field along the drift region (solid blue curve) drops, followed by an increase in surface lattice temperature (solid red curve). These suggest that

mesoplasma has shifted from the ion path towards the drain-side surface. Two lattice temperature peaks at the surface (red solid curve in Fig 5 (a)) reach peak temperature, where their locations are aligned with the surface electric field peaks at two corners of the drain field plate. This suggests the avalanche events at the drift region/n+ drain well boundary enhance the heating. Most heating at the SiC/SiO_2 interface is due to the low thermal conductivity of SiO_2. Despite the aid from the avalanche at the drain side, heating is subtle since the final mesoplasma location is far from the ion path for the vertical strike at the mid-drift region. Heating becomes significant as the strike location approaches the drain. Mesoplasma stays along the ion path under a strong vertical electric field near the drain. As illustrated in Fig 6 (c), the device fails at the bottom drain junction (0.5μm from the surface). This is attributed to the shortening of the ionization path caused by mesoplasma modulation of the electric field, leading to significant impact ionization at the junction. At failure, the carrier distribution along the ion path (Fig 6 (d)) confirms the mesoplasma location. Notably, this location aligns with the typical damage sites observed in experimental SEB results for SiC PiN diodes [12].

SEB failures occur for lateral strikes near the surface (LS1 and LS2). The SEB threshold voltage for lateral strikes near the surface is 800V, yielding an impressive V_{SEB}/BV_{rate} ratio of 0.67. This device demonstrates superior robustness to lateral strikes compared to vertical strikes (Fig 6 (c)), attributed to the reduced surface electric field (Fig 8 (a) and (b)) provided by the RESURF regions and field plates. Notably, the failure location, shown in Fig 7 (b) and (c), for both lateral strikes near the surface is at 26.7 μm (the drift region/n+ drain well boundary) on the SiC/oxide interface, which is the same peak lattice temperature position observed for the vertical strikes away from the drain (Fig 4 (d)-(f)). In addition, the device withstands both lateral strikes at a depth of 4 μm from the SiC surface under the full blocking voltage but with significant lattice heating (Fig 7(a)). Like vertical strikes away from the terminals, mesoplasma shifts away from the ion path due to a more substantial vertical electric field influence. It reaches its peak temperature at the same position on SiC/oxide interface (Fig 7(d)). Despite having significant heating at the boundary between the drift region and the n+ drain well near the SiC/oxide interface, SEB occurs in neither of the lateral strikes at a depth of 4μm under the full blocking voltage since the potential drop across the ion path is about half of 1200V. The final mesoplasma site remains distant from the ion path.

The substrate floating effect on SEB is investigated for the previously mentioned failure cases of the drain vertical strike and lateral strikes near the surface. Fig 9 (a) and (b) show the simulated peak lattice temperature transients for the studied cases. The results indicate that floating the substrate can improve vertical drain strike SEB threshold voltage to the rated 1200V but have minimal effect on the lateral strike cases. This is because floating the substrate effectively reduces the potential drop across the vertical ion path by half (Fig 9 (d)), decreasing the electric field along the ion path in the initial boundary condition (Fig 9 (c)). However, this has a minimal effect on the lateral electric field near the surface. Hence, SEB failure is limited by the lateral strikes near the surface. Substrate floating is commonly used in Silicon-on-Oxide (SOI) technology to reduce parasitic capacitances and leakage currents. 4H-SiC lateral SOI MOSFET may be viable for radiation-robust applications.

Conclusion

Unlike vertical power MOSFETs, mesoplasma formation in lateral MOSFETs is driven by comparable vertical and lateral electric fields in the drift region. Based on the investigated vertical and lateral strikes at various sites, the drain region is susceptible to ion-induced SEB. The junction boundaries at the drain are expected to be the primary SEB failure sites due to the highly localized carrier avalanche in this region. Notably, the SEB threshold voltage from vertical strikes at the drain can be enhanced to the rated voltage by floating the substrate, resulting in a maximum achievable SEB threshold voltage of 800V limited by lateral strikes near the surface for the target 1.2 kV 4H-SiC lateral RESURF MOSFET. This results in an impressive V_{SEB}/BV_{rate} ratio of 0.67—2.2 times higher than the reported 0.3 for conventional 4H-SiC vertical DMOSFETs with the same voltage rating [3]. This demonstrates superior SEB robustness compared to conventional 1.2kV 4H-SiC vertical DMOSFETs, as the RESURF region and gate/drain field plates effectively reduce the electric field along the ion path. Additionally, lateral strikes occur less frequently than vertical strikes due to

the generally larger vertical radiation capture cross-section. Consequently, the likelihood of SEB failure in lateral devices is expected to be lower than in vertical devices. These findings predict the high potential of lateral power devices for use in radiation-hardened environments. While experimental validation remains forthcoming, our future publications will present experimental results to further substantiate these findings.

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