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Investigation of Advanced Hexagonal Layouts for 650 V SiC MOSFETs

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Abstract. A set of novel features for the planar gate SiC MOSFETs with the hexagonal unit cell were investigated in terms of the $R_{DS,ON}$ and reliability (HTRB/HTGB) perspectives. The fabricated SiC MOSFETs with the proposed features improved the $R_{DS,ON}$ by 9~14% compared to the SiC MOSFETs with the conventional striped unit cell. From the $R_{DS,ON}$ temperature coefficient perspective (RT Vs. 150ºC), the SiC MOSFETs with the proposed features were close to the same counterpart with the marginal difference of ~2%. The SiC MOSFETs with the proposed features showed tighter $R_{DS,ON}$ and $I_{D,SS}$ spatial distributions in comparison to the SiC MOSFETs without the proposed features. Two batches of the SiC MOSFETs with select feature were tested for HTRB under the over-stressed conditions. One batch passed the 1,000hr HTRB test and another batch had one $I_{D,SS}$ failure at 600hr with no further failure up until 1,000hr.

Introduction

The idea of using the hexagons to layout the unit cells of discrete power MOSFETs dates to the year 1979 when International Rectifier announced its HEXFET for the first time in history [1]. The original HEXFET concept, which proved its significance to improve the trade-off relationship between $R_{DS,ON}$ and BV due primarily to the geometrical advantage of the hexagon with its highest close packing density, was implemented into the planar gate SiC MOSFETs with variations of the cell topology [2-5], where the SiC MOSFET with the hexagonal unit cell from Wolfspeed showed the significant $R_{DS,ON}$ improvement of ~ 13% compared to the conventional SiC MOSFETs whose unit cells are strip-patterned. The SiC MOSFETs that are based on the hexagonal unit cell designs, however, have a vulnerability within its JFET region which makes the SiC MOSFETs susceptible to the high drain bias. The vulnerability arises from the region where three hexagonal unit cells meet, where the JFET spacing becomes maximized, so the electric field exerted to the SiC/SiO2 interface of the region reaches its maximum. One example of such a vulnerable region is depicted in Fig. 1, where the vulnerable region is named as the *unshielded* region. Any portion of the gate oxide layer of the MOS stack formed directly on top of the unshielded region can be exposed to the high electric field when the drain terminal is biased high enough, and the gate oxide layer stressed can be ruptured causing a permanent failure in the form of the gate-to-drain short. The concern on the unshielded region can be notable when it is needed to ensure the reliable operation of the SiC MOSFETs in the long term.

The purpose of this work is to propose a protective measure for the unshielded region of the SiC MOSFETs whose unit cells are hexagon based, while minimizing the trade-off with the $R_{DS,ON}$. The proposed layout features were designed as layout elements that can be added to the existing or the POR hexagonal unit cells. The unit cells with the proposed features are compared to the conventional striped unit cell layout and to the hexagonal unit cell with the unshielded region only from the perspectives of the static performance and the long-term reliability. This work concludes with the results of 2,000+ hour-long, preliminary HTRB tests performed on the unit cell with the select feature proposed.

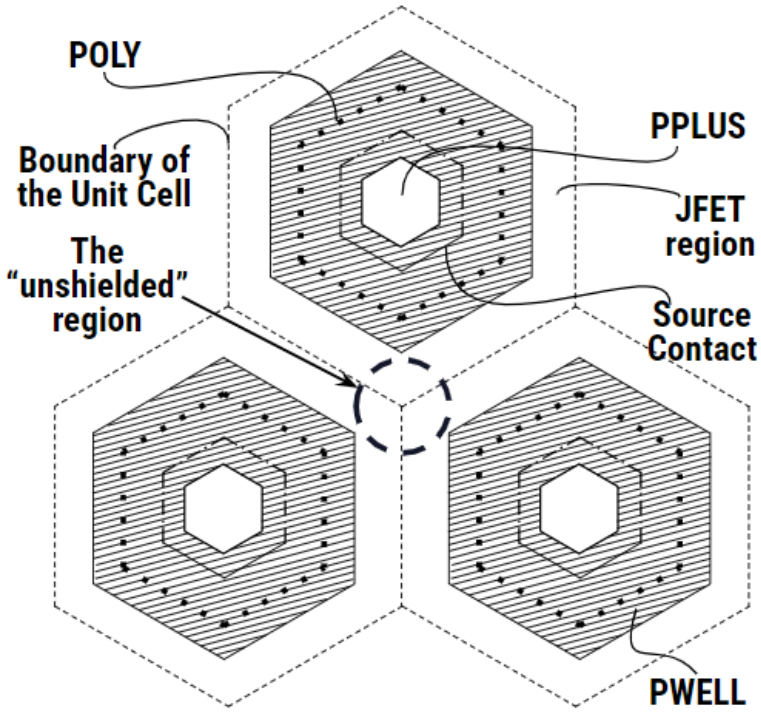


Fig. 1. Typical layout of the hexagonal unit cell with the unshielded region.

Design of the Unit Cell Layouts

Fig. 2 shows four layout variations used for this investigation. Fig. 2(a-c) show the hexagon-based unit cells, where Fig. 2(a), 2(b), and 2(c) are called Design A, Design B, and Design C, respectively. Fig. 2(d) shows a striped-based unit cell, and is named Design D. The three hexagon-based designs (Design A, Design B, and Design C) are identical from the layout perspective, except for extra layout features that are introduced in place of the unshielded region. Design A has the unshielded region without no such extra layout feature on top of the unshielded region. Unlike Design A, both Design B and Design C have new layout features that are placed in lieu of the unshielded regions. The main differences between Design B and Design C are the shapes of the p-type *Shield* region and the existence/non-existence of the p-type *Bridge* region, where the shield and bridge region are formed where the unshielded region used to exist.

Design B, as shown in Fig. 2(b), has a triangle-shaped shield region, which is connected to its three nearby PWELL hexagons via the three corners of its triangle, where the parameter "W" shown in the same figure depicts the amount of "contact" between the triangular shield and the PWELL hexagon. As the "W" increases, the area that connects the triangular shield and the PWELL hexagon become greater, and vice versa. We varied the dimension of the "W" parameter of Design B to observe the impacts of the parameter "W" on the overall static performances of the SiC MOSFETs. Varying the parameter "W" led to two sub variations of Design B family, which are Design B1 and Design B2, where the "W" of Design B1 is 43% smaller than that of Design B2 as shown in Table 1. Table 1 shows various unit cell topologies used for this study with the values of the parameter "W"s. Except for the "W" used, both Design B1 and Design B2 share the same layout designs.

Design C, shown in Fig. 2(c), has a regular-hexagon-shaped shield region being connected to three nearby PWELL hexagons via three bridge regions, where the widths of the three bridge regions (denoted as the parameter, "W" in Fig. 2(c)) are identical, being equal to the dimension of a side of the regular hexagon of the shield region. Varying the parameter "W" led to two sub variations within Design C family, which are Design C1 and Design C2, where the "W" of Design C1 is 25% less than the "W" of Design C2 by referring to Table 1. Except for the "W" used, both Design C1 and Design C2 share the same layout designs.

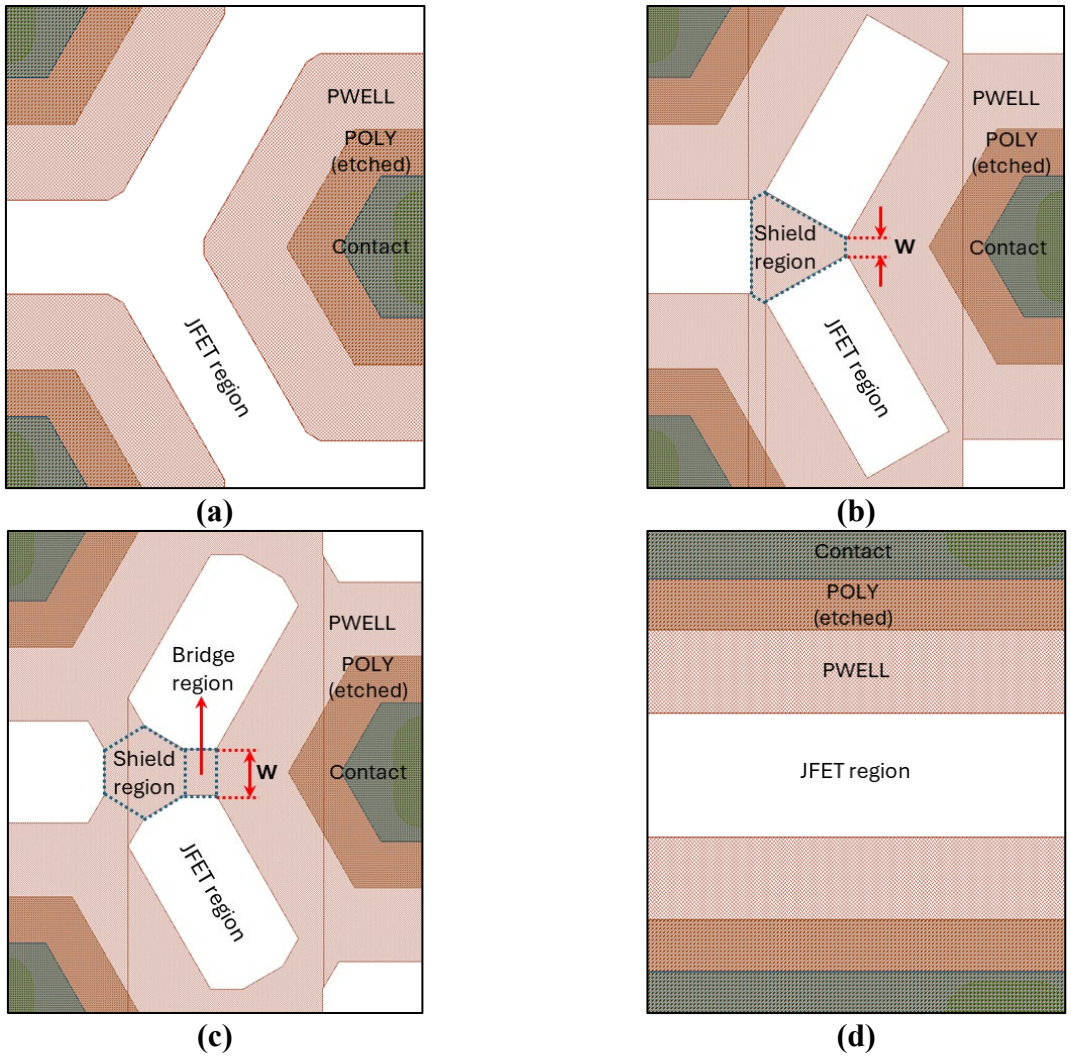


Fig. 2. Layouts of the unit cell topologies used for this investigation: (a) Design A, (b) Design B (with two sub variations of Design B1 and Design B2), (c) Design C (with two sub variations of Design C1 and Design C2), and (d) Design D.

Table 1. Parameter "W" (normalized) and Channel densities (normalized) of various unit cell topologies. All "W" values are normalized to the "W" of Design B1. All channel densities are normalized to the channel density of Design D.

Layout design	Design A	Design B1	Design B2	Design C1	Design C2	Design D
Parameter "W"	none	1.00	1.74	3.00	4.00	none
Channel density	1.33	1.96	1.89	2.28	2.19	1.00

Device Fabrication

All SiC MOSFETs of this investigation were fabricated using Navitas's proprietary GeneSiC™ "trench-assisted planar" SiC MOSFET architecture. The fabricated SiC MOSFETs were rated at 650 V and had a chip size of 3.06 mm^2. All unit cell layouts ascribed in Fig. 2(a-d), including all sub variations of Design B and Design C families, were implemented into the fabricated SiC MOSFETs.

The SiC MOSFETs fabricated with Design B2 and Design C2 were decapped/stripped off to investigate the p-type regions on the bare SiC surfaces, and the results are shown in Fig. 3. Fig. 3 shows the top-down SEM images of Design B2 and Design C2 and the mask layouts used for each design for comparison purpose. The SEM images in Fig. 3 show the shield and/or bridge regions that were perfectly aligned to their PWELL regions. The perfect alignment of the PWELL/shield/bridge regions was made possible due to the use of one single ion implantation step that formed the three

regions at the same time. As shown in the SEM images, the intricate interaction of the processing steps for PWELL and N+ source region formation with the as-drawn sub-micron bridge and shield features resulted in additional features not explicitly present in the mask layouts. For instance, the N+ source regions may also be formed within the shield/bridge regions, as observed from the SEM images in Fig. 3. Further, these N+ source regions may or may not be connected to the N+ source region within the main PWELL hexagons, which results in changes to the effective channel width of the SiC MOSFETs. Table 1 shows the channel densities of all layout design variations per unit cell to their theoretical maximum from the perspectives of the layouts.

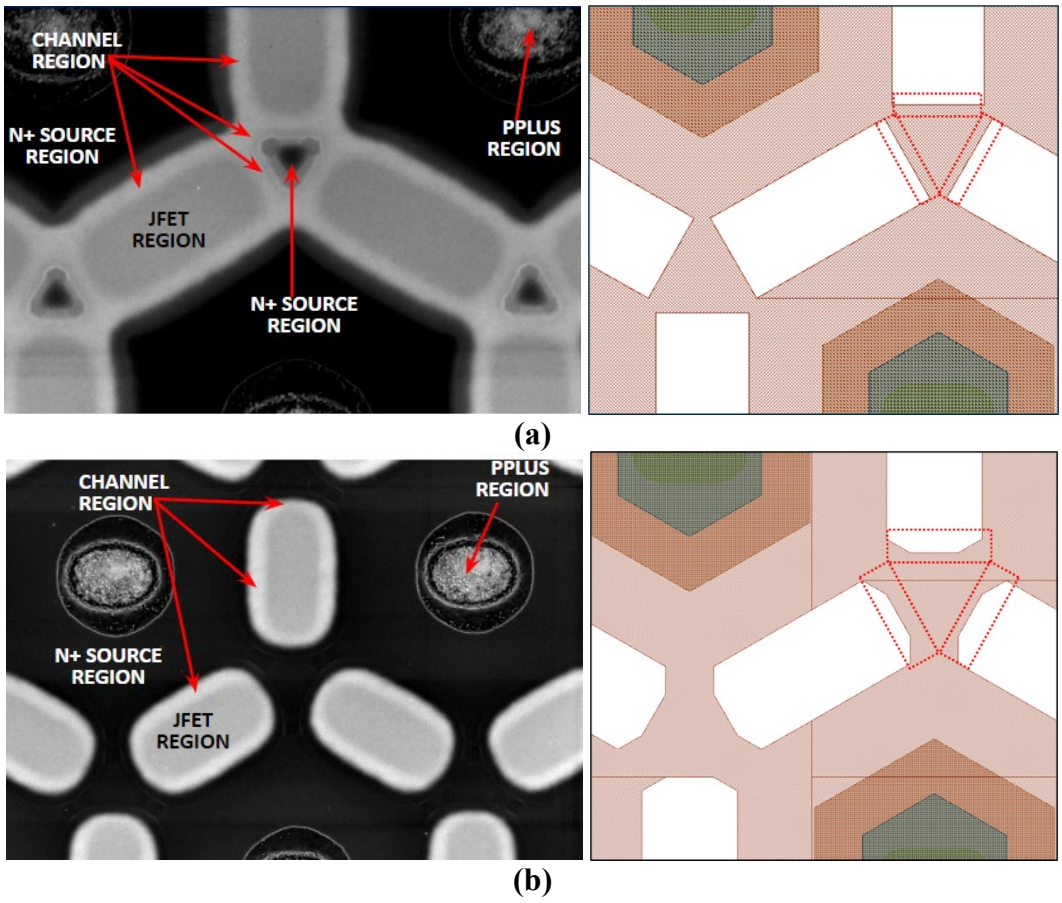


Fig. 3. The SEM images and the mask layouts of select hexagonal unit cells in (a) Design B2 and (b) Design C2. The red dotted lines shown in the mask layouts represent the channel regions formed around the corresponding shield regions.

The whole process steps to fabricate all SiC MOSFETs of this work were identical except for the split on the ion implantation schedules that formed the PWELL regions. The geometrical differences (the hexagons vs. the stripes) of the patterned PWELL hard masks substantially altered the doping profiles of the PWELL regions especially at/near the SiC surface (due mostly to the well proximity effect), which caused the difference of the V_{TH}'s of the SiC MOSFETs from the same wafer (*Wafer A*) as shown in Fig. 5. All SiC MOSFETs with the hexagonal unit cells featured with Design A, Design B's, and Design C's from *Wafer A* were ~3 V, where the SiC MOSFETs with the striped unit cell, i.e., Design D, from the same wafer (*Wafer A*) had the V_{TH}'s of ~3.3 V. The 10% difference of the V_{TH}'s from the SiC MOSFETs from Wafer A made it impossible to compare the SiC MOSFETs with the hexagonal unit cells (Design A/B's/C's) to the SiC MOSFETs with the striped unit cell (Design D). The V_{TH} difference justified the need for the wafer split at the PWELL ion implantation schedules and the new wafer (named as *Wafer B*) was made to meet the V_{TH} target of the SiC MOSFETs with Design D. The SiC MOSFETs with Design D from Wafer B showed V_{TH}'s of ~3 V as shown in Fig. 5.

Device Characterization

The SiC MOSFETs with all Design B's and Design C's featured with the shield/bridge regions showed the median $R_{DS,ON}$ values around 102~106 mΩ as shown in Fig. 4. A direct comparison of the SiC MOSFETs with Designs C1/C2 from Wafer A against the SiC MOSFETs with Design D from Wafer B, where their median V_{TH} values were close to ~3 V, showed 14% improvement of the $R_{DS,ON}$, which was due mostly to the difference of the JFET effect that originated from the difference of the hexagonal geometry of the unit cells.

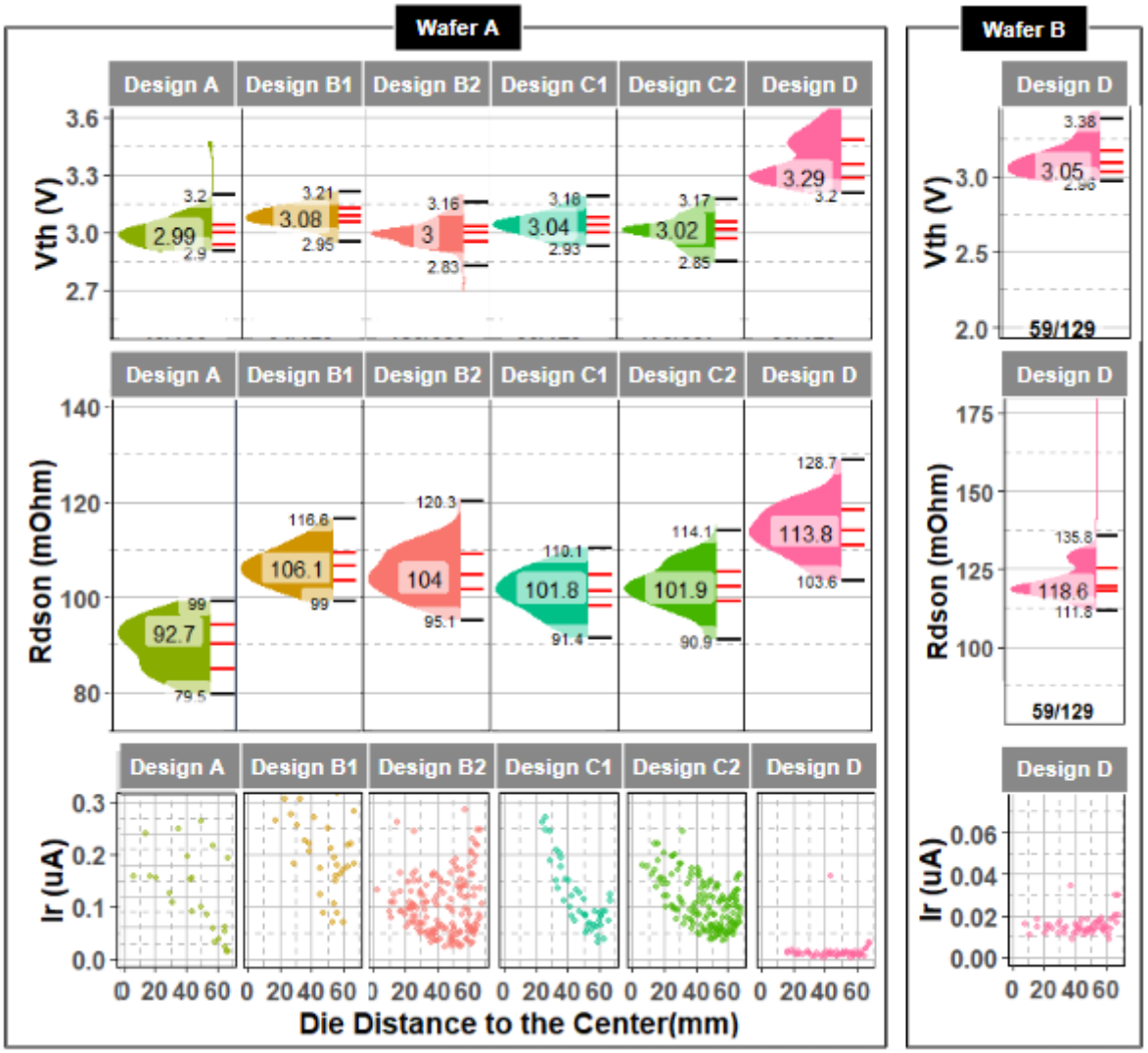


Fig. 4. Static performance of the fabricated SiC MOSFETs with all designs from all wafers.

The SiC MOSFETs with Design A featured with no shield/bridge region showed the lowest $R_{DS,ON}$ at 92.7 mΩ, which was less by 22% and by 9~13% than the $R_{DS,ON}$'s of the SiC MOSFETs with Design D from Wafer B and the $R_{DS,ON}$'s of the SiC MOSFETs with Design B1/B2/C1/C2, respectively. The significance of the $R_{DS,ON}$ differences (by the 9~13%) among the SiC MOSFETs with all hexagonal unit cell designs can be explained by the JFET effect that originated from existence/non-existence or the differences of the shapes/sizes of the shield/bridge regions.

The SiC MOSFETs with Design C1/C2 showed 2~4% lower $R_{DS,ON}$'s than the SiC MOSFETs with Design B1/B2, which was due primarily to the JFET effect mitigated.

The $I_{D,SS}$'s of all SiC MOSFETs in Fig. 4 is presented in the form of the spatial distribution of the $I_{D,SS}$ (measured at the rated voltage) across the wafers, where the left and the right ends of the horizontal axis of the plot represents the center and the edge of the wafers, respectively. The SiC MOSFETs with Design D from Wafer A and Wafer B showed the best $I_{D,SS}$ distributions across the wafers depicted as the flat lines/profiles. The SiC MOSFETs with all hexagonal unit cell designs

(Design A/B1/B2/C1/C2) showed that their $I_{D,SS}$'s varied substantially across the wafer (Wafer A). The SiC MOSFETs with Design B's and Design C's, which had the shield/bridge regions, showed considerably tighter $I_{D,SS}$'s in their spatial distributions over the SiC MOSFETs with Design A, which had no such shield/bridge region. The SiC MOSFETs with Design C's, which had the bridge regions comparing against the Design B's with no such bridge regions, showed the best performance from the $I_{D,SS}$ spatial distribution standpoint.

Fig. 5 shows the trends of the $R_{DS,ON}$'s of the SiC MOSFETs with respect to the temperature (T_C) of select designs (Design A/B2/C2/D), where the T_C was varied from the RT and 175ºC. The $R_{DS,ON}$ temperature coefficients are summarized in Table 2. The SiC MOSFETs with Design A with no shield/bridge region showed the lowest $R_{DS,ON}$ temperature co-efficient (RT Vs. 150ºC) of 1.08, which was far better (by ~8%) than the SiC MOSFETs with Design D from Wafer B, where their V_{TH} are equal to ~3V. The lowest $R_{DS,ON}$ temp-co of Design A can be explained due to the less JFET resistance than that of Design D. The SiC MOSFETs with Design B2/C2 showed the $R_{DS,ON}$ temperature coefficients (RT Vs. 150ºC) of 1.21 and 1.20, respectively, which were close to the SiC MOSFETs with Design D from Wafer B with the marginal difference of ~2%. The SiC MOSFETs with Design B2/C2 showed a similar performance compared to the SiC MOSFEETs with Design D from Wafer B from the $R_{DS,ON}$ temperature coefficient (RT Vs. 175ºC) standpoint.

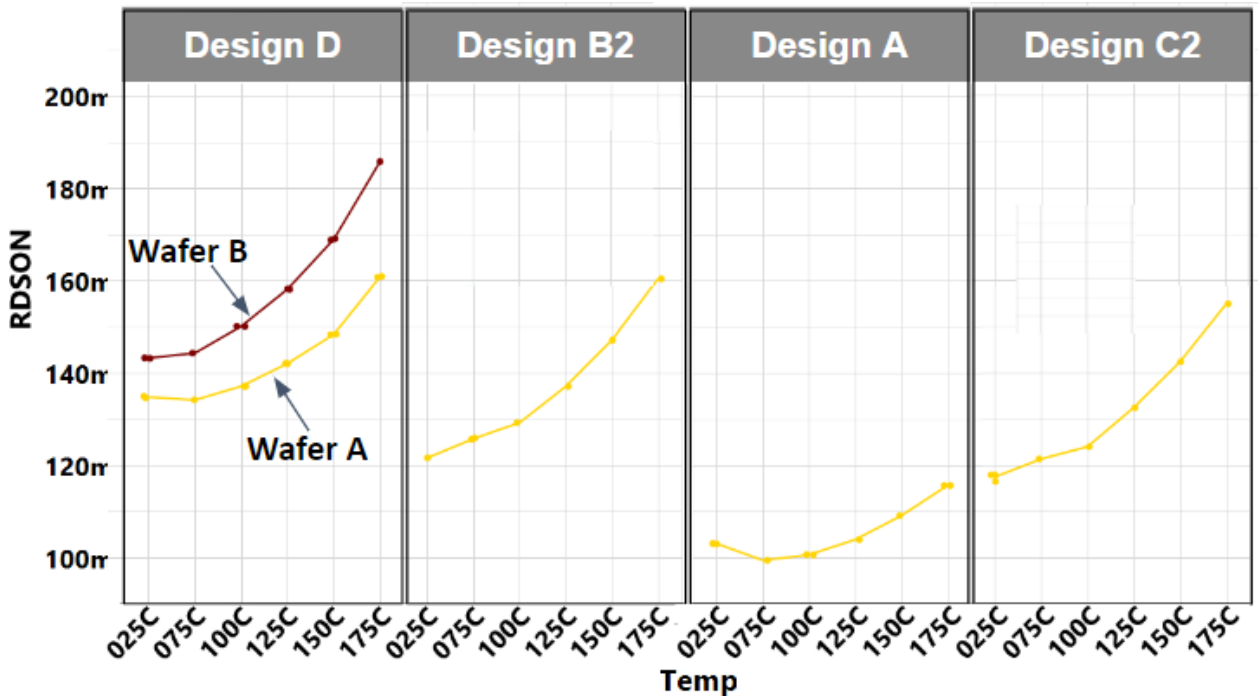


Fig. 5. $R_{DS,ON}$ vs. T_C of Design D, Design B2, Design A, and Design C2 for the consideration of the $R_{DS,ON}$ temperature co-efficient.

Table 2. $R_{DS,ON}$ temperature coefficients with different temperature ranges.

$R_{DS,ON}$ Temp Co.	Wafer	Design A	Design B2	Design C2	Design D
RT Vs. 150ºC	Wafer A	1.08	1.21	1.20	1.09
	Wafer B	-	-	-	1.18
RT Vs. 175ºC	Wafer A	1.13	1.33	1.32	1.20
	Wafer B	-	-	-	1.30

Fig. 6 shows the results of the preliminary HTGB test (up to 500hr) of the SiC MOSFETs with select designs (Design B2/C2/D). The SiC MOSFETs with Design B2/C2 featured with the shield/bridge regions showed less V_{TH} shifts and better tightness than the SiC MOSFETs with Design D in striped unit cell. The HTGB result suggests that the shield/bridge regions from Design B2/C2 provide better protection to the gate oxide layer of the MOS stacks in comparison to Design D. The Design B2 and Design C2 did not show significant differences from this preliminary HTGB test.

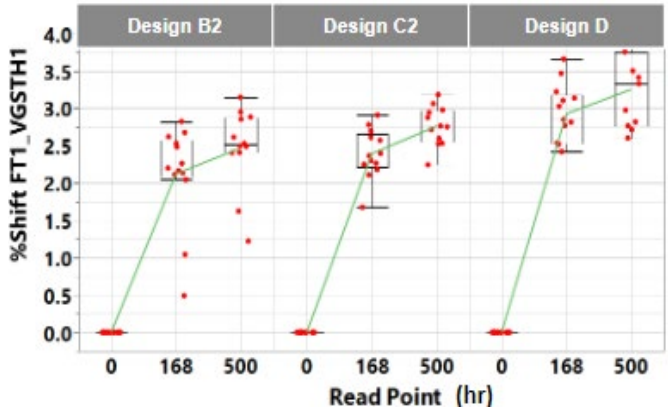
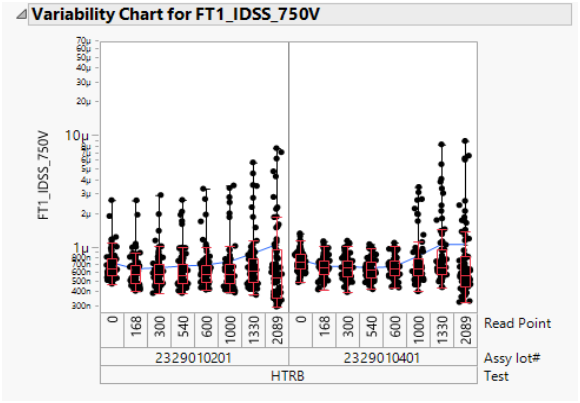
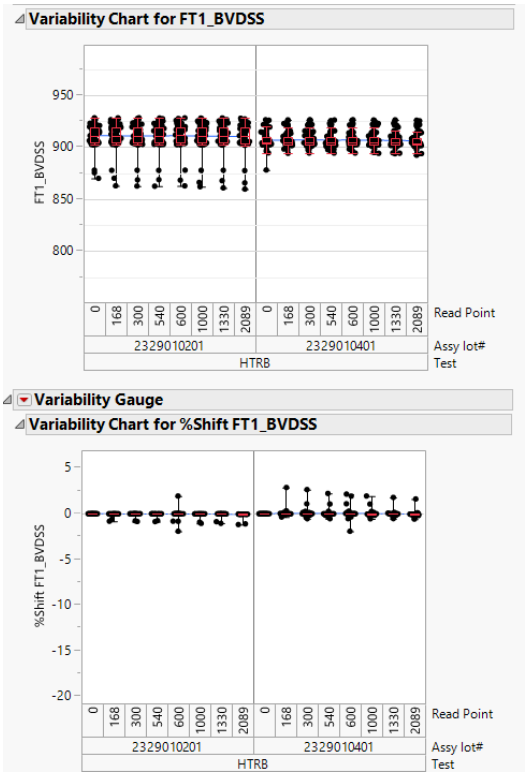


Fig. 6. The results of the 500hr HTGB tests of the SiC MOSFETs with Design B2/C2/D.

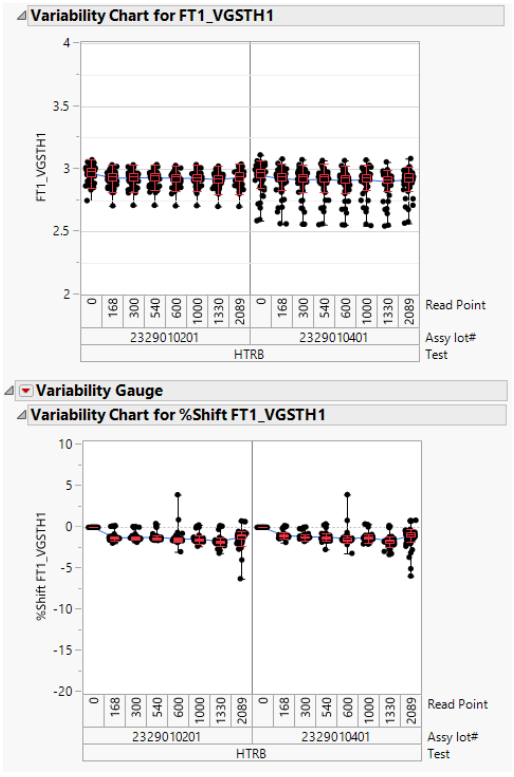
A series of preliminary reliability tests were conducted up to 2,000 hours using the 25 mm^2-sized SiC MOSFETs with the hexagonal unit cells featured with Design C2, and Fig. 7 shows the results of the HTRB tests performed at 175ºC/ 750 V (15% over-stressed from the rated BV).



(a)



(b)



(c)

Fig. 7. The results of the 2000+ hour HTRB test at 750V/ 175ºC conducted on the SiC MOSFETs with the hexagonal unit cell featured with Design C2.

Two batches (80 devices per batch) were used for the test. We observed that the first batch #2329010201 had one failed device with $I_{D,SS}$ at 600hr and there was no additional failure at 1000hrs. The second batch #2329010401) showed no failure until 1000 hours for all device parameters considered. Each batch showed two additional $I_{D,SS}$ failures at 1330hr and no further failures up until 2000 hours.

It should be noted that there is a four-sided JFET depletion effect in the shielded/bridged devices (Design B2/C2) while the stripe layout (Design D) only has a double-sided JFET depletion effect. This leads to a smaller E_{OX} at the center of the JFET region under the condition of the high drain bias, providing extra protection to the gate oxide portion of the MOS stack.

Summary

The shield and bridge regions for the hexagonal unit cells for the SiC MOSFETs were investigated from the static performance and/or reliability standpoints in comparison to the SiC MOSFETs of the same kind without the shield/bridge regions or to the SiC MOSFETs with the striped unit cell. The SiC MOSFETs with the hexagonal unit cell featured with the select shield/bridge design showed a reduction of the $R_{DS,ON}$ by 14% compared to the SiC MOSFETs with the striped unit cell, with a marginally similar performance in the $R_{DS,ON}$ temperature coefficient (RT Vs. 150ºC) by ~2%. The SiC MOSFETs with the select shield/bridge regions showed tighter spatial distributions of the $R_{DS,ON}$ and $I_{D,SS}$ in comparison to the same type of SiC MOSFETs with no shield/bridge regions. Two batches of the SiC MOSFETs with the select design were tested under the over-stressed HTRB conditions, where the first batch passed the 1,000hr HTRB test and the second batch had one failure at 600hr with no further failure until 1,000hr. The shield/bridge regions enables the four-sided JFET depletion effect within the JFET region reducing the electric field at the center of the JFET region, providing extra protection to the gate oxide of the MOS stack.

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