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A Novel Design of SiC High-Voltage Lateral PiN Diode for IC Application

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Abstract. With its excellent thermal conductivity, high critical breakdown field strength, and high temperature tolerance, Silicon Carbide (SiC) is widely used in the fabrication of power devices. In recent years, many vertical high-voltage SiC PiN diodes with superior performance have been reported. However, since the cathode-anode voltage in these devices is vertically blocked in the semiconductor, the on-chip isolation between the devices is difficult to achieve. For this reason, the vertical power device is typically employed for high power densities in single-device packages or power modules. In contrast, effective isolation between lateral high-voltage devices can be achieved by using isolation structures, which enables monolithic integration with lateral PiN diodes, transistors, and resistors to achieve control, routing, and power density regulation in smart power-integrated circuits (ICs). This work describes the design and fabrication process of a novel SiC high-voltage lateral PiN (HVLPN) diode with the addition of a lateral isolation structure with a thickness of 10 μm to achieve sufficient isolation between breakdown voltages and devices, as well as a solution for the deep etching of the SiC over 10 μm with a thick enough Hard Mask (HDM), which is required for the actual fabrication process.

Introduction

SiC devices have seen significant advancements in power applications due to their high-temperature temperature tolerance, high switching frequency, and superior efficiency to silicon-based devices [1, 2]. One of the promising areas of development is the integration of power transistors with additional control, diagnostic, and protection functions. This concept, like smart discrete silicon de- vices, enhances performance by reducing internal parasitic impedance for faster switching and offering better robustness and reliability. These advancements make SiC devices ideal for applications in aerospace, nuclear energy, oil drilling, and automotive sectors, where power management robustness is crucial [3].

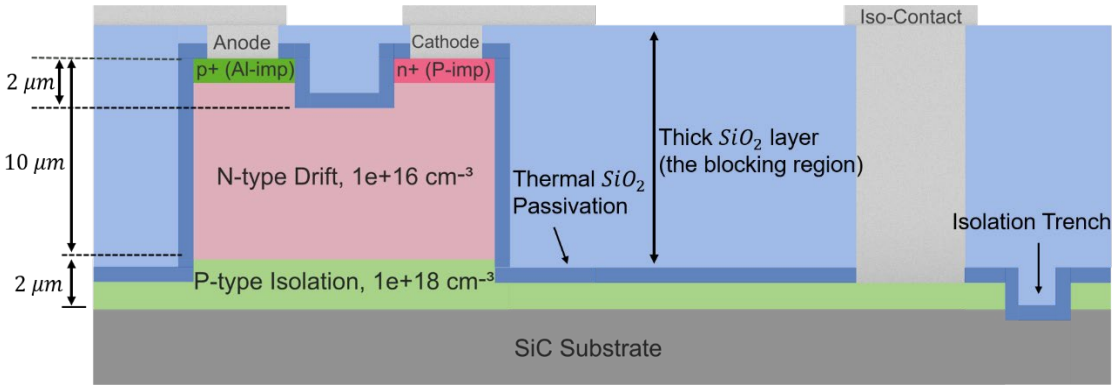
Power ICs using SiC are still in the developmental stages, but their potential is widely recognized for high-temperature operations. Several researchers have demonstrated the use of 4H-SiC bipolar technology to develop differential amplifiers, linear voltage regulators, and wide-bandgap voltage references that can operate at temperatures up to 500 °C [4–6]. Moreover, digital ICs using 4H-SiC depletion-mode JFETs have shown short-term operational capacity at up to 800 °C [7]. However, there are still challenges such as high gate leakage current at elevated temperatures. Current efforts are focused on integrating power transistors with SiC-based small-signal circuits, to improve power IC performance in high-frequency power conversion applications [8].

The monolithic integration of power transistors and ICs is a primary emphasis in SiC device manufacturing. Monolithic integration denotes the combination of various functionalities - such as driving, diagnosing, and protecting - onto a singular chip [9]. This technology is essential for developing high- performance, dependable, and resilient power devices, particularly for rigorous applications like power converters and intelligent power circuits. Researchers have established the viability of co-integrating vertical and lateral SiC Bipolar Junction Transistors (BJTs) on a single wafer utilizing conventional power BJT methodologies [10]. This methodology also possesses the considerable potential for developing analog and logic circuits for power ICs.

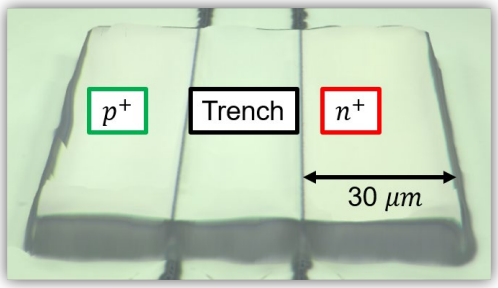
Vertical devices are favoured in high-power density applications because they can effectively block voltage in a vertical orientation, facilitating high power density in single-device packages or modules [11]. Nonetheless, these devices encounter difficulties in attaining on-chip isolation. Lateral devices provide simpler isolation structures, rendering them appropriate for monolithic integration in smart power-ICs. Although lateral devices exhibit a lower power density than vertical devices, they are advantageous for incorporating supplementary functionalities, such as control and regulation, essential for power-IC applications [12]. This research introduces an innovative design of a SiC HVLPN with a thick SiO_2 blocking layer, with the fabrication process and simulation results showing a 1000 V diode for monolithic IC applications.

Device Structure and Simulation Results

The HVLPN structure is shown in Fig. 1(a). Fig. 1(b) illustrates the 3D structure of HVLPN. Based on the simulation results shown in Fig. 2(a), the typical diode behaviour shows a forward voltage of about 2.5 V. Fig. 2(b) shows a trench with a depth to 2 µm was needed to achieve a breakdown voltage of about 1000 V. With a 2.5 µm isolation trench around the device, combined with the 10 µm deep blocking area, devices can be effectively blocked, which allows further research into the manufacture of ICs and opens up the possibility of combining power devices with logic and memory circuits. With a doping concentration of 1×10^{16} cm^{-3} in the drift layer, the blocking layers need to be 10 µm thick to achieve the breakdown voltage and sufficient isolation between devices. The simulation results of this novel structure were obtained with Sentaurus TCAD.



(a)



(b)

Fig. 1. (a) Schematic cross-sectional view of the SiC HVLPN simulated and fabricated in this work. The figure is not to scale in the x-axis. (b) The 3D microscope picture of the HVLPN, photographed by Nikon L200ND microscope after mesa etch and HDM mask removed.

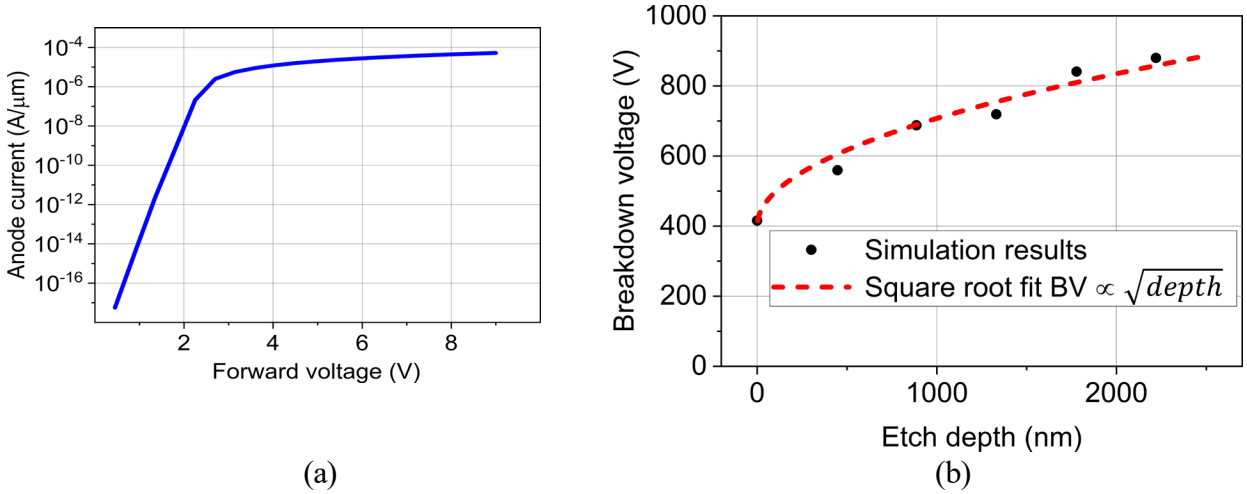


Fig. 2. (a) Forward I-V simulation results for the SiC HVLPN. (b) Breakdown voltage versus depth of trench between the anode and cathode implants. Simulation results from Sentaurus TCAD.

Fabrication Procedure

Fig. 3 shows the major processing flow. Fabrication of the physical devices was finished in KTH Electrum's cleanroom. The HVLPN can be fabricated with the same vertical power PiN fabrication process without an extra mask or processing step.

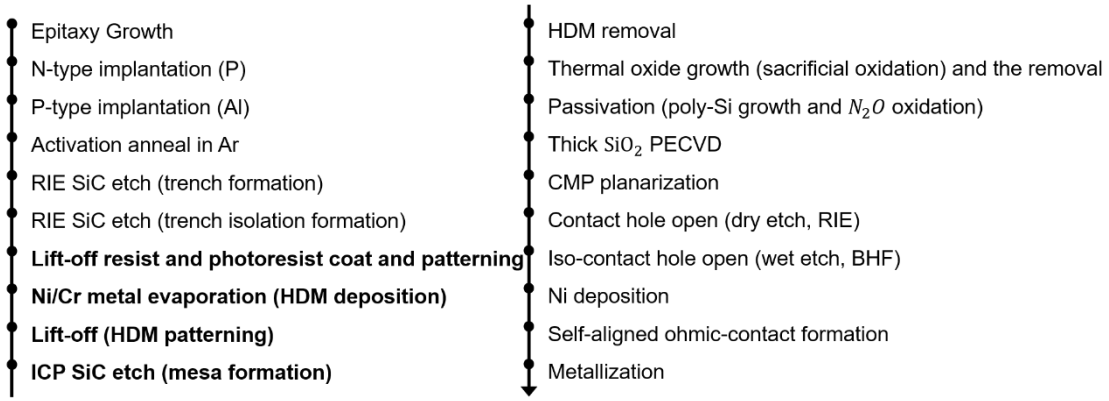


Fig. 3. Major process flow of HVLPN fabrication.

Initial 4H-SiC wafers fabricating the HVLPN device comprise 2 epitaxial layers and an N+ substrate. The N-drift layer was 15 μm thick and doped at 1×10^{16} cm^{-3}. The P-isolation layer was doped at 1×10^{18} cm^{-3}. Phosphorus and aluminium are chosen as the implantation elements to form the n+ region at the anode and the p+ region at the cathode, respectively. After that, the implanted ions were activated by annealing in Ar ambient for 15 min with a protective carbon cap.

The trench between the anode and cathode was etched by reactive ion etching (RIE) using plasma- enhanced chemical vapour deposited (PECVD) SiO_2 as HDMs. The width of the trench varies from 1 um to 30 um, and its depth was set to 1 um and 2 um for different wafers. The trench isolation structure was also etched in the same way.

To obtain 10 μm thick blocking layers, achieve 1000 V breakdown voltage and sufficient isolation between devices, deep SiC etching of more than 10 μm is required for fabrication. Surface passivation is necessary to reduce the etching surface defects and increase the quality of the SiO_2/SiC interface. The use of nickel (Ni) or chromium (Cr) as HDM materials for SiC Inductively Coupled Plasma (ICP) etching has been demonstrated to facilitate deep etching of SiC. Both Ni and Cr have been shown to exhibit high etch selectivity for SiC etching and surface integrity of the mask after etching. A lift-off technique was employed to pattern the mask to reduce micro-patterning. As shown in the processing flow diagram Fig. 4, 100-nm SiC wafers are used for this work. At first, a 1-μm layer of lift-off resist (LOR™ 5A, MicroChem™) is spun on the wafer, followed by the

coating of a 1-μm layer of photo-resist (SPR™ 700, MICROPOSIT™). The PR and LOR layers are patterned simultaneously by photo-lithography, and undercuts between these two layers are formed. Then a Cr, or heterogeneous Ti/Ni metal layer, is formed by e-beam metal evaporation with a thickness of about 400 nm. Then the wafers are soaked in 75 °C resist remover with ultrasonic washing until lift-off is finished. Eventually, the patterns are transferred to the metal HDM. SiC deep etching is performed with ICP using O_2 and SF_6. The etching selectivities were 55 and 40 for Ni and Cr masks, respectively. The ICP parameters for the SiC deep etching are shown in Table 1.

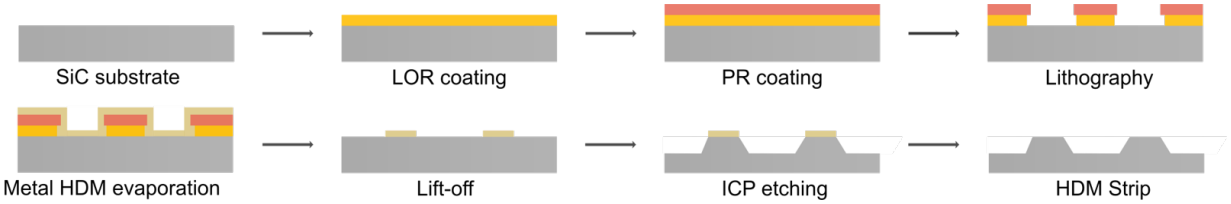


Fig. 4. Detailed processing flow of HDM patterning and SiC deep etching.

Table 1. SiC deep etching recipe.

ICP Parameters	
Pressure [mTorr]	5
SF_6 flow rate [sccm]	55
O_2 flow rate [sccm]	10
Coil power [W]	800
Platen power [W]	75

About 20 nm of thermal oxide is grown at 1150 °C in dry oxygen. Then the sacrificial oxidation was stripped by BHF. The sacrificial oxidation after ICP etching helps to reduce etch surface defects. Polysilicon was deposited on the wafer. After that, the wafers were annealed in O_2 and then N_2O. The following post-oxidation annealing in N_2O has a positive effect on the SiO_2/SiC interface.

After thick PECVD SiO_2 deposition, CMP planarization is used before the IC interconnect layers. After the CMP planarization, the contact holes on cathodes and anodes were opened with the RIE etching of SiO_2, and the contact holes on isolation structures were opened with BHF wet etching. The self-aligned ohmic contacts were formed by sputtering 20 nm of Ni on the surface and then annealing at 600 °C for 60 seconds and 900 °C for another 60 seconds. Finally, 100 nm TiW and 1 μm of Al were sputtered on the surface, patterned with lithography and then etched by using RIE to achieve metallization contact and measurement pads. Finally, the protective overglass layer was deposited with PECVD and then etched with RIE.

Experimental Results and Discussion

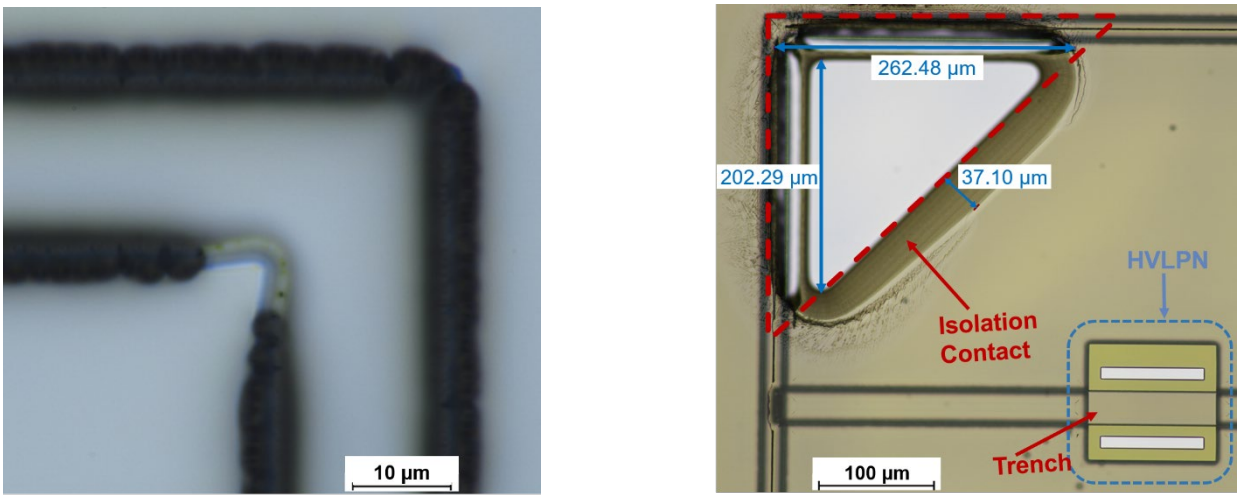
As shown in Table 2, Ni HDM shows better etching selectivity under the same etching environment. A passivation layer of Ti between Ni and SiC can help to adhere to the Ni and reduce the surface stress of the Ni layer during evaporation, thus preventing flakes from appearing on the Ni surface. Fig. 1(b) also shows the microscope image after deep etching of SiC in the mesa region.

However, upon observation (Fig. 5(a)), it was found that this ICP etching would affect the already existing structure. Some irregular micro-peaks as high as 3 to 4 μm appeared at the edge of the previously etched trench, and the reason for this phenomenon was speculated to be due to the anisotropy of the ICP etch at the edge of the trench.

Table 2. SiC deep etching results.

HDM	Ni	Cr
Mask thickness before etching [nm]	362	409
Etch time [min]	60	70
Mask thickness after etching [nm]	206	114
SiC etch depth [nm]	10855	12731
SiC etch rate [nm/min]	181	182
Mask etch rate [nm/min]	2.6	4.2
Etching selectivity	69	43

In order to evaluate the electrical blocking effect, a contact hole to the p-type isolation layer is necessary, achieved here with BHF for SiO_2 etching. Due to the isotropic etching rate characteristic of BHF wet etching, the etched isolation contact hole shows transverse expansions up to three dozen µm wide around the periphery at the longitudinal etching depth of 13 to 15 µm, as shown in Fig. 5(b). In this process, the etching rate of PECVD SiO_2 in BHF was approximately 160 nm / min. Due to the instability of BHF wet etching, other alternatives may be considered in the future, such as dry etching using the ICP technique.



(a) (b)

Fig. 5. (a) Micro-peaks formed on preexisting features after ICP etching. (b) Microscope image of the HVLPN with the isolation contact hole.

Summary

The study introduces a new SiC-based HVLPN diode aimed at improving power ICs, particularly for high-temperature and high-power applications. Using a thick SiO_2 blocking layer and SiC deep etching technique, the design can achieve a breakdown voltage of 1000 V with forward voltage per- formance suitable for future monolithic integration of power transistors. The fabrication process used conventional power PiN methods, validating the potential of this diode for reliable, high-performance power electronics, and opening avenues for combining power devices with logic and memory circuits. Simulation results further confirm the effectiveness of the proposed structure.

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