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Design and Simulation of Improved Future Generation 4H-SiC JFET-R Integrated Circuits for Prolonged 500°C Operation

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Abstract. This work compares design layouts and circuit simulations of the next two prototype NASA Glenn SiC JFET-R IC fabrication runs designated "IC Gen. 12" and "IC Gen. 13". Even though both generations employ the same physical JFET gate length and chip size, SPICE simulations predict drastic improvements to IC capabilities and performance metrics for Gen. 13 over Gen. 12. The main factors behind simulated performance differences are thinner n-channel layer leading to reduced operating voltages and switch to stepper-based photolithography that enables roughly 4-fold layout area reductions for functionally identical circuit blocks.

Introduction

NASA Glenn Research Center has previously reported the world's first and only semiconductor integrated circuits (ICs) to demonstrate stable electrical operation for over a year at 500 °C [1]. However, these initial prototype 4H-SiC Junction Field Effect Transistor-Resistor (JFET-R) chips were of limited circuit complexity (< 200 transistors per chip) and require detrimentally higher voltage, current, and power compared to functionally equivalent conventional-temperature silicon chips. Further upscaling of circuit complexity while reducing power consumption is clearly crucial towards realizing impactful infusion of SiC JFET-R ICs into extreme environment applications.

This work compares design layouts and circuit simulations of the next two planned SiC JFET-R IC prototype fabrication runs designated "IC Generation 12" and "IC Generation 13". These designs are based upon foundational mask layout and SPICE modeling guides posted online for these respective technologies [2].

JFETs & Resistors

Both Gen. 12 and Gen. 13 prototypes follow the same general fabrication flow as for earlier-generation NASA Glenn SiC JFET-R ICs [3]. However, IC Gen. 13 will employ stepper-based patterning that effectively eliminates alignment errors while enabling smaller feature sizes compared to contact mask aligner lithography layout rules employed for IC Gen. 12 design. Key technology parameters for these runs are summarized in Table 1. Both prototypes feature the same overall chip/die size of 5 mm x 5 mm and the same JFET gate length L_G of 3µm. The gate length was not reduced for IC Gen. 13 design in

Table 1. Key SiC JFET-R IC technology parameters.

Parameter	IC Gen. 12	IC Gen. 13*
Chip Dimensions	5 mm x 5 mm	5 mm x 5 mm
Resistor Width W_R	2 µm	1 µm
Gate Length L_G	3 µm	3 µm
JFET Threshold Voltage V_{T0}	-9.4V (25°C, 1 cm) -11.4V (25°C, 2 cm) -12.1V (500°C, 2 cm)	-2.89V (25°C) -3.47V (500°C)
JFET I_{DSS} for $V_S = 0$ (µA/µm)	76.8 (25 °C, 1 cm) 97.5 (25 °C, 2 cm) 35.75 (500 °C, 2 cm)	18.3 (25°C) 6.12 (500°C)

* SIMS impurity concentration profiles indicate that IC Gen. 13 threshold voltage is independent of radial wafer position.

order to manage the combined risks of epilayer variations [4,5] and short-channel effects [6] adversely impacting JFET turn-off characteristics. Once improved reproducibility and uniformity of SiC JFET epilayers is achieved in the future, smaller gate lengths will become more practical with acceptably lower risk. The width of SiC n-mesa resistors W_R was halved which enabled significantly smaller layout areas for realizing Gen. 13 integrated n-mesa resistors compared to same-value Gen. 12 resistors. Modest additional Gen. 13 resistor layout area efficiency was also facilitated by elimination of Gen. 12 resistor mesa layout shape restrictions [2].

Towards the goal of reducing JFET IC power consumption, IC Gen. 13 technical procurement specifications requested a thinner n-channel epilayer than for IC Gen. 12 [2]. The JFET electrical properties of the respective Gen. 12 and Gen. 13 prototypes calculated for zero substrate bias V_S are given in Table 1. The p^+ gate and n-channel epilayer doping and thickness profiles employed for these calculations are based upon the Secondary Ion Mass Spectroscopy (SIMS) measurements [7] (Fig. 1) conducted on selected procured Gen. 12 and Gen. 13 epiwafers [8]. Consistent with trends observed in prior JFET-R IC prototype generations [4,5], IC Gen. 12 SIMS results indicate a consequentially thicker n-channel near the wafer edge than near the wafer center. The JFET threshold voltage V_{T0} is therefore a function of device distance from the center of the wafer for IC Gen. 12, as can be seen by comparing 25 °C calculated values for 1 cm and 2 cm distance from wafer center shown in Table 1 [9]. Remarkably however, SIMS results from IC Gen. 13 epi-wafers did not resolve any difference in n-epilayer thickness between the wafer center and wafer edge. As a result, IC Gen. 13 JFET SPICE models were accordingly updated as independent of device position on the wafer [10]. The significantly smaller magnitudes for calculated V_{T0} and saturation current I_{DSS} shown in Table 1 are a direct result of significantly thinner channel of Gen. 13 compared to Gen. 12.

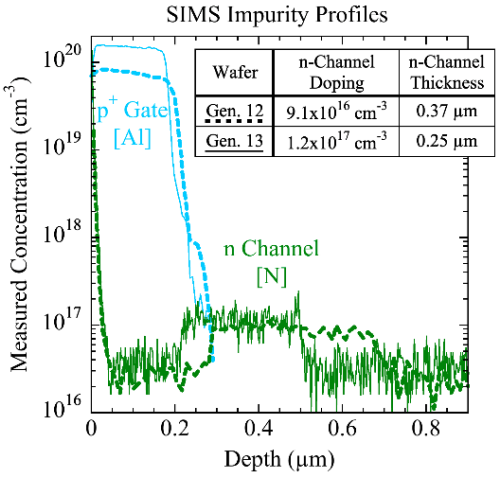

Fig. 1. SIMS-profile comparison of IC Gen. 12 (dashed) vs. IC Gen. 13 (solid) p^+ gate [Al] and n-channel [N] epilayer profiles measured near wafer center.

All SPICE simulations were conducted using NASA-posted SPICE models [2,9,10] in both LTSPICE [11] and T-SPICE [12]. It is important to note that the NASA SPICE models are first-order approximations of expected behavior (derived from combination of earlier JFET-R run results and device-physics calculations) that remain to be fully validated after Gen. 12/13 fabrication is completed. Figure 2 compares SPICE-simulated Gen. 12 and Gen. 13 JFET current vs. voltage (I-V) characteristics. Fig. 2a compares 500 °C simulated drain current I_D vs drain voltage V_D characteristics with the bulk/substrate voltage V_S = 0 V. Both devices are "depletion-mode" in that negative gate voltage V_G must be applied to turn off the transistor current flowing from source to drain. As expected, the thinner-channel Gen. 13 JFET exhibits lower I_D as well as turn-off at less-negative applied gate voltage V_G. Fig. 2b compares the SPICE-simulated I_D vs V_G turn-off characteristics at 25 °C and 500 °C for drain bias V_D = 10 V (i.e., in saturation), but with bulk/substrate bias V_S set to respective negative power supply values V_{SS} (-25V for Gen. 12, -10V for Gen. 13) employed for IC operation. The y-axis of Fig. 2b is $\sqrt{I_D/W_G}$ in order to (1) normalize current to gate width W_G, and (2) illustrate V_T as the x-intercept of the plots (since saturated $I_D \cong I_{D0}\ (1 - V_G/V_T)^2$ [13]). The non-negligible

substrate/body bias effect [4] shifts V_T to less-negative values than V_{T0} values shown in Table 1. The shift in V_T to more negative values as temperature increase is caused by reduction of pn junction built-in potential V_{bi} with temperature, which results in modest shrinkage of the depletion widths that modulate n-channel drain current conduction.

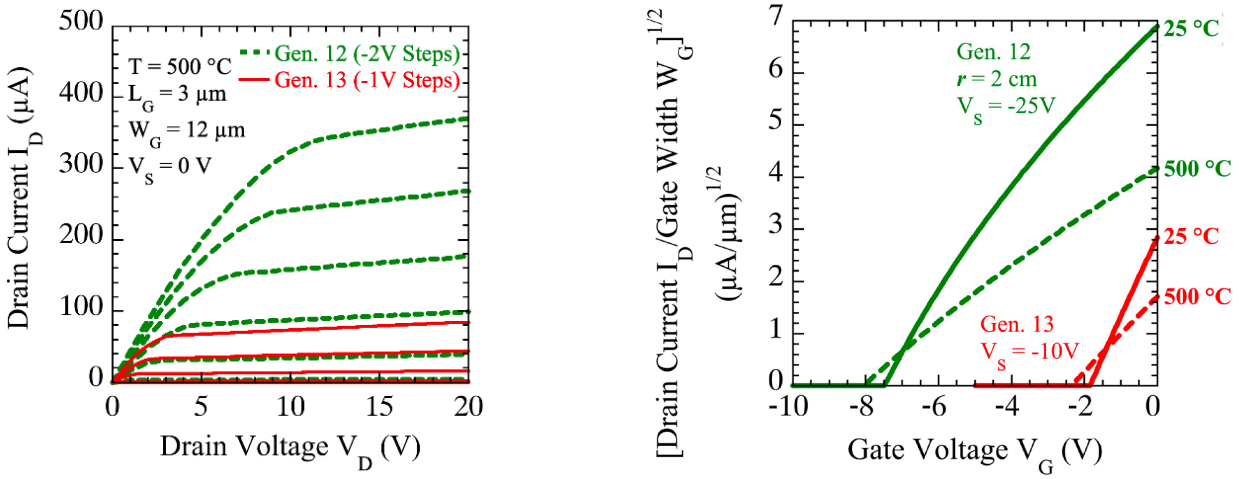

Fig. 2. Comparison of calculated 500°C IC Gen. 12 (green) vs. IC Gen. 13 (red) 4H-SiC JFET I-V characteristics. (a) 500 °C I_D vs. V_D for zero V_S substrate bias. (b) $(I_D/W_G)^{1/2}$ vs. V_G turn-off characteristics for V_S set to the technology's negative power supply value V_{SS} (-25 V for Gen. 12 and -10 V for Gen. 13).

Logic Gates

Figure 3 shows the electrical schematic diagrams of Gen. 12 and Gen. 13 "base power" NOT logic gates. The circuit diagrams are essentially identical except that IC Gen. 13 features larger resistor values (enabled by more-compact resistor layouts) and smaller power supply voltages (enabled by smaller magnitude of JFET V_T). The more than 2-fold increase in Gen. 13 resistor values reflects a design choice to substantially reduce Gen. 13 logic gate power consumption relative to Gen. 12 (even at the expense/tradeoff of increased logic propagation delay) to help thermally manage higher number/density of gates in a Gen. 13 chip. The Fig. 4 mask layout drawings of the Fig. 3 NOT circuits confirm that 3 to 4 times as many Gen. 13 logic circuits can be packed into a comparable chip area than for Gen. 12. SPICE-simulated V_{IN} vs. V_{OUT} DC transfer characteristics of these NOT logic gates at 25 °C and 500 °C are plotted in Fig. 5. Despite the large differences in quantitative transistor characteristics with temperature (Fig. 2), the logic voltage transfer curves exhibit insignificant temperature dependence consistent with prior NASA SiC JFET-R IC results [1,4,5].

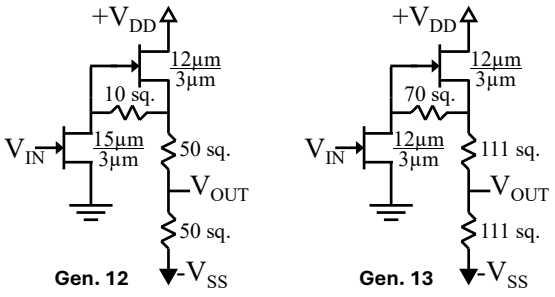

Fig. 3. NOT logic gate schematic diagrams. JFET gate width/gate length is shown along with number of squares for each SiC resistor.

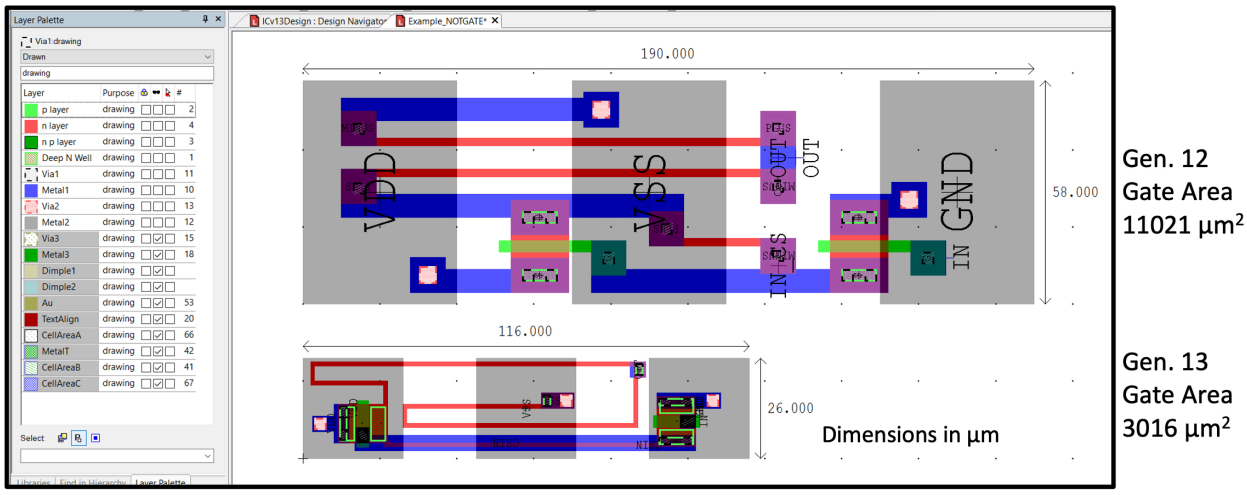

Fig. 4. Comparison of IC Gen. 12 (top) and 13 (bottom) NOT logic gate IC layouts [2]. Almost 4-fold smaller area is enabled for IC Gen. 13 via stepper-based lithography. See [2] for details.

Table 2 quantitively compares a variety of relevant performance benchmarks of the SPICE-simulated logic gates. The Gen. 13 circuit beneficially enables more than 10-fold reduction in simulated maximum power consumption compared to Gen. 12 logic gate, but at the penalty of significantly reduced operating frequency/speed.

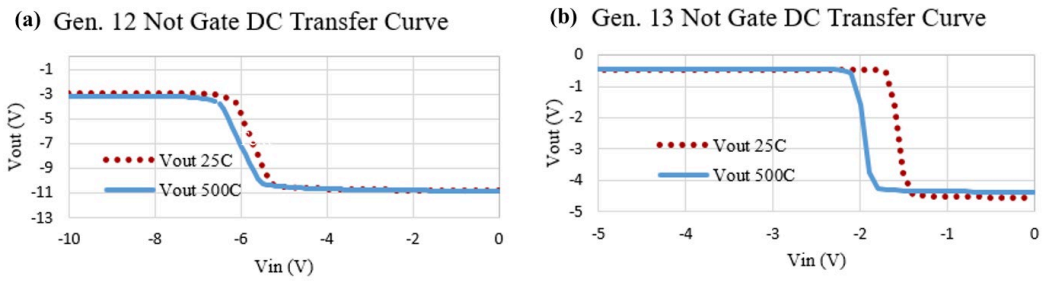

Fig. 5. Comparison of Gen. 12 and Gen. 13 Single Not Gate DC Transfer Curve at 25°C (dotted) and 500°C (solid).

Complex ICs

With the performance trends of foundational JFETs, resistors, and logic circuits established, it is useful to benchmark the resulting impact on complex integrated circuits and systems. Table 3 quantitatively compares application-relevant circuit metrics obtained for the most complex circuits that were designed for implementation in both IC Gen. 12 and IC Gen. 13. In particular, Random Access Memory (RAM, using 6-transistor memory cells [1]), Read Only Memory (ROM, using single-transistor fabrication-mask programmed memory cells), Venus lander sensor digitization and control subsystem, and simple microprocessor [14] circuits were designed for implementation.

Table 3 quantitatively compares key metrics (at application-desired high ambient temperature) for these four higher complexity Gen. 12 and 13 circuits obtained during SPICE simulations and chip layout.

Table 2. Comparison of SiC JFET-R IC basic logic gate parameters.

Parameter	IC Gen. 12	IC Gen. 13	12/13 Ratio
Layout Area	11021 μm^2	3016 μm^2	*3.65X*
Power Supply	± 25 V	± 10 V	*2.50X*
Level Shifter Resistor (MΩ)	0.229 (25°C, 2 cm) 0.880 (500°C, 2 cm)	0.430 (25°C) 1.672 (500°C)	*0.53X* *0.53X*
Output High Voltage V_{OH} (V)	-2.89 (25°C, 2 cm) -3.14 (500°C, 2 cm)	-0.46 (25°C) -0.36 (500°C)	* *
Output Low Voltage V_{OL} (V)	-10.8 (25 °C, 2 cm) -10.8 (500 °C, 2 cm)	-4.64 (25°C) -4.38 (500°C)	* *
Noise Margin Low NM_L (V)	4.5 (25 °C, 2 cm) 4.24 (500 °C, 2 cm)	2.95 (25°C) 2.37 (500°C)	*1.53X* *1.79X*
Noise Margin High NM_H (V)	2.31 (25 °C, 2 cm) 2.26 (500 °C, 2 cm)	0.93 (25°C) 1.34 (500°C)	*2.48X* *1.69X*
Maximum Power (mW)	**5.14 (25 °C, 2 cm)** **1.45 (500 °C, 2 cm)**	**0.47 (25°C)** **0.12 (500°C)**	***10.9X*** ***12.1X***
3-Stage Ring Osc. Frequency (MHz)	3.70 (25 °C, 2 cm) 0.99 (500 °C, 2 cm)	0.68 (25°C) 0.27 (500°C)	*5.4X* *3.7X*

Table 3. Comparison of complex IC Gen. 12 and IC Gen. 13 SPICE circuit simulation results.

Benchmark IC	Performance Metric	IC Gen. 12	IC Gen. 13	IC Gen. 13 Improvement
Random Access Memory (RAM)	Storage Capacity	248 (31x8) bits	1024 (128x8) bits	***4.1X***
	500 °C Chip Power	1.1 W	0.33 W	***3.3X***
	Power per bit	4.4 mW/bit	0.32 mW/bit	***14X***
Read Only Memory (ROM)	Storage Capacity	2048 (128x16) bits	5376 (256x21) bits	***2.6X***
	500 °C Chip Power	0.9 W	0.13 W	***6.9X***
	Power per bit	0.44 mW/bit	0.024 mW/bit	***18X***
Microprocessor	# of Chips Needed	2	1	***2X***
	Data Bus Width	8	16	***2X***
	500 °C Circuit Power	1.3 W	0.15 W	***8.6X***
Venus Lander Control Circuit	# of Chips Needed	5	1	***5X***
	460 °C Circuit Power	0.6 W	0.061 W	***10X***

The numerical degree/ratio of Gen. 13 metric improvement over Gen. 12 is shown in the last column. For the memory IC designs, Gen. 13 technology more than doubles single-chip data storage capacity. This is simultaneously achieved while reducing power consumption to less than 1/3rd of the power needed to operate the corresponding Gen. 12 memory chips of much smaller data storage capacity. Likewise, Table 3 shows even larger degree (> 8X) of power consumption improvement for the Gen. 13 Venus lander and microprocessor circuits compared to Gen. 12 (despite the expansion of the microprocessor's data/address bus width from 8 bits to 16 bits). The Venus lander and the microprocessor circuits were too large to fit within 5 mm x 5 mm maximum chip size using Gen. 12 layout rules. As a result, multiple chips are needed (as shown in Table 3) to implement these Gen. 12 circuits. In contrast, IC Gen. 13 enables highly advantageous monolithic single-chip implementation. Such "system on a chip" realization greatly reduces overall electronic system packaging requirements, functional cost, and other implementation barriers including technical risk. So long as other factors (such as IC robustness) are not compromised, the superior capabilities of IC Gen. 13 can be expected to pave the technical path for further maturation, manufacturing, and beneficial application infusions of 500 °C durable SiC JFET ICs.

Summary

Even though both IC Gen. 12 and IC Gen. 13 prototype designs employ the same physical JFET gate length (3 μm) and chip size (5 mm x 5 mm), SPICE simulations predict drastic improvements to IC capabilities and performance metrics for Gen. 13 over Gen. 12. The main factors behind simulated performance differences are: (1) IC Gen. 13 n-channel epilayers are both thinner and completely uniform across each wafer, and (2) the switch to stepper-based photolithography for IC Gen. 13 enables smaller layouts to be implemented for functionally identical circuit blocks. This simulation study confirms that SiC JFET-R IC Gen. 13 offers novel "system on a chip" beneficial capabilities to extreme environment applications.

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