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Optimizing Short Channel Designs in 1700 V 4H-SiC VDMOSFET

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Abstract. Shorter channel-length and thinner gate-oxide are required for the scaling of design pitch and improving device performance. We explored variations in the channel length and gate oxide thickness for 1700 V 4H-SiC based VDMOSFETs. A design of experiments was applied to cover multiple designs and process conditions. The final device results show that the shorter channel with thinner gate-oxide leads to better device performance including lower on-resistance, higher current and transconductance. However, an increase in the device leakage starts affecting the breakdown voltage thus limiting the scaling for given process conditions, such as Pwell and JFET implants.

Introduction

Higher breakdown voltage devices based on 4H-SiC enable simplified circuit designs with simultaneous increase in efficiency and reduction in the size and weight of power converters and power systems. With 1700 V 4H-SiC MOSFETs both low and high-power applications like auxiliary power supply and multi-phase inverters offer unparalleled advantages in solar, traction, solid-state transformers and EV/HEV drives. [1,2] For reliable and efficient operation at high voltages, optimization for both device design and processing are required. In this work, variations in critical device parameters like channel doping, channel length (L_{ch}) and gate oxide thickness (T_{ox}) are studied for optimizing the design for any detrimental effects including short-channel effects on the device characteristics.

Fabrication and Measurements

Figure 1(a) shows a schematic of the 1.7 kV VDMOSFET fabricated on 150 mm, N+ 4H-SiC wafers with figure 1(b) showing the picture of the fabricated wafer along with the inset highlighting a field-shot which includes multiple devices and PCM (Process Control Monitor) structures. The key device parameters including channel length and gate oxide are marked as p-well and oxide in the schematic. The variations in the device characteristics were investigated on a design of experiment batch of wafers. For this investigation, channel length was varied from 0.5 to 0.8 µm with a step-size of 0.1 µm and the gate oxide thickness was varied from 50 nm and 65 nm. The variation in the channel length was implemented by varying the cell pitch while keeping the key parameters like JFET width, N+, P+ spacing similar for different designs.

The wafers were processed as follows: for P+/JTE/Pwell and N+/JFET usual aluminum and nitrogen implants were used, respectively; implant activation through high temperature annealing; the gate oxide process involves oxide formation followed by post oxidation annealing to passivate interface and oxide traps; a nickel process was used to form the front ohmic; a power metal stack of Ti/TiW/AlCu deposition for the source and gate. While for the back contact, a laser annealing process forms an ohmic back contact before a solderable back metal stack is deposited.

For electrical characterization, Agilent B1505A power device analyzer was used for both wafer-sort and sweep measurements. The gate oxide thickness was also tracked both by inline optical and EOL (End of Line) measurements using PCM's. Other typical process control parameters like field effect mobility, gate breakdown voltages, specific contact resistance, sheet resistance for N+, P+, poly layers were also measured using dedicated structures.

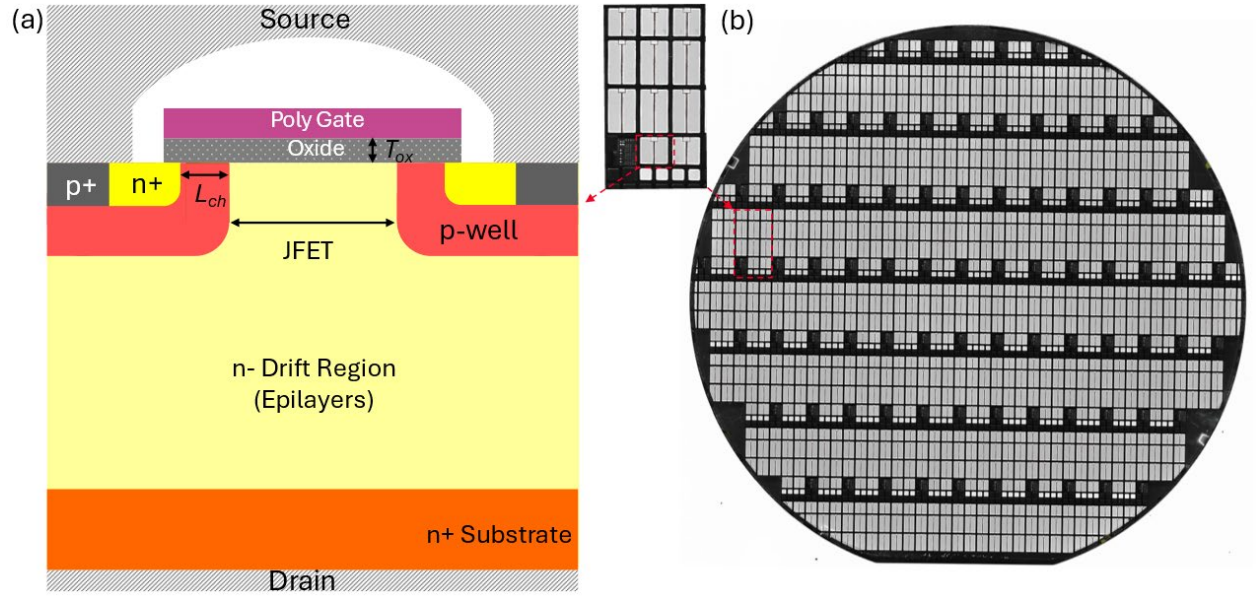

Fig. 1 (a) Cross-sectional view of the 1.7 kV VDMOSFET **(b)** image of a multi-project 150 mm processed SiC wafer with the inset showing a field-shot of the multi-designs 1.7 kV VDMOSFETs.

Results and Discussion

Figure 2(a) and (b) show variation in the threshold voltage, V_T *-mA*, defined at a fixed drain current of 7.3 mA, and body-diode forward voltage, V_{SD}, at gate-source voltage, V_{gs}, 0 V and -5 V, respectively, for different L_{ch} and T_{ox} considered in this study. With shortening of channel length, L_{ch}, from 0.8 to 0.5 µm, V_T *-mA* decreases gradually for both 50 and 65 nm gate-oxide (T_{ox}) in figure 2(a). This reduction in V_T *-mA* indicates towards the physical shortening of the channel length and/or manifestation of the short-channel effects (SCEs), which scales up for the lower L_{ch}. [3] The difference in V_{SD} at V_{gs}, 0 V and -5 V, in figure 2(b) further confirms an increase in the channel leakage as L_{ch} is scaled from 0.8 to 0.5 µm for both T_{ox} of 50 and 65 nm. Further, marginal lower values of both V_{SD} at V_{gs}, 0 V and -5 V for 65 nm compared to 50 nm for similar channel length are likely due to variation in the P+ ohmic properties. Such variations are typically linked to higher consumption of SiC for 65 nm GOX process and can be corrected by tweaking the related implant profiles. Other studies related to channel length scaling reports manifestation of similar SCEs in the range varying from 0.9 to 2.7 µm, with critical channel-length depending on other device specs including Pwell doping and thickness of gate oxide. [3-8]

Though such channel current leakage at shorter channel can be optimized by increasing the associated Pwell doping, this is at the cost of higher on-resistance due to a decrease in the channel carrier mobility because of an increase in the coulomb scattering due to the heavier implant-dose. Therefore, a judicious optimization is required for such trade-off, depending on the end application and user requirements.

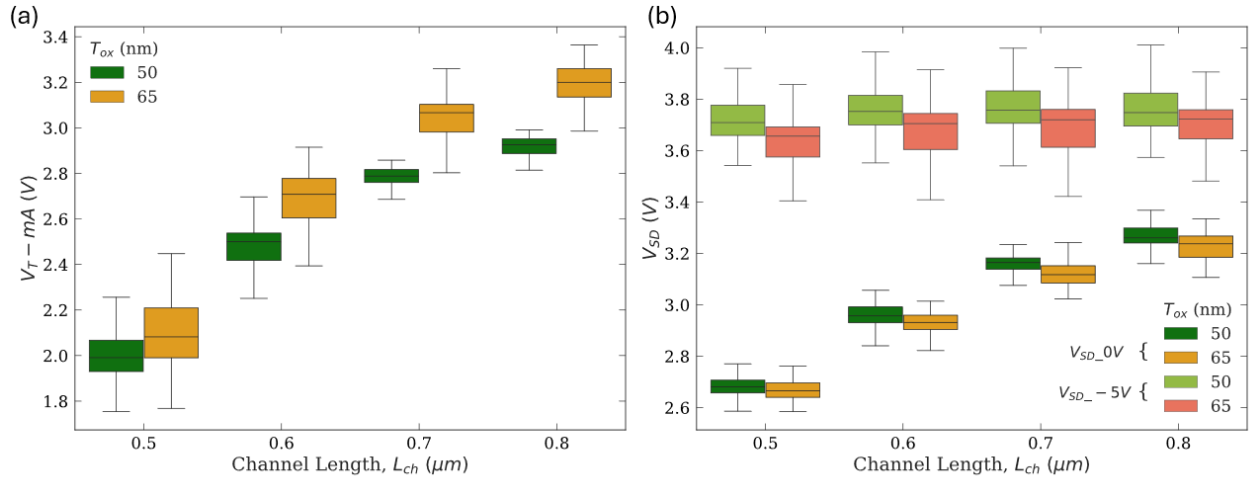

Fig. 2. (a) Box plot of threshold voltages measured at a fixed drain current of 7.3 mA, V_T*-mA* and **(b)** body-diode forward voltage, V_{SD}, for variations in the channel length and gate oxide of 0.5, 0.6, 0.7, and 0.8 µm and 50 nm, 65 nm, respectively.

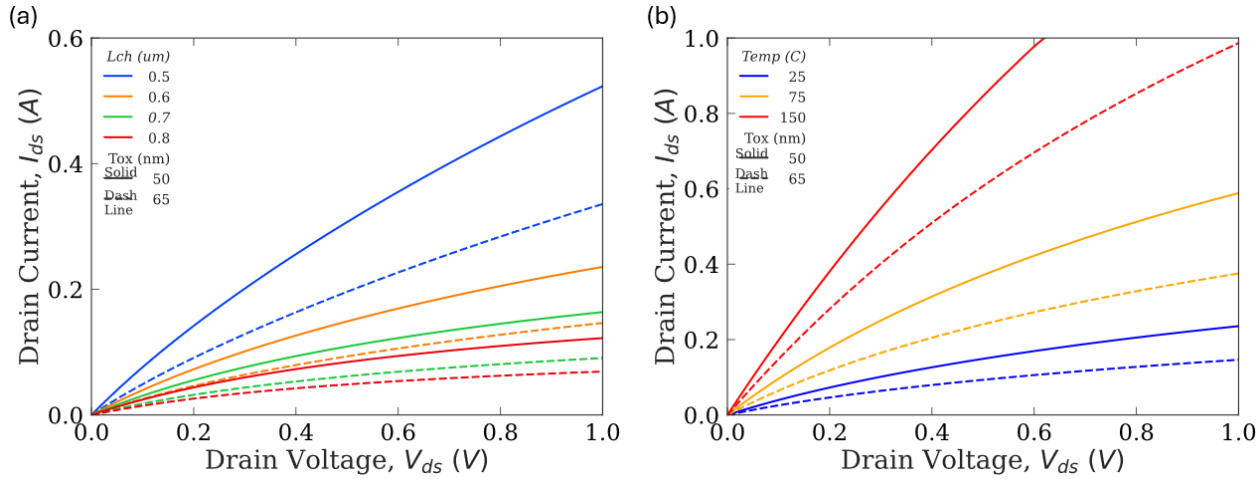

Fig. 3. (a) Output characteristics of different L_{ch} devices **(b)** plots output curves for L_{ch} = 0.6 µm device at different temperature, for both 50 and 65 nm gate oxide thickness.

Figure 3(a) plots the output characteristics at gate voltage of 5 V, shows the advantage of shorter channel and thinner gate-oxide leading to higher current or lower on-resistance. Figure. 3(b) show output curves measured at different temperatures of 25, 75 and 150°C. The increase in the drain current with temperature shows typical positive temperature coefficient at lower gate voltages due to higher carrier concentration in the channel overpowering current lowering due to mobility degradation. At higher gate voltages, drain current with temperature shows negative temperature coefficient as phonon scattering induced decrement in carrier mobility overcomes any corresponding increase in the drain current due to lowering of threshold voltage or increase in carrier concentration. Several other factors like bandgap narrowing at higher temperature and lowering of threshold voltage due to complex dynamics at the gate-oxide-SiC interface also play a key role in determining the current variation with temperature. [9,10]

Figure 4(a) and (b) plot the transfer and transconductance (g_m) curves for various combination of L_{ch}, and T_{ox}. The channel-length scaling from 0.8 to 0.5 µm for 50 nm gate-oxide show increase in both drain current and transconductance in figure. 4(a) while the advantage of thinner T_{ox} is evident in figure. 4(b) for both 0.5 and 0.8 µm channel-length. Again, the left shift in both the drain current and transconductance curves agrees with the SCE (Short Channel Effect) theory, decreasing the threshold voltages, but still not by enough to reduce the peak transconductance values. [11,12]

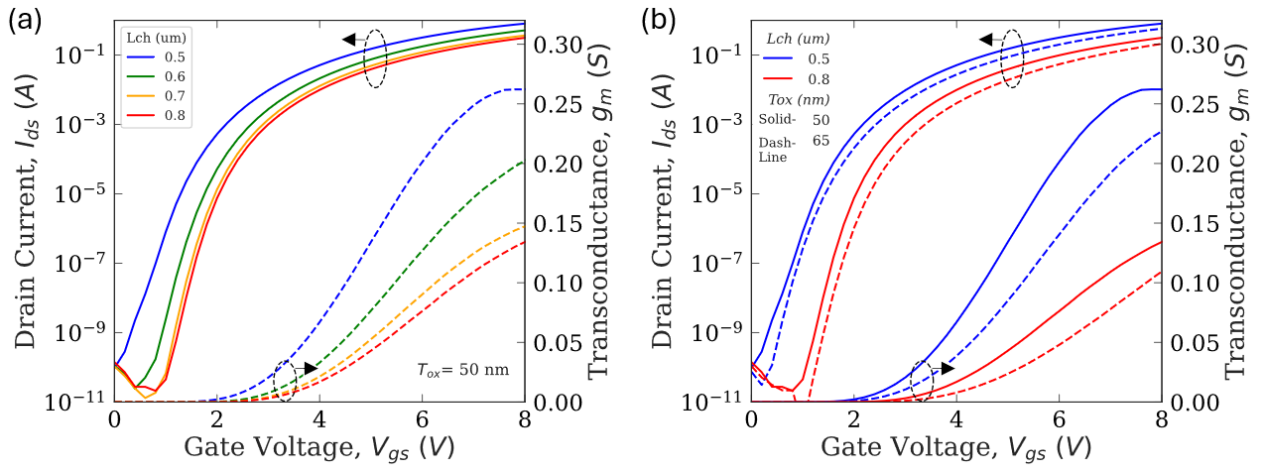

Fig. 4. (a) Transfer characteristics of T_{ox} = 50 nm devices for different L_{ch}, the secondary y-axis plots the corresponding transconductance curves **(b)** Comparison of transfer characteristics of L_{ch} = 0.5 and 0.8 µm devices for 50 and 65 nm gate oxide thickness, the secondary y-axis plots the corresponding transconductance curves.

Figure. 5(a) show variations in the drain current and transconductance with temperature ranging from 25 to 150°C. A similar increase in the drain current as seen in the output characteristics in figure. 3(b) can be seen in these transfer characteristics where the gate-oxide-SiC interface is the dominant criteria leading to this decrease in the threshold voltage and increase in the drain current. Variations in the threshold voltage plotted in figure 5(b) are based on the five-point sweep measurements carried out on wafers representing gate-oxide splits of 50 and 65 nm, while the data plotted in Figure 2 and Figure 6 is from spot-test measurements carried out at wafer level covering all devices, using an IP tester and automatic probe set-up. [13]

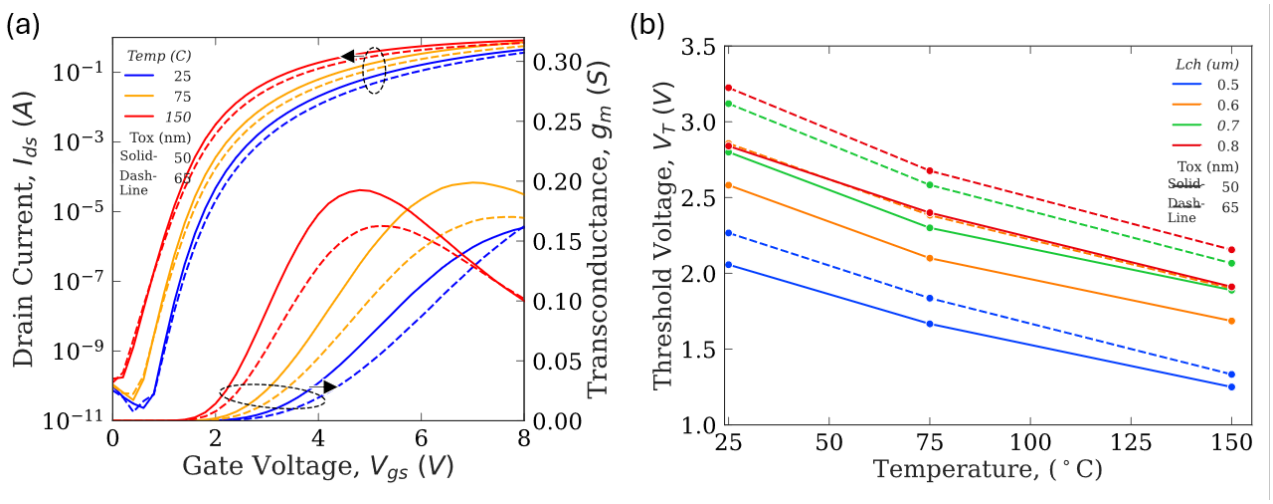

Fig. 5. (a) Transfer characteristics of 0.6 µm devices for both T_{ox} = 50 and 65 nm at different temperatures, the secondary y-axis plots the corresponding transconductance curves **(b)** Variation in the threshold voltage with temperature ranging from 25 to 150 °C for various L_{ch} and T_{ox}.

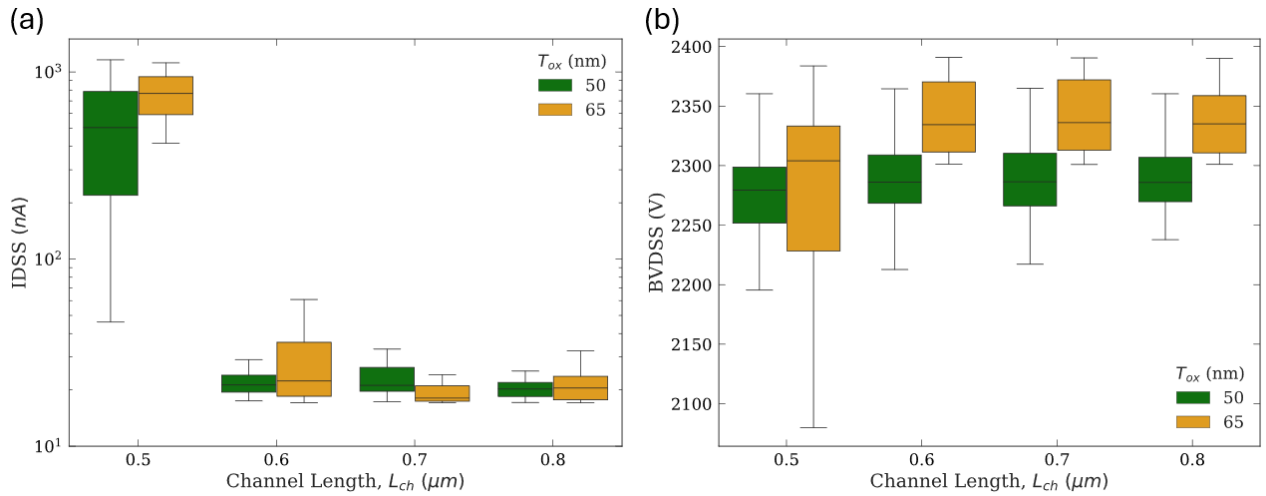

Fig. 6. (a) Device leakage current (IDSS) measured at 1700 V plotted in base Log_{10} scale and **(b)** Breakdown voltage (BVDSS) for different L_{ch} and T_{ox} devices.

Figure 6(a) and (b) show variations in the device leakage current (IDSS) and breakdown voltages (BVDSS), respectively. The consequence of a higher leakage current in 0.5 µm devices results in the lowering of BVDSS, measured at 100 µA of leakage current, signifying the critical role of channel length in optimizing the device characteristics. It may be noted that the larger statistical variations for 65 nm process as seen in figures 2(a), 6(a), and 6(b) are more likely to be linked to the underlying wafer quality rather than any process variations. For the current process and implant parameters, the longer channel ≥ 0.6 µm appears to be more robust and not affected by the short-channel effects while the 0.5 µm channel length appears to be at the edge of usefulness when considering the high-voltage characteristics. Further, other device characteristics like on-resistance showed typical variations with L_{ch} and T_{ox}, while the gate-leakage current (IGSS) did not show any significant variation in 50 and 65 nm devices offering scope of further optimization.

Summary

This design-of-experiments demonstrates the advantages of thinner gate-oxide and shorter channel length are limited by the device characteristics like IDSS and BVDSS for a given process environment. The results indicate that with appropriate implant adjustments for shorter channel and thinner gate-oxide could provide further device improvement while maintaining aggressive device pitch. However, any such improvements will be ultimately limited by the device leakage current, gate leakage current and related reliability issues, thus defining the lower and upper limits for scaling L_{ch} and T_{ox} respectively.

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