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Fast High Current Sensing SMD Resistor Network Layout for Low Inductance Insertion

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Abstract. This work presents simple layout configurations for current sensing resistor networks to measure fast and high currents in SiC devices. The proposed layout reduces the inserted inductance in the switching loop when compared to coaxial shunts, which is key for the application of SiC devices in space. High inductance in the switching loop leads to dangerous overshoots during turn-off transients, that can block the adoption of SiC devices in space due to single event burnouts. After presenting the different proposed layouts, the inserted inductance of each one is measured with an impedance analyzer as well as performing switching tests. Applying field cancellation techniques in the layout of a simple parallel resistor network, the inserted inductance is reduced up to 17.6 % when compared to a coaxial shunt, while obtaining the same current sensing performance.

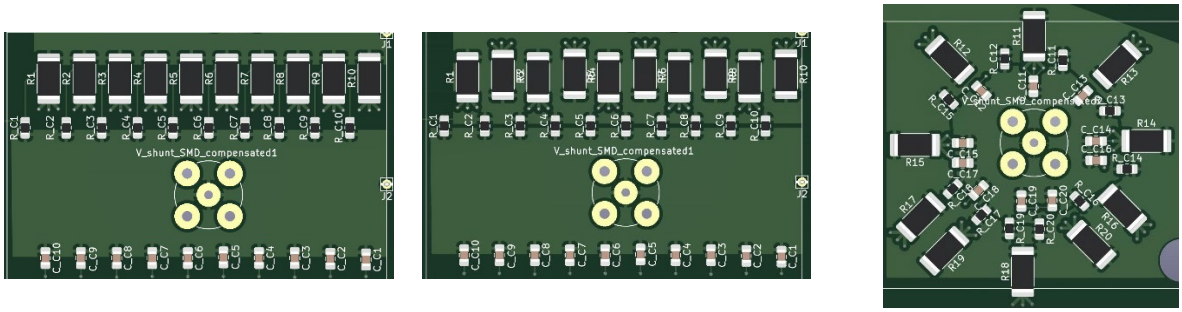
Introduction

The new space missions in the main space agencies will require high-power (HP) electronic systems [1], [2]. Following the trend in terrestrial HP electronics, space power industry is also looking to use SiC devices to achieve the required technical figures in such HP applications. However, SiC devices suffer severely from single event effects (SEE) in space applications, and need to derate their voltage considerably [3], [4], [5]. This is why controlling the voltage overshoot created by the layout stray inductance is key for the safe operation of SiC devices in space. All these makes the insertion of current measuring systems in space power converters very challenging with SiC.

SiC devices such as SiC MOSFETs have the unique characteristic of managing several tens or even hundreds of Amps at high switching speed and are required to do so in HP applications. This creates hard to measure high current derivatives, di/dt, in the switching loop of power electronic circuits. The current measurement in such systems should be high-current, high bandwidth and low inductance, to properly measure the current without creating dangerous overshoots in the switching transients. The preferred devices to measure fast currents on the range of several tens of Amps are the coaxial shunts, but they are expensive and bulky, inserting a considerable inductance, several nH, in the switching loop [6]. Surface mounted device (SMD) resistor networks are used in low current systems with excellent time response and minimum added inductance, achieving better performance than the coaxial shunts [6]. This is challenging in high currents, because bigger SMD footprints must be used, paralleling several resistors to meet the current rating, thus creating wider layouts with higher added inductance. Compensation networks can be used to improve the dynamic performance of parallel SMD networks [7], but the layout remains the most important factor, and has not been analyzed in such systems. This work compares the added inductance and the switching performance of three different layouts with the one of a coaxial shunt experimentally in a 30 A converter.

Proposed Layouts

Parallel SMD. The first configuration is the simplest one, shown in Fig. 1(a), based on 10 SMD resistors placed in parallel. The objective is to divide the current between the 10 resistors, so their footprint can be smaller thus with lower self-inductance. In addition, paralleling the resistors divides the total network inductance.



(a) (b) (c)

Fig. 1. Proposed and tested layouts, (a) parallel SMD, (b) field cancellation and (c) radial configurations.

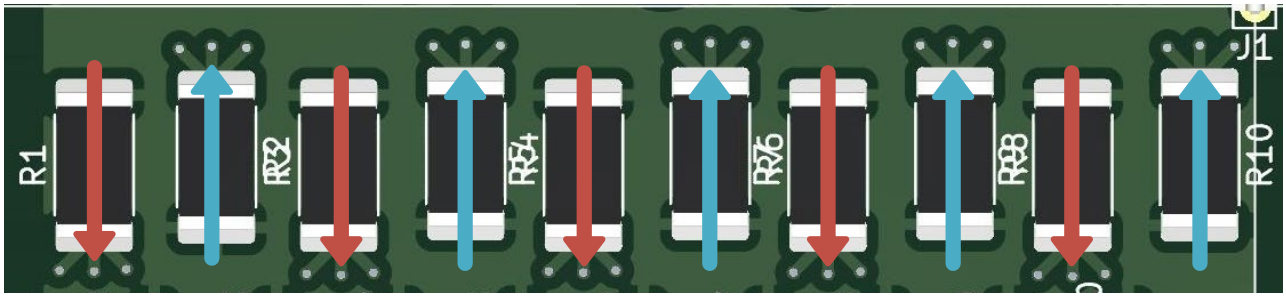


Fig. 2. Direction of the current through the resistor network with field cancellation, forcing opposite currents.

Field cancellation. The second configuration takes advantage of the mutual inductance concept, which should be added to the self-inductance of each device in two-layer conductors [8]. Equation (1) represents the value of the mutual inductance, being μ_0 and μ_r vacuum permeability and relative permeability of the insulation material, $l, w,$ and h are length, width and thickness of the conductors, d is the distance between them, k is the correction factor and φ is the angle between the current directions [9].

$$M = \frac{\mu_0 \mu_r l h}{\pi \sqrt{4(d + h)2 + kw^2}} \cos \varphi \quad (1)$$

By forcing opposite current between subjacent devices, $\varphi = 180$ °, mutual inductance M is made negative, subtracting the mutual inductance between devices to the self-inductance [10]. As observed in Fig. 2, in where the direction of the current through the resistors is indicated, the subjacent currents are made opposite and transferred to the lower layer of the PCB with vias in the lower or upper end of the resistor.

Radial. The third configuration combines the field cancellation technique in the previous configuration, with the radial layout approach in [6], and is shown in Fig. 1(c). This approach intends to reduce the area required for the current sensing network, as well as embracing the coaxial connector used to extract the shunt signal, ideally reducing the layout inductance. This approach is successful in [6], at lower current, being able to integrate the SMD resistors in a very compact way, but at tens of Amps, and with the bigger device footprints, this approach needs to be tested.

Experimental Testing

Setup. The three current sensing networks, as well as the coaxial shunt are tested using the double pulse testing (DPT). This test allows to evaluate the switching behavior of devices, as well as the layouts, and is the ideal test to compare the fast current sensing performance of the different configurations. The test, shown in Fig. 3, is done by charging an inductor to the desired current by keeping the device under test (DUT) on, then switching the DUT off to evaluate the turn-off. The test current is kept in the inductor recirculating it in a freewheeling diode, or the body diode in the case

two equal devices are used. Next, the DUT is turned on to evaluate the turn-on transition at the desired load current. The transient currents in the test are used to compare the different current measurement networks. The same setup is used, shown in Fig. 3(c), with the same layout for every tested board, being the only difference the current sensing network.

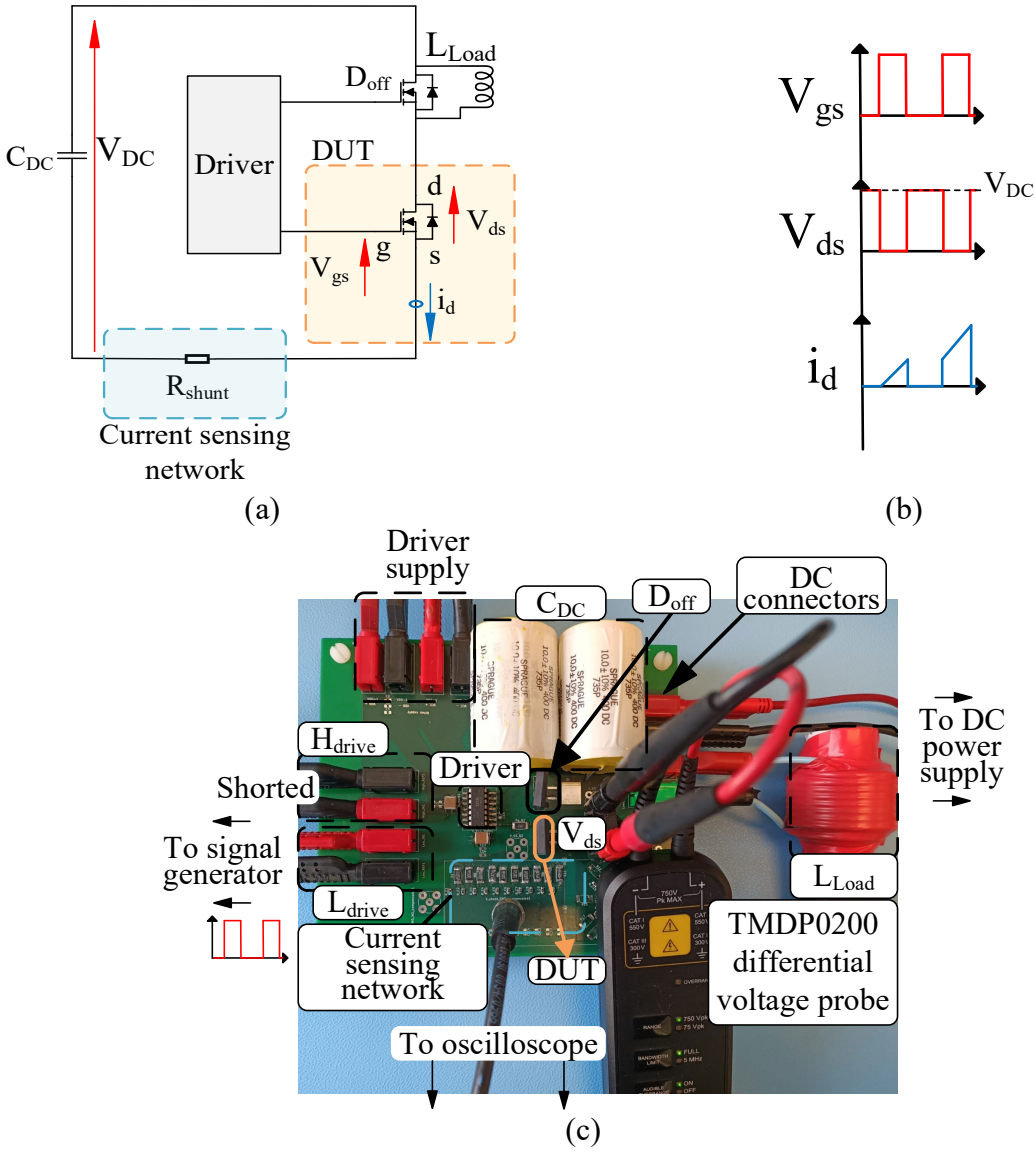


Fig. 3. DPT setup, (a) circuit diagram with the measured parameters (b) the voltage and current in the DUT terminals and (c) board and laboratory setup layout.

Impedance analysis. The impedance of all the current measurement networks is analyzed using the Bode100 equipment. First, the current sensing network is isolated and measured alone. Fig. 4 shows the results, being Fig. 4(a) the impedance and Fig. 4(b) the inductance measurements. Focusing on the second one, it can be concluded that all the proposed SMD networks reduce the inserted inductance at high frequency, over 10 MHz, when compared to the coaxial shunt. As for the proposed layouts, the configurations with the field cancellation get the lowest inserted inductance. The results are analyzed at over 10 MHz due to the expected fast current rise and fall times, tens of nano seconds, leading to high frequency excitation in the switching loop.

To be able to validate the impedance measurement results, they must be compared to the switching test results. However, the switching test will show the inductance in the whole switching loop, so new impedance measurements are performed considering the whole switching loop, and shown in Fig. 5. As expected, the inductance of the whole switching loop is higher than the one of the isolated current sensing network. However, the trend in high frequency is the same, being the layouts with the field cancellation the ones with the least inductance.

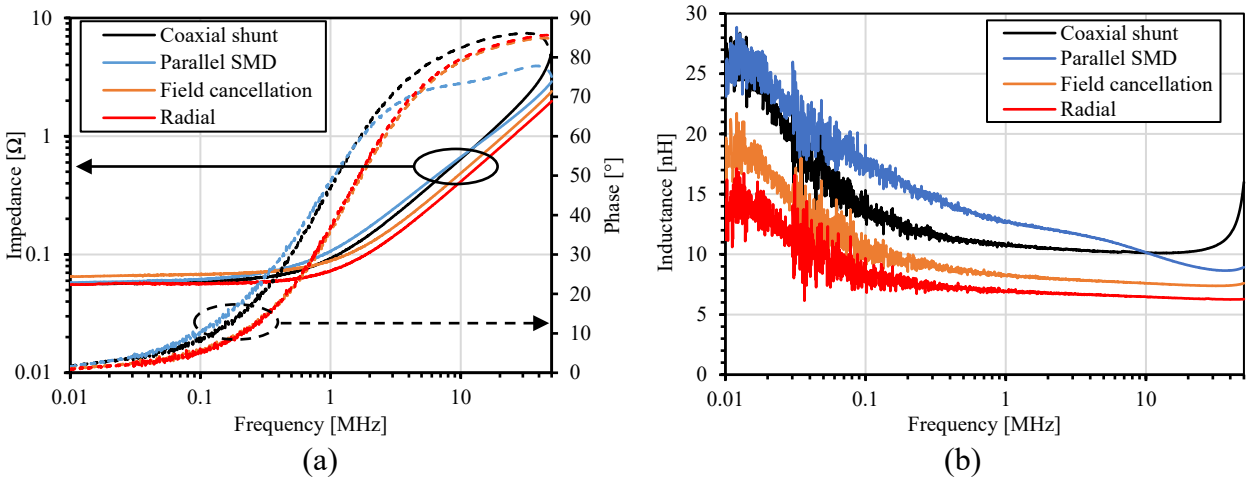


Fig. 4. Impedance measurement of the current measurement network, (a) the impedance with magnitude and phase and (b) the inductance.

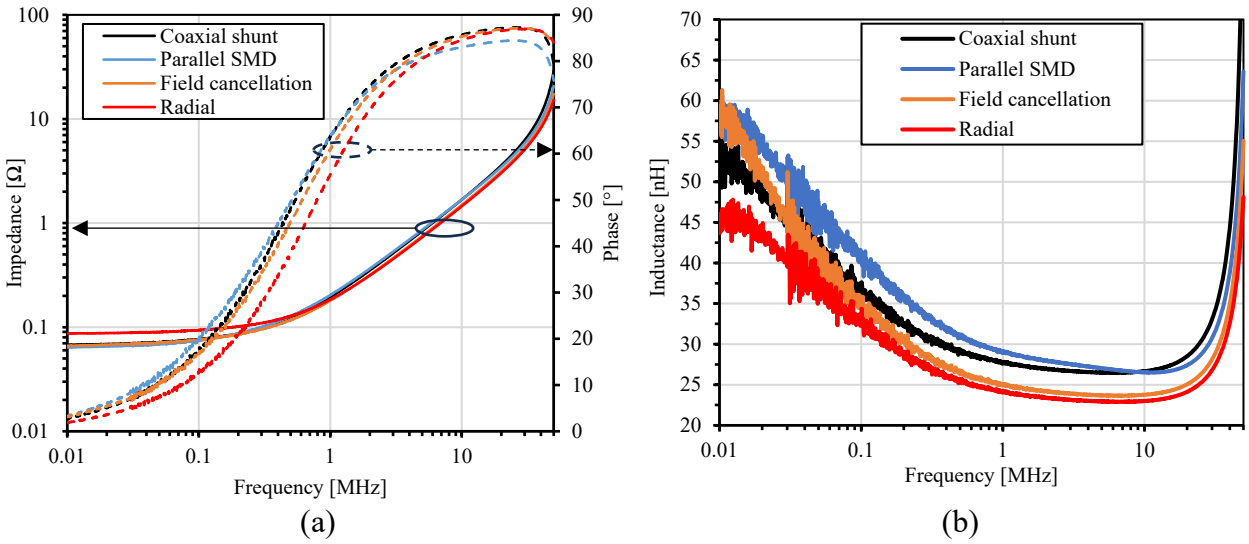


Fig. 5. Impedance measurement of the whole switching loop, (a) the impedance with magnitude and phase and (b) the inductance.

To validate the testing setup and the impedance measurements, the difference between the switching loop inductance, L_{SL}, and the current measurement loop inductance, L_{CMN}, calculated as $L_{SL} - L_{CMN}$, is calculated for all the configurations and shown in Fig. 6. The result are very similar for every configuration, as the calculated inductance is the inductance added by all the power components in the DPT setup, which are the same for all the current measurement networks. The maximum difference between any configuration at 25 MHz is only 1.2 nH, validating the testing setup and the impedance measurements.

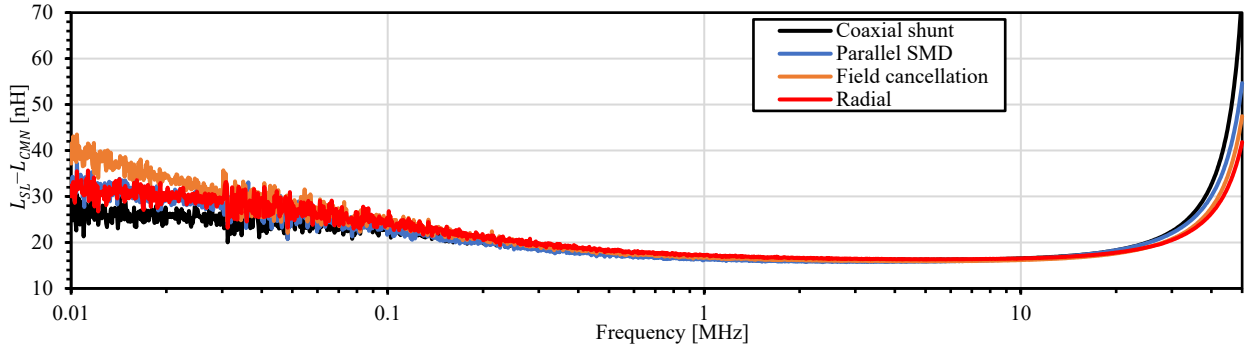


Fig. 6. $L_{SL} - L_{CMN}$ inductance calculation for the different proposed configurations.

Switching test. Finally, the DPT is executed with every current sensing network, and both the current and voltage waveforms are compared, Fig. 7. The study focuses on the turn-off transition, being the one causing the potentially dangerous overshoot for the SiC in space. First, it should be noted no difference is observed between the proposed networks and the coaxial shunt in the sensed current. As the measurements performed by the coaxial shunt are considered as the reference, the proposed networks are validated for a correct current sensing. However, and due to a difference in the inserted inductance, a different overshoot value is observed in the turn-off voltage. The overshoot value is defined by (2), being L_s the total stray inductance in the switching loop, and di/dt the current derivative in the switching transition.

$$Overshoot = V_{DC} - L_s \frac{di}{dt} \tag{2}$$

Using (2) and measuring the di/dt and the overshoot values in the switching waveforms, L_s can be calculated, confirming the results obtained in the impedance measurements: the configurations with the field cancellation layout obtain the least overshoot thus insert the least inductance, repeating the trend in the measurements in Fig. 5(b).

Finally, the inductances calculated from the switching waveforms are compared with the ones measured in the impedance analysis, and shown in Table 1. Following the effective frequency theory, the measured inductance value should be given depending on the current fall or rise time [11]. In the turn-off, the current fall time is 12 ns, leading to 26.9 MHz. This frequency value is just used to identify the frequency for the impedance measurement. Accurate measured values for each waveform and configuration are used to calculate the inductance in the tun-off transition using (2). Both the measured inductance and the inductance calculated with the switching waveforms match, validating the measurements and calculations.

Table 1. Measured and calculated inductance of the current measurement networks.

Test	Coaxial shunt	Parallel SMD	Field cancellation	Radial	Unit
Measured [26.9 MHz]	31.2	29.4	26.9	25.7	nH
Turn-off [Waveforms]	32.5	29.6	26.6	25.1	nH

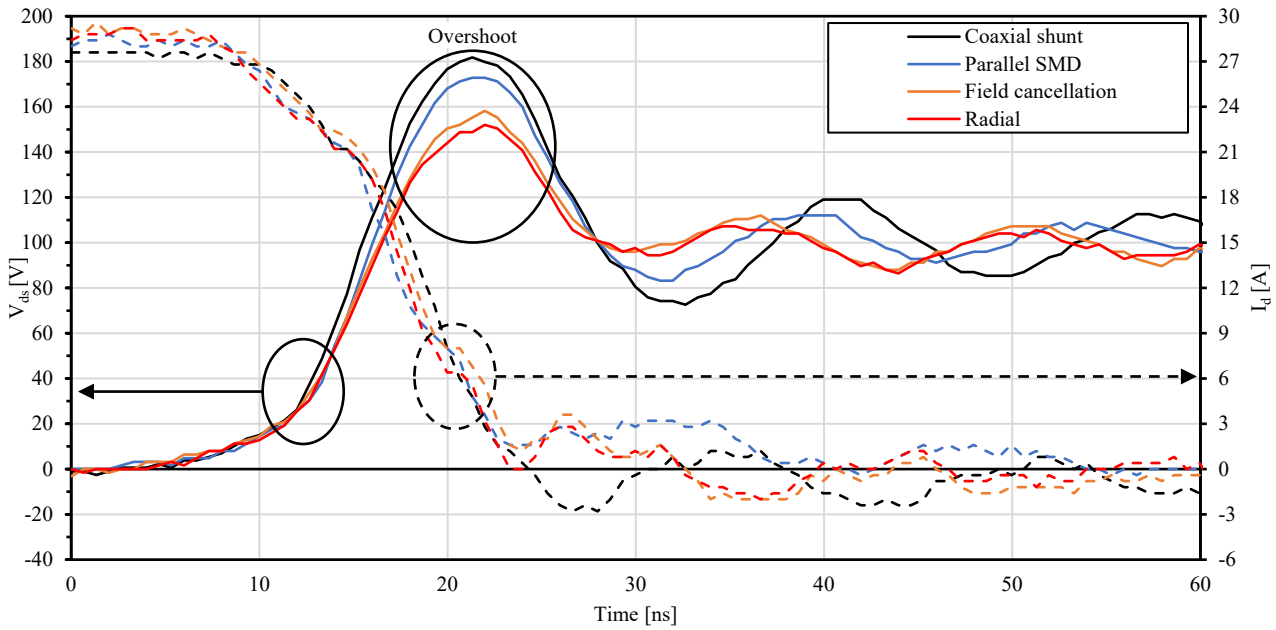


Fig. 7. Switching waveforms of the turn-off transition for the different configurations, highlighting the overshoot.

Analyzing the results in Table 1, it is seen the current sensing with parallel SMD network reduces the inserted inductance of the switching loop 5.7 % when compared to the coaxial shunt. However, applying the field cancellation technique to the same layout reduces the inductance 13.8 % when compared to the coaxial shunt, validating the field cancellation technique. Using the radial approach, the inductance reduction when compared to the coaxial shunt is 17.6 %, improving the layout even more. These results can easily be seen analyzing the highlighted overshoot in Fig. 7, with the best layouts obtaining the lowest overshoot.

Conclusion

SMD resistor networks are proposed as current sensing networks for SiC devices in space, to avoid the overshoot generated by the high inserted inductance of the coaxial shunts. The current sensing performance of the proposed networks is validated through DPT, and by comparing the current waveforms obtained with the one sensed with the coaxial shunt. In addition, it is demonstrated the layouts using field cancellation techniques, forcing opposite current through subjacent resistors insert less inductance in the switching loop than the just parallel layout.

With the SiC devices being considered for the HP systems in space, the voltage they block should be monitored with care. In this aspect, the overshoot during the turn-off transitions due to the switching loop inductance can be dangerous. Using simple and low inductance current sensing networks to reduce the overshoot will contribute to the adoption of the SiC devices in space.

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