Key Engineering Materials
ISSN: 1662-9795, Vol. 1023, pp 7-12
doi:10.4028/p-Xtm1Pm

Submitted: 2024-09-20
Revised: 2025-08-01
Accepted: 2025-08-04
Online: 2025-09-10

Cost-Effective Design and Optimization of a 3300-V Semi-Superjunction 4H-SiC MOSFET Device

Kyrylo Melnyk[1,a*+], Marco Boccarossa[1,2,b+], A.B. Renz[1,c], Q. Cao[1,d], P.M. Gammon[1,e], V.A. Shah[1,f], L. Maresca[2,g], A. Irace[2,h], Marina Antoniou[1,i]

[1]University of Warwick, Coventry, United Kingdom

[2]University of Naples Federico II, Naples, Italy

[a]Kyrylo.Melnyk@warwick.ac.uk, [b]Marco.Boccarossa@warwick.ac.uk, [c]Arne.Renz@warwick.ac.uk, [d]Q.Cao.2@warwick.ac.uk, [e]P.M.Gammon@warwick.ac.uk, [f]Vishal.Shah@warwick.ac.uk, [g]Luca.Maresca@unina.it, [h]Andrea.Irace@unina.it, [i]Marina.Antoniou@warwick.ac.uk

Keywords: Superjunction, Semi-Superjunction, Trench MOSFET, Planar MOSFET, High Voltage.

Abstract. This study investigates a cost-effective semi-Superjunction (SSJ) solution for 3.3 kV silicon carbide (SiC) MOSFETs, comparing planar and trench configurations. The semi-SJ method, utilizing side-wall implantation and silicon oxide trench refill, offers a practical alternative to the more complex multi-epitaxial growth approach. Through TCAD simulations, the planar semi-SJ MOSFET (planar-SSJ) achieved a 48 % reduction in specific on-state resistance (7.5 mΩ.cm^2) and a 4.5 % improvement in maximum blocking voltage (4210 V) compared to conventional planar MOSFET. The trench semi-SJ MOSFET (trench-SSJ), depending on the deep trench angle, can further reduce the specific on-state resistance by 52 % (7.0 mΩ.cm^2) and improve the maximum blocking voltage by 6 % (4285 V), while also providing a wider implantation window and a lower gate-oxide electric field.

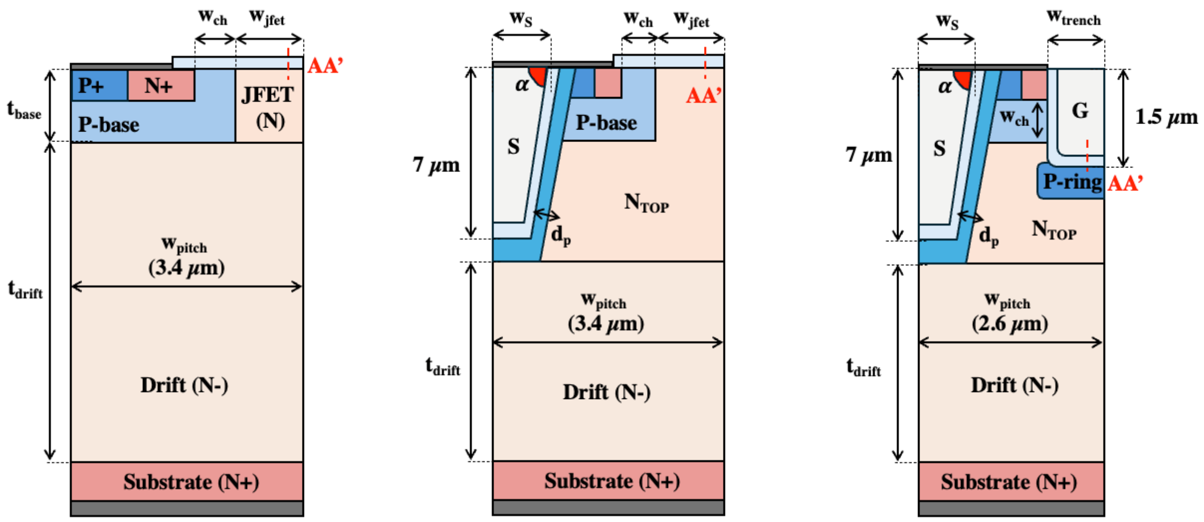
Introduction

Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are increasingly replacing silicon (Si) in high-switching applications within the blocking voltage range of 650 V to 1700 V [1]. In high-voltage SiC MOSFETs, especially those exceeding 3000 V, the thick drift region is the major contributor to on-state resistance, resulting in conduction losses comparable to or greater than those of silicon insulated-gate bipolar transistors (IGBTs) [2]. To overcome the 1D unipolar limit of SiC MOSFETs, Superjunction (SJ) and semi-Superjunction (SSJ) technologies have been introduced, offering an improved tradeoff between conduction losses and breakdown voltage (BV) [3,4]. Unlike in Si, the commercialization of these designs in SiC faces challenges due to the complexity of forming deep p-type pillars. Two main fabrication methods exist for SJ structures: 1. Multi-epitaxial growth with shallow aluminum (Al) implants to form the p-pillar, and 2. Side-wall Al implantation through deep trenches, which are then refilled with silicon oxide (SiO2) [1-5]. Both techniques have been experimentally demonstrated in [2,4,5], with the multi-epitaxial growth method being more complex due to potential misalignment issues and the requirement for multiple implantation steps. While multi-epitaxial growth enables the implementation of a full-SJ design, side-wall implantation is typically limited by implantation angles and trench depth, favoring a semi-SJ design [2,3]. Despite these limitations, side-wall implantation offers significant on-state performance improvements with simpler fabrication steps compared to the multi-epitaxial approach.

The authors have previously introduced cost-effective methods for fabricating Schottky barrier diodes (SBDs), optimizing a semi-SJ structure, enabling the SJ effect with minimal implantation depth and wide implantation window [3,6]. In this study, a 3.3 kV SSJ SiC MOSFET is proposed using these techniques, with the goal of reducing fabrication costs and improving on-state resistance. TCAD simulations were used to evaluate and compare the performance of a standard planar structure, a planar Semi-SJ MOSFET (planar-SSJ), and trench semi-SJ MOSFET (trench-SSJ) devices.

Structure Description

The half-cell pitch schematic of the planar, planar-SSJ and trench-SSJ MOSFET is shown in Fig. 1, with highlighted key parameters. The planar MOSFET structure was based on [7] and adjusted to match the on-state performance in [8]. The p-base depth (t_{base}) of 1.0 µm, half-cell JFET opening (w_{JFET}) of 0.7 µm and half-cell pitch (w_{pitch}) of 3.4 µm is in both conventional and planar-SSJ designs. The channel width of 0.5 µm and drift doping concentration of $3{\times}10^{15}$ cm^{-3} across all three designs. The half-cell pitch in the trench-SSJ design is 2.6 µm and based on the optimization results detailed in [3], the optimal depth of the source connected trench is 7 µm and 1.5 µm (half-cell) wide (w_S), with a nitrogen (N) n-top layer doping concentration of $3{\times}10^{16}$ cm^{-3} in both planar and trench-SSJ configurations. Note, that the active trench is protected with the p-ring implanted through the bottom of the active trench, to protect the gate-oxide from high electric fields (EFs). The depth of the p-ring is fixed at 0.5 µm with the peak doping concentration of $4{\times}10^{18}$ cm^{-3}. The side-wall p-implantation depth (d_p) is 0.25 µm and the doping concentration is part of the design optimization [3,6].

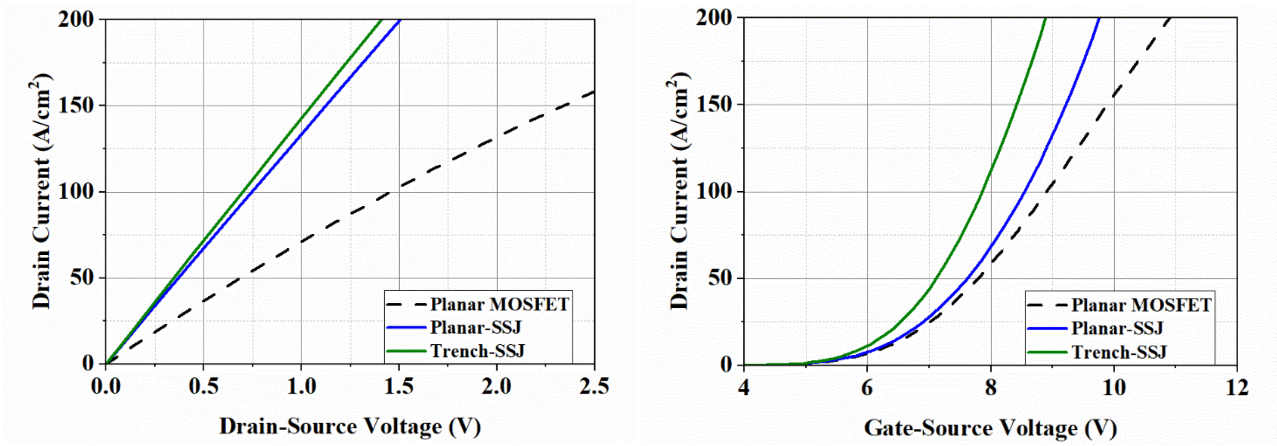


(a) (b) (c)

Fig. 1. (a) planar MOSFET, (b) planar-SSJ MOSFET and (c) trench-SSJ MOSFET.

On-State Performance

The on-state and transfer characteristics are shown in Fig. 2 (a) and (b). The channel doping concentration was calibrated to result in threshold voltage (V_{th}) of 3.5 V at 1 mA/cm^2. In both on-state and off-state simulations, the fixed charge density (Q_F) of $1{\times}10^{12}$ cm^{-2} and D_{it} trap density extrapolated from [9] was modelled at the interface between SiO_2 and SiC. Note, that the on-state performance of the planar-SSJ device is not affected by the side-wall doping concentration, due to a small JFET effect along the semi-SJ region [3]. This is also true for the trench-SSJ configuration, where the pitch size is smaller compared to the planar solutions. The specific on-state resistance ($R_{ON,SP}$) at 100 A/cm^2 is 14.5 mΩ.cm^2, 7.5 mΩ.cm^2 and 7.0 mΩ.cm^2 for planar (w_{pitch} – 3.4 µm), Planar-SSJ (w_{pitch} – 3.4 µm) and Trench-SSJ (w_{pitch} – 2.6 µm) MOSFETs, respectively.



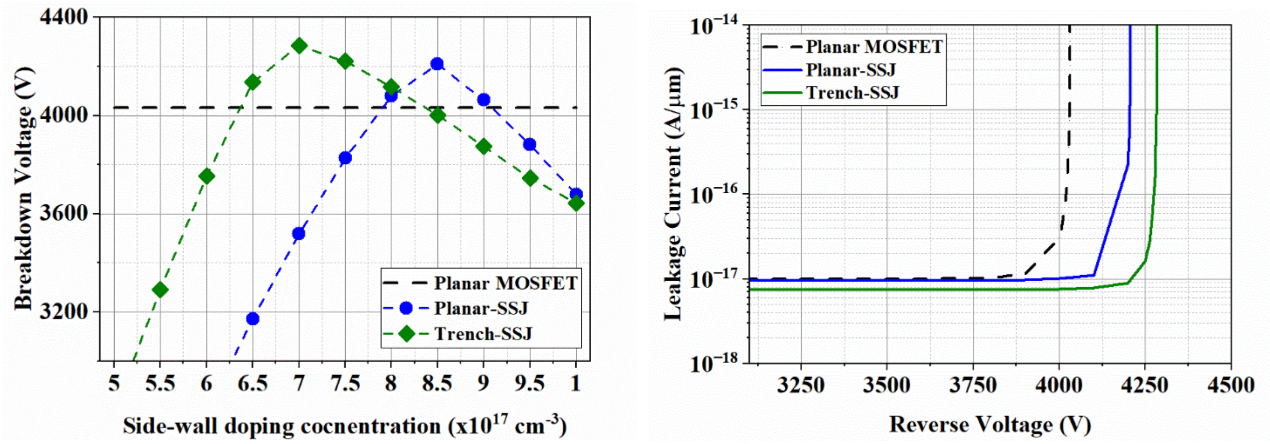
(a) (b)

Fig. 2. Planar, planar-SSJ (α = 80 degrees) and trench-SSJ (α = 80 degrees) MOSFET (a) on-state characteristics and (b) transfer characteristics.

This represents a 48 % and 52 % reduction in specific on-state resistance for planar-SSJ and trench-SSJ designs compared to the conventional planar MOSFET. While the on-state improvement of the trench-SSJ compared with the planar-SSJ is small, due to the introduction of a p-ring at the bottom of the active trench. However, a narrower pitch compensates for this additional resistance and also enhances the off-state performance due to an improved charge balance, which will be discussed in the next section.

Off-State Performance

As described in [3,6], the blocking performance of the semi-SJ structure depends on the charge balance between the side-wall p-layer and the fixed n-top layer (3×10^{16} cm^{-3}). It is also affected by the distance between deep trenches and the trench opening (ws). The trench angle (α – 80 degrees), shown in Fig. 1, causes uneven charge distribution in the semi-SJ region compared to ideal vertical p and n-pillars [1,3]. The conventional planar MOSFET has a maximum breakdown voltage (BV) of 4030 V. Fig. 3 (a) shows the BV of Planar-SSJ and Trench-SSJ designs as a function of the peak side-wall doping concentration, while Fig. 3 (b) presents the simulated reverse leakage current.



(a) (b)

Fig. 3. (a) BV versus p-implantation doping concentration and (b) off-state performance of the conventional MOSFET versus planar-SSJ (α = 80 degrees) and trench-SSJ (α = 80 degrees) with the peak side-wall doping concentration: 8.5×10^{16} cm^{-3} and 7×10^{16} cm^{-3}, respectively.

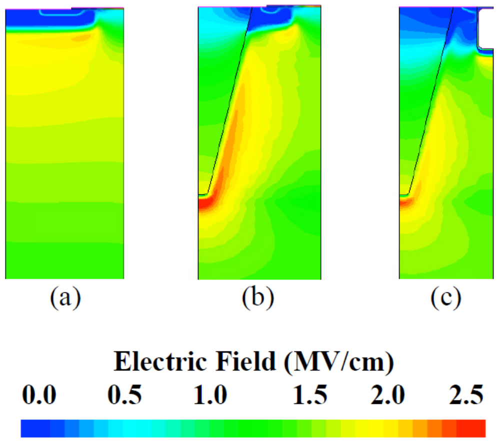


Fig. 4. EF distribution at 3.3 kV of: (a) Planar, (b) Planar-SSJ and (c) Trench-SSJ MOSFETs.

A high doping concentration of the p-implant increases the EF at the bottom of the trench, leading to breakdown, with the n-top layer (Q_N) remaining under-compensated at the surface. On the other hand, a lighter p-implant doping concentration increases the EF at the surface. As a result of the higher n-top doping concentration compared to the JFET doping in the planar MOSFET, this causes premature avalanche breakdown and a significant increase in the gate-oxide EF, the n-top layer at the surface is over-compensated. The maximum blocking voltage for angles $\alpha < 90$ degrees is achieved when the EF along the Y-axis (cutline AA' in Fig. 1) in the semi-SJ region becomes flatter. According to [1], in a vertical semi-SJ structure ($\alpha = 90$ degrees), a perfectly rectangular EF distribution indicates a charge-balanced condition. As illustrated in Fig. 3 (a), the BV of the Planar-SSJ is 4210 V and Trench-SSJ is 4285 V, when the peak side-wall doping concentration is 8.5×10^{17} cm^{-3} and 7×10^{17} cm^{-3}, respectively.

The EF distribution for all three designs can be seen in Fig. 4, where the side-wall doping concentration is 8.5×10^{17} cm^{-3} and 7×10^{17} cm^{-3} for the Planar-SSJ and Trench-SSJ, respectively. The higher EF at the bottom of the deep trench occurs in Planar-SSJ design, resulting in a poorer off-state performance compared to the Trench-SSJ. The n-top layer in the Planar-SSJ design is overcompensated and the narrower distance between deep trenches of the Trench-SSJ design, 1.1 µm compared to 1.9 µm in Planar-SSJ structure, improves the charge balance, resulting in a higher off-state performance and wider implantation window (see Fig. 3 (a)). Additionally, the gate-oxide EF through the cutline AA' (denoted in Fig. 1) at 3.3 kV is 1.8 MV/cm, 2.1 MV/cm and 0.9 MV/cm for the planar, Planar-SSJ and Trench-SSJ MOSFET, respectively.

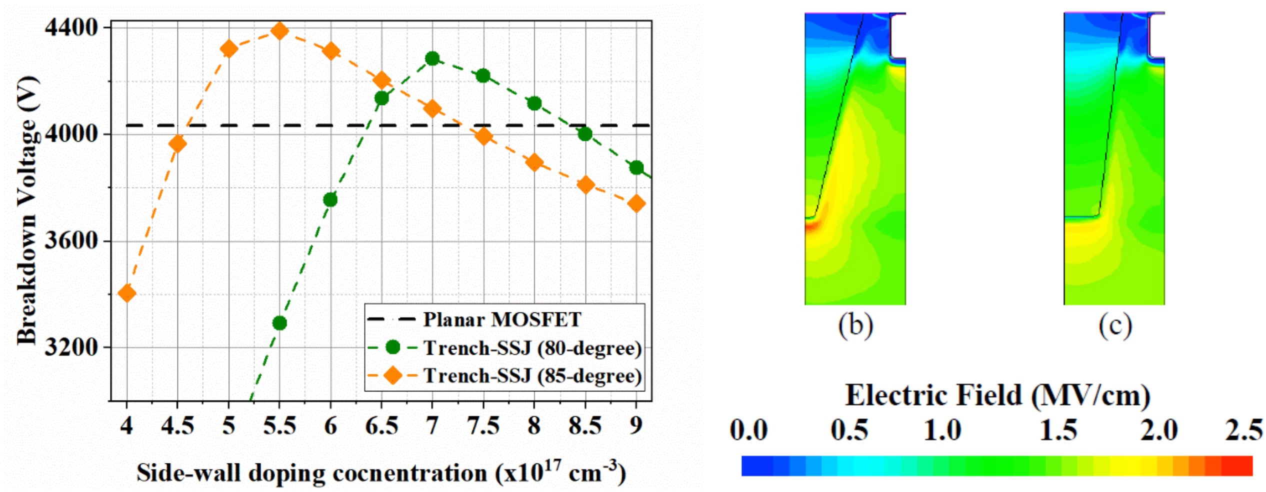


Fig. 5. (a) BV versus p-implantation doping concentration for Trench-SSJ with trench angle of 80 and 85-degrees; Trench-SSJ EF distribution recorded at 3.3 kV: (b) 80-degree trench angle (7×10^{17} cm^{-3}) and (c) 85-degree trench angle (5.5×10^{17} cm^{-3}).

Increasing the trench angle to 85 degrees, while maintaining the same trench opening (1.5 µm – half-cell), improves charge balance and increases the ideal BV (see Fig. 5 (a)). The EF distribution in Fig. 5 (b) and (c) is more uniform with the 85-degree angle and shows better charge balance across the semi-SJ region. This results in a maximum BV of 4389 V, when the peak side-wall doping concentration is 5.5×10^{17} cm^{-3}. Additionally, the EF at the bottom of the deep trench is reduced, lowering the EF in the deep trench oxide, which will positively impact long-term reliability. However, the 85-degree trench angle increases the JFET effect, resulting in a higher $R_{ON,SP}$ in the trench-SSJ configuration (from 7.0 mΩ.cm² to 8.2 mΩ.cm²). The on-state resistance can be reduced by narrowing the deep trench opening, but this adjustment may lead to un-implanted trench corners due to implantation angle geometry [2,3].

The performance of both Planar-SSJ and Trench-SSJ with trench angle (α) of 80 and 85-degrees designs, compared to the conventional planar MOSFET, is summarized in Table 1.

Table1. Static performance comparison between conventional and SSJ designs.

Structure:	α [degrees]	$R_{ON,SP}$ [mΩ.cm^2]	Gate-oxide EF [MV/cm]	Implantation window [cm^{-3}]	Max BV [V]
Planar	-	14.5 (-)	1.8 (-)	-	4030
Planar-SSJ	80	7.5 (- 48 %)	2.1 (+ 16.5 %)	8 – 9 ×10^{17}	4210 (+ 4.5 %)
Trench-SSJ	80	7.0 (- 52 %)	0.9 (- 50 %)	6.5 – 8 ×10^{17}	4285 (+ 6 %)
Trench-SSJ	85	8.2 (- 43.5 %)	0.9 (- 50 %)	5 – 7 ×10^{17}	4390 (+ 9 %)

Conclusion

In 3.3 kV SiC MOSFET devices, high on-state resistance is primarily due to the low drift doping concentration and thick drift region. The semi-SJ method discussed in this study, involves side-wall implantation and silicon oxide trench refill, which is a cost-effective solution that requires only two additional steps beyond the conventional planar or trench MOSFET process flow. This study demonstrates that the Planar Semi-SJ MOSFET (Planar-SSJ) reduces $R_{ON,SP}$ from 14.5 mΩ.cm² to 7.5 mΩ.cm² (a 48 % reduction) and improves the maximum blocking voltage from 4030 V to 4210 V (a 4.5 % increase) , compared to the conventional planar MOSFET. The Trench Semi-SJ MOSFET (Trench-SSJ) further reduces to 7.0 mΩ.cm² (a 52 % reduction) and improves the maximum blocking voltage to 4285 V (a 6 % increase), if the trench angle is 80-degrees. Reduction of the trench angle to 85-degrees has the trade-off between $R_{ON,SP}$ (8.2 mΩ.cm²) and maximum BV (4390 V). Additionally, both 80-degree and 85-degree Trench-SSJ designs show a lower gate-oxide electric field compared to the conventional and Planar-SSJ structures, which could enhance long-term reliability without a significant compromise on the on-state performance.

Acknowledgements

The AdvanSiC project has received funding from the European Union’s Horizon Europe programme under grant agreement No 101075709. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union. Neither the European Union nor the granting authority can be held responsible for them.

References

[1] G. W. C. Baker *et al*., "Optimization of 1700-V 4H-SiC Semi-Superjunction Schottky Rectifiers With Implanted P-Pillars for Practical Realization," in *IEEE Transactions on Electron Devices*, 2022.

[2] X. Zhong, B. Wang and K. Sheng, "Design and experimental demonstration of 1.35 kV SiC super junction Schottky diode," *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD).*

[3] K. Melnyk *et al*., "3.3 kV 4H-SiC Trench Semi-Superjunction Schottky Diode With Improved ON-State Resistance," in *IEEE Transactions on Electron Devices*, 2024.

[4] M. Baba, T. Tawara, T. Morimoto, S. Harada, M. Takei and H. Kimura, "Ultra-Low Specific on-Resistance Achieved in 3.3 kV-Class SiC Superjunction MOSFET," *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD).*

[5] S. Harada *et al*., "First Demonstration of Dynamic Characteristics for SiC Superjunction MOSFET Realized using Multi-epitaxial Growth Method," *2018 IEEE International Electron Devices Meeting (IEDM)*, 2018.

[6] K. Melnyk *et al*., "Design and Optimization of 3.3 kV Silicon Carbide Semi-Superjunction Schottky Power Devices," *2024 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Bremen, Germany, 2024.

[7] X. Chen *et al*., "Different JFET Designs on Conduction and Short-Circuit Capability for 3.3 kV Planar-Gate Silicon Carbide MOSFETs," in *IEEE Journal of the Electron Devices Society*, 2020.

[8] H. Kono *et al*., "3.3 kV all SiC MOSFET module with Schottky barrier diode embedded SiC MOSFET," PCIM Europe Conference, 2021.

[9] S. Yu, M. H. White and A. K. Agarwal, "Experimental Determination of Interface Trap Density and Fixed Positive Oxide Charge in Commercial 4H-SiC Power MOSFETs," in *IEEE Access*, 2021.