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SiC Half-Bridge Modules to Improve Efficiency and Reduce Area of High-Power Motor Drives in Space

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Abstract. This work proposes SiC half-bridge modules to improve the high-power motor drive systems in space. The high current capability of the modules allows to reduce the number of required components, reducing the required PCB area. Using analytical loss calculation models the losses and the efficiency of the Si and SiC configurations is calculated, obtaining better results with the SiC due to the lower conduction losses, even if the voltage rating of the devices is severely derated to avoid single event burnouts in the space application.

Introduction

The new missions in space will require high power (HP), as the main space agencies aim to land on the moon and even create a permanent lunar base [1], [2]. Among these HP systems, electric motor drives gain relevance for their application in launchers, electric pump control, lunar landers, cargo ships and the heavy machinery that will be required in the permanent lunar base construction and maintenance.

This work considers a three phase (3P) 56 kW electric motor drive, using the 2 level (2L) 3P voltage source converter (VSC) topology. As most HP motor drives in space, it has a dedicated battery, which operates at 150 V when fully charged, but can go as low as 100 V in the end of discharge. Fig. 1 shows the electrical architecture of the system. At the lowest input voltage and maximum power, the 2L 3P VSC must operate at 300 ARSM, creating a challenging environment for current space technology.

Following the approach in terrestrial HP electronics, SiC devices are being considered to improve the technical figures of HP systems in space, mostly due to the limitations of the space qualified Si technology. Even if SiC devices have already been tested in space systems [3],[4],[5], [6], they are susceptible to single event effects (SEE) and need to derate their voltage considerably to avoid SE burnouts (SEB) [7], [8], [9]. The SEE test results analyzed in the bibliography [7], [8], [9], show 1200 V SiC MOSFETs can suffer degradation at blocking voltages as low as 300 V at high Liner Energy Transfers (LET). This rules 650 V SiC devices out of this application, and forces to use 1200 V SiC MOSFETs, but it also opens up the opportunity to use HP half-bridge (HB) modules containing these 1200 V SiC MOSFETs, as specified in Fig. 1.

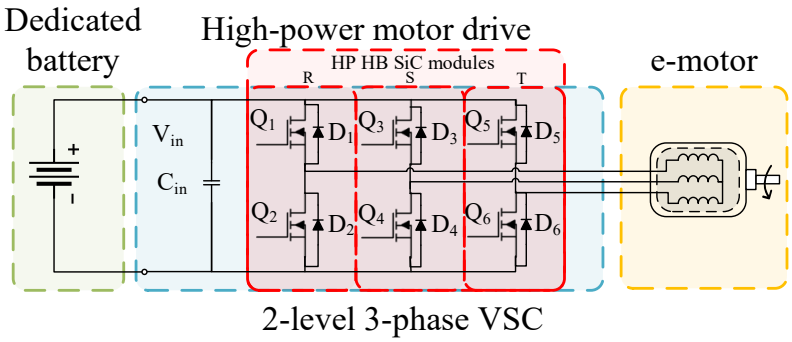

Fig. 1. The electrical architecture for high-power motor drives with HP HB SiC modules in space.

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$18.03x13.61\ mm$

$109.85x62\ mm$

*Package photos adapted from Infineon datasheets.

(a) (b)

Fig. 2. The selected devices with dimensions, (a) Si MOSFET and (b) SiC half-bridge module.

Table 1. Main ratings of the selected devices.

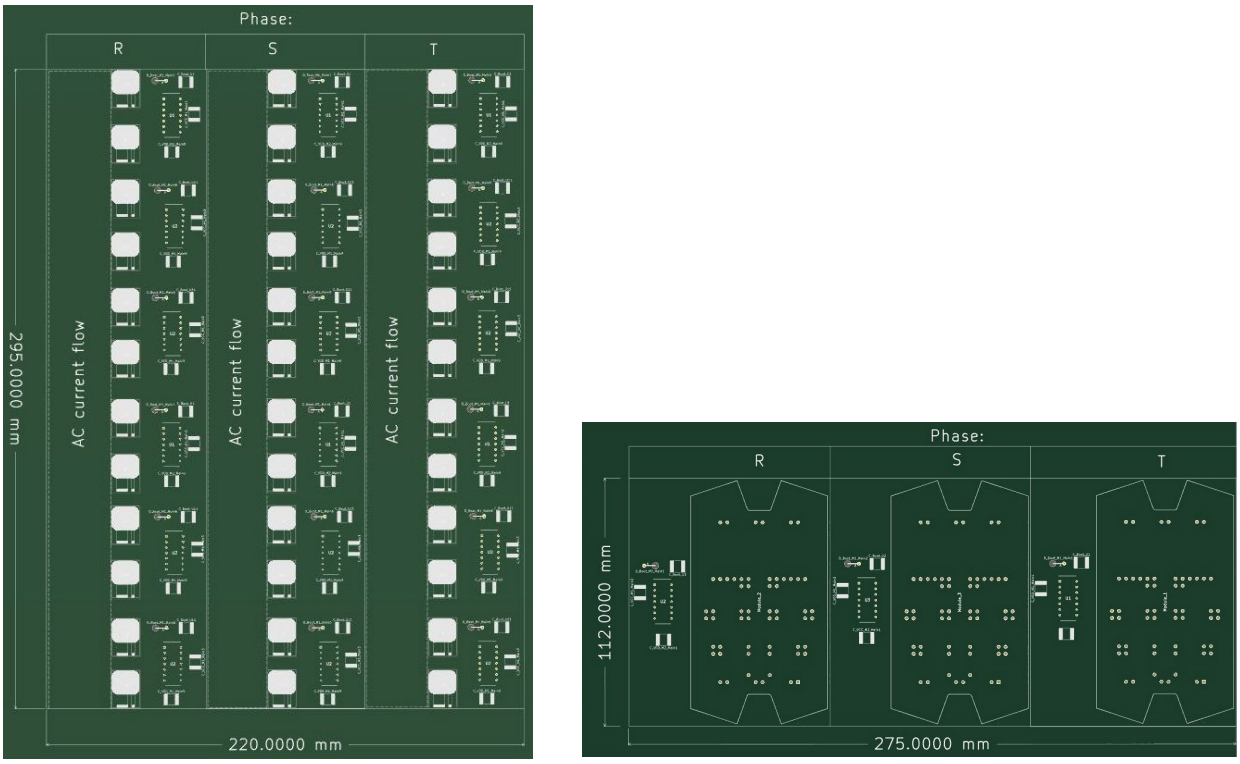
Parameter	Si MOSFET	SiC module	Unit
Part number	IRHNS9A7264	FF2MR12W3M1H_B11	/
Technology	Space qualified Si MOSFET	Industrial SiC half-bridge module	/
V_{ds}(max)	250	1200	V
I_d(max) continuous ($T_j = 100\ ^\circ C\ for\ Si - 175\ ^\circ C\ for\ SiC$)	52	400	A
Required number	36	3	# of discretes/modules

The paper compares the converter setup for a 56 kW motor drive with space qualified Si MOSFETs and 1200 V SiC HP HB modules, in terms of printed circuit board (PCB) design, as well as the thermal and electrical performance. The next steps to follow up on the project are also presented.

Converter Setup

Device Selection. 250 V components must be used to switch 150 V in space, applying the derating rules [10]. To reach the required RMS current in the maximum power, 300 A_{RMS}, and considering IRHNS9A7264 Si MOSFETs with 52 A continuous maximum current at 100 ˚C, 6 parallel devices must be used, 12 per phase to get the high and low sides, and 36 in total to get the three phases of the 2L 3P VSC. Using the FF2MR12W3M1H_B11 1200 V SiC HB module, with 400 A continuous maximum current at 175 ˚C only 3 modules are required to form the whole 2L 3P VSC. The selected driver for both configurations is the space qualified high and low side, HV and high speed RIC7S113 driver. In the case of the SiC modules, two drivers per module are used, to double the gate current capability. Fig. 2 shows the two selected devices, together with their dimensions. Table 1 shows their main ratings. It should be noted the Si device is surface mounted, while the SiC module is screwed directly to the cooling system, and the PCB press fitted on top.

PCB Layout. The power stage design is shown in Fig. 3, using the space qualified high and low side, HV and high speed RIC7S113 driver, and the required bootstrap components. In the case of the SiC modules, the second driver is connected directly underneath the main driver in the bottom layer. This is possible because the SiC modules are connected to the PCB by press-fitting, and the generated gap is enough to place the second driver. By doing so, no extra PCB area is required and the gate current is doubled. In the Si configuration, this cannot be done because the Si MOSFET is SMD, thus the PCB must be directly connected to the cooling system to ensure thermal dissipation. The converter with the 36 Si MOSFETs and their driving components require 649 cm^2 in the PCB, Fig. 3(a). However, the configuration with the larger SiC HB modules, only needs 308 cm^2, as only three modules and driving components are needed. The required PCB area is reduced 52.5 % with the use of SiC HB modules.



(a) (b)

Fig. 3. PCB area required for the motor drive power stage with (a) space graded Si MOSFETs and (b) SiC modules.

DC Losses and Thermal Restrictions. The DC resistance of any conductor is proportional to its length. Following this principle, we can deduce the DC resistance thus the DC losses in the PCB required by the Si MOSFETs will be around 2.5 times higher than the ones in the PCB with SiC modules. These losses are proportional to the square of the RMS current, so not neglectable at all in such high-current systems.

The second consideration is the thermal design of the two configurations. In the first design, the Si devices are SMD, dissipating heat directly to the PCB. This heat should be added to the one directly generated in the PCB by the DC losses mentioned before. However, having all the components in one side of the PCB would allow to directly connect the PCB to the cooling system, making the thermal conduction of the PCB easier.

On the contrary, the SiC modules are optimized for thermal performance, having a thermal plate directly conducting the heat to the cooling system. In fact, the modules are screwed to it, connecting the PCB on top by press-fitting it. Again, this makes the thermal management of the SiC modules easier but complicates the dissipation of the DC losses in the PCB.

Finally, if the device thermal resistance is compared, a big difference can be observed. The junction to PCB thermal resistance of the Si MOSFETs is 1.6 K/W, while it is 0.128 K/W, 12.5 times less, for each MOSFET in the SiC HB module. Each SiC module is composed of two parallel dies in the high side, and two parallel dies in the low side, composing 4 dies (MOSFETs) per module and 12 in total in the whole converter. In the case the two configurations generate the same losses, which it is seen to be false in the following section, each Si MOSFET would have to dissipate less power than each SiC MOSFET because of their parallel connection. However, if both use the same cooling system, the temperature increase in each Si MOSFETs would be 4 times higher than in each SiC MOSFET, showing the advantages of the thermal optimization of the SiC modules.

Electrical Performance

Analytical Loss Model. The electrical performance of the two configurations is tested using analytical equations to calculate the losses. The conduction losses are calculated using the generic equation (1),

$$P_{cond} = V_f \cdot I_{Avg} + R_{DS(on)} \cdot {I_{RMS}}^2 \tag{1}$$

V_f is the forward voltage drop, which is considered 0 V simplifying to (2) in MOSFET technology.

$$P_{cond} = R_{DS(on)} \cdot {I_{RMS}}^2 \tag{2}$$

I_{RMS} calculation is done for the 2L 3P VSC converter, considering sinusoidal AC current and the conduction times of the high side and low side switches for all the fundamental period [11]. (3) is synthesized being M_a the modulation index and φ the power factor of the inverter.

$$P_{cond} = {I_{peak}}^2 \cdot R_{DS(on)} \cdot \left(\frac{1}{8} + \frac{M_a}{3\pi} \cdot \cos\varphi\right) \tag{3}$$

Next, the switching losses of the MOSFETs are calculated. The calculations are based on (4), where the on and off transitions are separated, being t_{on} the turn-on time, and t_{off} the turn-off time. f_{sw} is the switching frequency of the converter.

$$P_{sw} = \left(\frac{1}{2} I_{RMS} \cdot V_{DC} \cdot t_{on} + \frac{1}{2} I_{RMS} \cdot V_{DC} \cdot t_{off}\right) \cdot f_{sw} \tag{4}$$

The switching times are represented depending on the gate charges, the gate to source charge Q_{GS}, Q_{GD} the gate to drain charge and driving circuit characteristics such as the gate current I_G. Considering the turn-on circuit and the turn-off circuit are the same, (5) is derived, and replacing (5) and I_{RMS} for the 2L 3P VSC in (4), the expression (6) is obtained for the switching losses.

$$t_{on} = t_{off} = \frac{Q_{GS} + Q_{GD}}{I_G} \tag{5}$$

$$P_{sw} = I_{peak} \cdot \sqrt{\frac{1}{8} + \frac{M_a}{3\pi} \cdot \cos\varphi} \cdot V_{DC} \cdot \frac{Q_{GS} + Q_{GD}}{I_G} \cdot f_{sw} \tag{6}$$

Next, the body diode losses are calculated. In the 2L 3P VSC the body diodes conduct during dead times DT, which is considered constant, 500 ns, in this work. First, the duty cycle of the diode D_{diode} is calculated with respect to the switching period $T_{sw} = {}^1/_{f_{sw}}$ (7).

$$D_{diode} = \frac{DT}{T_{sw}} \tag{7}$$

Then, the average and RMS currents are calculated for the diode, in order to populate (1). The conduction time of the diode is constant during the fundamental period, and a diode only conducts during one half of the fundamental period, so the conduction losses of the diode are calculated with (8), being V_f the forward voltage drop of the body diode, and R_{diode} the conduction resistance, which is obtained from the conduction characteristic plot in the datasheets.

$$P_{cond_{Diode}} = D_{diode} \cdot \left(V_f \cdot \frac{I_{peak}}{\pi} + \frac{I_{peak}^2}{4} \cdot R_{diode} \right) \quad (8)$$

Last, the switching losses of the diodes are also calculated, which are considered to occur due to the reverse recovery charge, Q_{rr}, and shown in (9) [12]. Remember each diode only participates during half of the fundamental period. Q_{rr} is considered negligible in the case of the SiC MOSFETs, so the diode switching losses are neglected for the SiC converter.

For the Si, and even if the manufacturer only provides the Q_{rr} data for the maximum current, the reverse recovery charge increases with the forward current, I_f, of the diode [12]. For this loss model, the Q_{rr} is considered to increase with the square root of I_f in the diode, until the data provided by the manufacturer is reached. So a specific Q_{rr} is considered for each operating point, depending on the current conducted by the diode.

Table 2. Main technical characteristics of the selected devices at $V_{ds} = 100\ V$, obtained from the manufacturer datasheets.

Parameter	Si MOSFET	SiC module	Unit
Q_{GS}	64	400	nC
Q_{GD}	48	25	nC
$Q_{rr}(I_f = 50\ A)$	4.864	/	µC
$R_{DS(on)}$ $(T_j = 100\ ^\circ C\ for\ Si - 175\ ^\circ C\ for\ SiC)$	28.9	3.09	mΩ

$$P_{sw_{Diode}} = \frac{1}{2} \cdot Q_{rr}(I_f) \cdot V_{DC} \cdot f_{sw} \quad (9)$$

Calculating a variable $Q_{rr}(I_f)$ only causes marginal differences in the losses, however, using this approach avoids penalizing the Si in low power operation conditions, which would happen if the full Q_{rr} losses were considered. In reality, the diode only stores the Q_{rr} corresponded to the conducted forward current in each operation condition, thus generating lower switching losses in low power operations.

The main technical characteristics to populate the analytical model are shown in Table 2, obtaining the data from the manufacturers datasheets, and considering the capacity characteristics constant at the operation voltage. In the case of the Si, the manufacturer already provides the gate charges for different operation voltages. For the SiC modules, the charges are obtained from the capacity characteristics plot for $V_{ds} = 100\ V$, and using the expressions (10) and (11) from [13], that again assume the interelectrode capacitances constant.

$$Q_{GS} = C_{iss}(V_{ds}) \cdot V_{Mill} \quad (10)$$

$$Q_{GD} = C_{rss}(V_{ds}) \cdot V_{Mill} \quad (11)$$

Analytical Loss Model Results. The analytical model presented before is used to calculate the losses and the efficiency of both configurations at the lowest input voltage, thus at the highest current, showing the results in Fig. 4. First, all the power range is tested at 20 kHz switching frequency, Fig. 4(a). At low power, the current in the converter is low, so high efficiency is achieved with the SiC configuration. The Si configuration is penalized by the body diode switching losses which are neglected in the SiC configuration. As the power thus the current is increased, the conduction losses become much more relevant. The better conduction resistance, $R_{DS(on)}$, of the SiC modules makes the difference in efficiency, improving it around 1.1 % when compared to the Si configuration at maximum power.

However, this first results already show the good switching performance of the Si configuration, taking advantage of the parallel devices, but mostly the individual driving of each device, minimizing the switching losses. The Si configuration achieves lower switching losses at high power, even if the quadratic relation to the current highly affects conduction losses, completely dominating the switching losses as the power is increased.

The good switching performance of the Si configuration is shown in Fig. 4(b), in where the losses of the two configurations are calculated for the full power, but at different switching frequencies. It is seen the switching losses at full power are very similar for both configurations, but the conduction losses are the ones making all the difference. In fact, it is desirable to keep the switching frequency as low as possible, to reduce the losses of the system. Selecting a switching frequency about 10 to 15 times higher than the fundamental frequency of the inverter should be enough for such HP motor drives. Once again, this analysis shows the dominance of the conduction losses over the switching losses in HP systems in space.

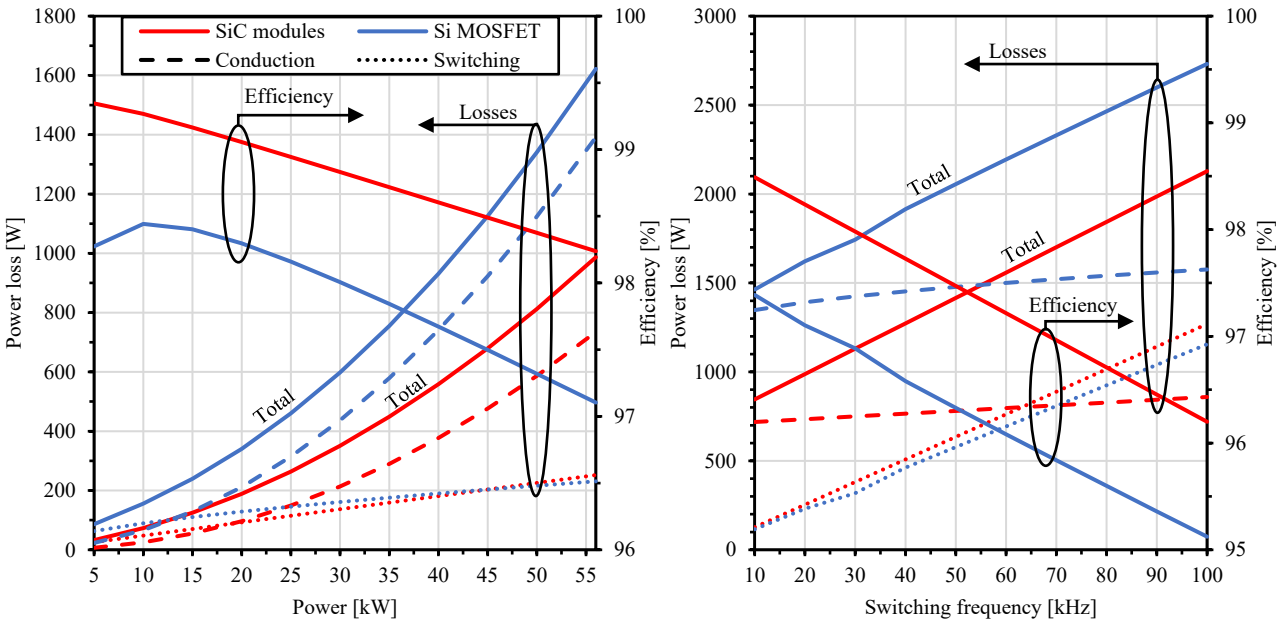


Fig. 4. Power loss distribution and efficiency of the motor drive with SiC modules and Si MOSFETs, for (a) different operation powers at 20 kHz switching frequency and (b) different switching frequencies at maximum power.

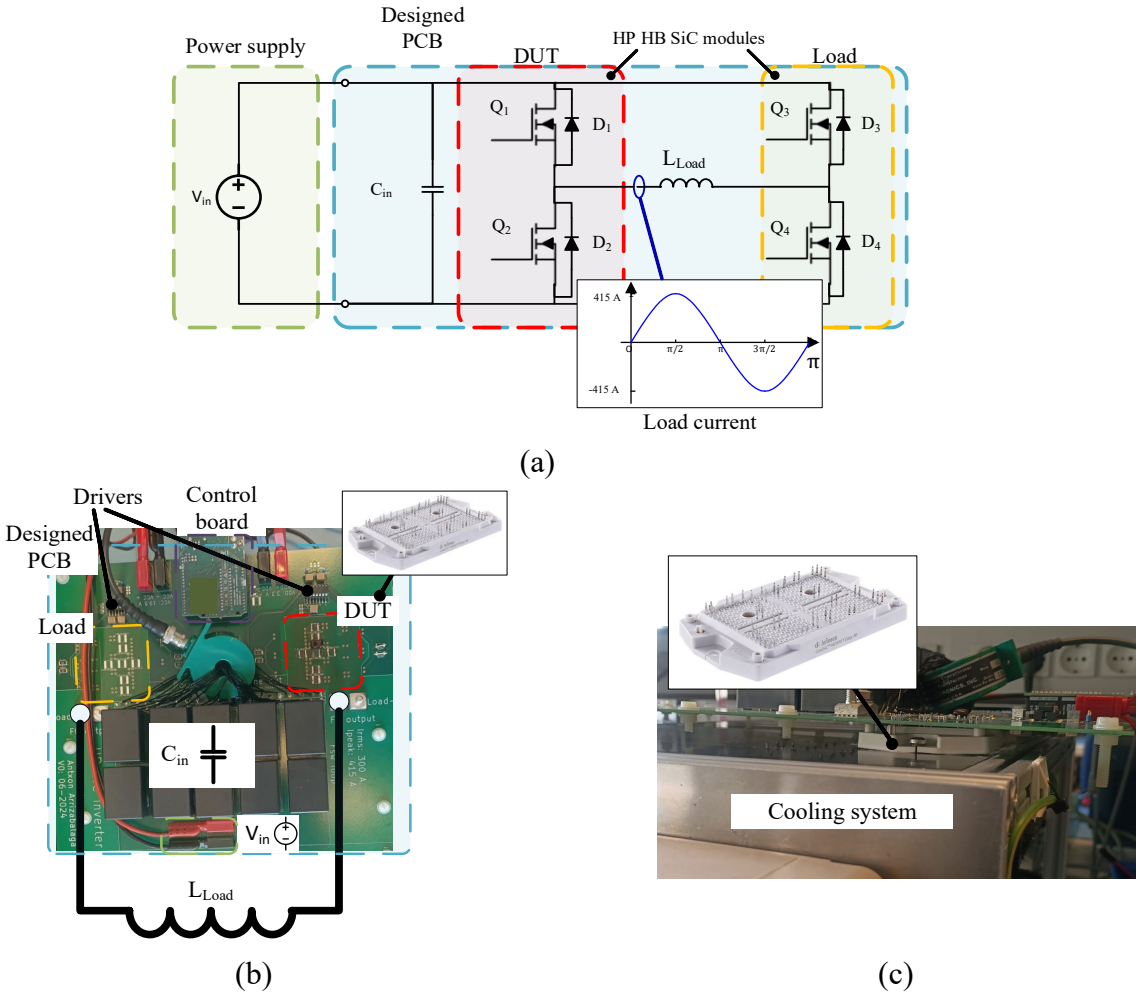


Fig. 5. Proof-of-concept prototype for the next steps in the project (a) conceptual diagram, (b) the PCB with the SiC HB modules underneath and (c) a close look to the SiC HB modules screwed to the cooling system with the PCB press-fitted on top.

Conclusion and Future Work

This work proposes 1200 V SiC HB modules to improve the HP motor drives in space. Using the high current capability of SiC HB modules the systems can be designed using a single module per phase, reducing the required PCB area 52 %. In addition, analytical loss calculations confirm the conduction losses are the most dominant form of losses in this type of application, so reducing these losses becomes key to improve the efficiency. The lower $R_{DS(on)}$ of the SiC modules, when compared to the space qualified Si MOSFETs allow to increase the efficiency of the system significantly.

Their specific design for HP, with the thermal conduction pad to directly screw the modules to the cooling system, as well as the high current capability make the SiC modules the perfect devices to overcome the challenges faced by Si devices in HP systems in space.

A proof-of-concept prototype has been designed and built, Fig. 5, combining the SiC HB modules and space qualified drivers. The next steps will focus on proving these modules can be driven with space qualified drivers, by testing the prototype, enabling the easy technological transition to the SiC for space industry. Overall, following the terrestrial trend to use HP SiC modules in HP systems seems logical also in space, even if the 1200 V voltage rating needs to be derated significantly.

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