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Latching Current Limiter for High-Power Distribution in Space Enabled by SiC N-MOSFET

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Abstract. High power and high voltage distributions will be required in space, but the necessary latching current limiters to manage the loads are not feasible with current Si P-MOSFET technology in the required power and voltage range. The generated losses and the number of parallel components make the system performance unacceptable. SiC N-MOSFETs are proposed as an alternative, due to their superior current ratings, reduced conduction resistance and increased thermal limits. Using these characteristics, two preliminary designs are proposed with SiC N-MOSFETs, one to optimize the power losses in the nominal operation and the other to reduce the required number of parallel devices and increase the allowable time under fault of the system. Both configurations overcome the challenges brought by the high power and high voltage distributions in space, reducing the losses and the complexity of the system while increasing the time under fault. This work shows how SiC technology can enable high power and high voltage distribution in space, while highlighting the importance of high power packages and thermal characteristics in certain applications.

Introduction

The demand for high-power (HP) electronic systems is growing in space, as the main space agencies are designing more ambitious space and lunar missions [1], [2]. All these HP payloads will require HP distribution, which will have to be high voltage (HV), preferably over 100 V. The latching current limiters (LCL) are used for managing the loads in space electrical distribution systems being the Si P-MOSFETs the preferred devices due to their easy control. However, space graded Si P-MOSFETs are limited in terms of conduction resistance and blocking voltage, generating unacceptable losses if used at HP [3].

In this contest, the use of SiC devices in space HP systems is being studied [4],[5],[6], [7]. However, and due to their susceptibility to single event burnouts (SEB) at high blocking voltage, their operation voltage is significantly derated forcing to use 1200 V SiC devices below 300 V in space environments [8], [9], [10]. Although the 1200 V voltage rating is highly popular in terrestrial applications and provides a wide variety of products with different characteristics, SiC P-MOSFETs are marginal, being the vast majority SiC N-MOSFETs.

The driving of N-channel MOSFETs for LCL was solved in [11], [12], and SiC N-MOSFETs have been proposed and demonstrated for a class 10 LCL [3], achieving improved performance when compared to Si P-MOSFETs. This work studies the possibility to further increase the power of the distribution line, up to 10 kW while following the operation defined for a class 10 LCL [13].

Study

Operation of the LCL. A 120 V distribution line is considered to supply the HP payloads. A constant 83 A current is distributed in the line during nominal operation, reaching 10 kWs. When a fault occurs in one of the loads, the load current in the line is increased to the limiting value following the regulation of class 10 LCLs, 140 % of the nominal current [13], defining the operation under fault in 116.2 A. The minimum current limiting time is 1.5 ms, so the LCL must operate limiting the fault current at least for that period.

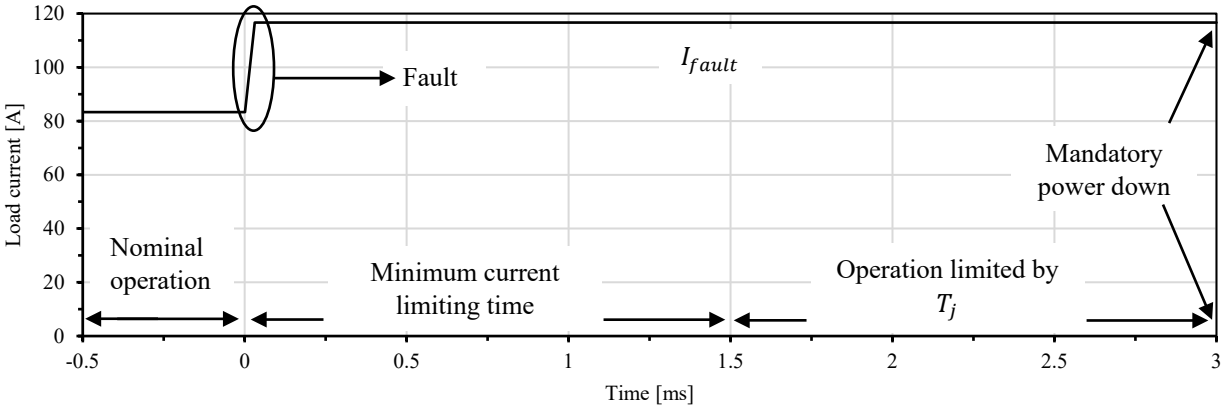


Fig. 1. Operation of the proposed HP LCL.

The junction temperature, T_j, of the device must remain below the maximum permitted value for each device, following the derating standards for electrical, electronic and electro-mechanical (EEE) components [14]. After this time, the power line can be powered down, or kept on until 3 ms, if the T_j limit is not reached, when the whole line needs to be powered down if the fault is not cleared. Fig. 1 shows the current profile in the distribution line under study, highlighting every operation point. The overload event with the current overshoot is not considered for this analysis.

To calculate the power losses in the analyzed configurations, as well as the T_j, the analytical equations proposed in are [15] used. The power losses under nominal operation are calculated with (1), being $R_{DS(on)}$ the conduction resistance and I_{nom} the nominal value of the distribution current under nominal operation, 83 A, times -0.5 ms to 0 ms in Fig. 1.

$$P_{nom} = R_{DS(on)} \cdot {I_{nom}}^2 \tag{1}$$

When the fault occurs, times 0 ms to 1.5 ms in Fig. 1, the power device works in linear mode, blocking the full line voltage, $V_{bus} = 120\ V$ and conducting the limiting current, $I_{fault} = 116.2\ A$. The power loss in the device is expressed as (2).

$$P_{fault} = V_{bus} \cdot I_{fault} \tag{2}$$

For the thermal modeling, a Cauer network is used, considering an ideal heat-sink for every configuration. Datasheet values are used to model the transient temperature evolution populating the Cauer model, using the transient thermal impedance graphs provided by the manufacturers. The junction temperature is calculated using (3), where $T_{j(nom)}$ represents the steady state temperature of the junction during nominal operation, and $T_{j(rise)}$ the temperature increment in the device during the operation under fault.

$$T_j(t) = T_{j(nom)} + T_{j(rise)}(t) \tag{3}$$

The junction temperature in the nominal operation is calculated using the power losses in nominal operation P_{nom}, and the junction to case thermal resistance R_{Th} in (4).

$$T_{nom} = T_0 + P_{nom} \cdot R_{Th} \tag{4}$$

Then the temperature rise during time is calculated during the fault operation with (5), modeling it like a RC network and considering the C_{Th} thermal capacitance obtained from the transient thermal impedance graphs provided by the manufacturers.

$$T_{rise}(t) = P_{fault} \cdot R_{Th}(1 - e^{\frac{t}{(R_{Th} \cdot C_{Th})}}) \tag{5}$$

Device Selection. A Si P-MOSFET and two SiC N-MOSFETs are selected for the study, Table 1. Due to the low HV availability of the Si P-MOSFETs, the selected device has low current capability, and high $R_{DS(on)}$. This leads to high losses in nominal operation, as well as a high required component count in parallel. High current SiC devices are selected, with the objective of only using a single device in the HP LCL.

Table 1. Main technical characteristics of the selected devices.

Parameter	IRFP9240	AIMBG120R010M1	SCT020H120G3AG
Technology	Si P-MOSFET	SiC N-MOSFET	SiC N-MOSFET
Name	Si	SiC 1	SiC 2
V_{ds} $[V]$	200	1200	1200
I_d $(T_j = 100\,°C)$ $[A]$	7.5	150	128
$R_{DS(on)}$ [mΩ]	500	8.7	9.3
$T_{j(\max)}[°C]$	150	175	200
$R_{Th(J-C)}[°C/W]$	0.83	0.13	0.2
$C_{Th(J-C)}[J/W]$	0.018	0.019	0.075

15.7 x 20.55 mm

(a)

10 x 15 mm

(b)

18.8 x 43.7 mm

(c)

Fig. 2. Packages of the selected devices with their dimensions, (a) Si, (b) SiC 1 and (c) SiC 2.

Two different packages are compared, but also considering the T_j maximum limit of each device. [14] states 110 °C is the maximum junction temperature for EEE components, or $T_{j(\max)} - 40$ °C, whichever is more restrictive. However, an exception is made in devices with $T_{j(\max)} \geq 150$ °C. In such cases the $T_{j(\max)} - 40$ criteria should prevail. Exploring the high $T_{j(\max)}$ capability of SiC MOSFETs, a SiC device with small SMD package and good $R_{DS(on)}$ is selected, while the other SiC device is a SiC MOSFET with a HP package and extended $T_{j(\max)} = 200$ °C temperature range. Having a HP package increases the footprint area, but slows down the thermal dynamic due to the increased C_{Th}. Table 1 shows the main device characteristics, while Fig. 2 shows the packaging of each device as well as their dimensions.

Results

Nominal Operation. 16 parallel Si devices are required to operate the HP distribution line due to the current rating and the current during the fault operation. Dividing the nominal operation current between the 16 devices, and applying (1), the power losses in the nominal operation point are calculated to be 215 W. A single SiC device is required considering their current rating for both devices. Doing the same calculation, the LCL with SiC 1 consumes 60 W while the LCL with SiC 2 consumes 64 W in normal operation.

However, the three configurations consume and must dissipate the same amount of power during a fault, 13944 W, calculated with (2). This power is independent from the device, being the junction temperature the limiting factor during a fault, as shown in Fig. 1.

Thermal Simulation. Equation (3) is used to calculate the T_j evolution during a fault for the three configurations. Even if the $T_{j(\max)} \geq 110\,°C$ limit is extended to $T_{j(\max)} \geq 135\,°C$ and to $T_{j(\max)} \geq 160\,°C$ for SiC 1 and SiC 2 devices respectively using the exception in [14], both SiC devices cannot withstand the thermals stress of a fault during 1.5 ms with a single device. On the contrary, the 16 paralleled Si devices do not require any further change due to the thermal stress.

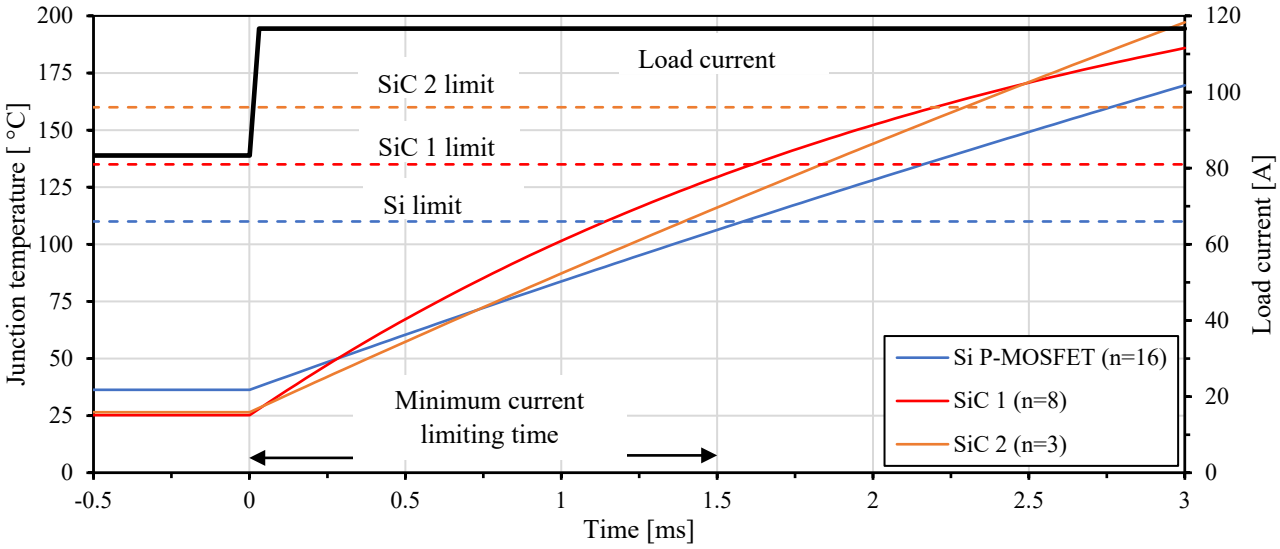


Fig. 3. Junction temperature evolution of the analyzed devices during a fault event.

Simulation shows 8 parallel devices are required for SiC 1, while 2 parallel devices are just not enough for SiC 2, requiring 3. Fig. 3 shows the calculated T_j evolution during a fault for the three configurations, together with the thermal limits. These results show a clear dependency on the thermal capacitance during the fault operation, rather than on the thermal resistance.

Using (5) at the end of the minimum current limiting time, $t = 1.5\,ms$, for different R_{Th} and C_{Th} couples, simulating the different characteristics of devices and packages, and normalizing the temperature increase T_{rise}, Fig. 4 can be obtained. The plot shows how the temperature increase barely changes even if the thermal resistance is increased, when the thermal capacitance is high. On the contrary, at low C_{Th}, even a small increase in the R_{Th} causes a big change in the increased temperature. This is what forces SiC 1 to parallel up to 8 devices even with a better R_{Th} than SiC 2. The effect of the C_{Th} can be clearly seen, damping the thermal response when exposed to short but high power dissipation periods. So, it is concluded the use of the HP packages with high thermal capacitance is key for their use in LCLs, or in the applications with high transients in the load current thus in the thermal stress, helping to reduce the temperature increase in the junction during the short high power dissipation periods.

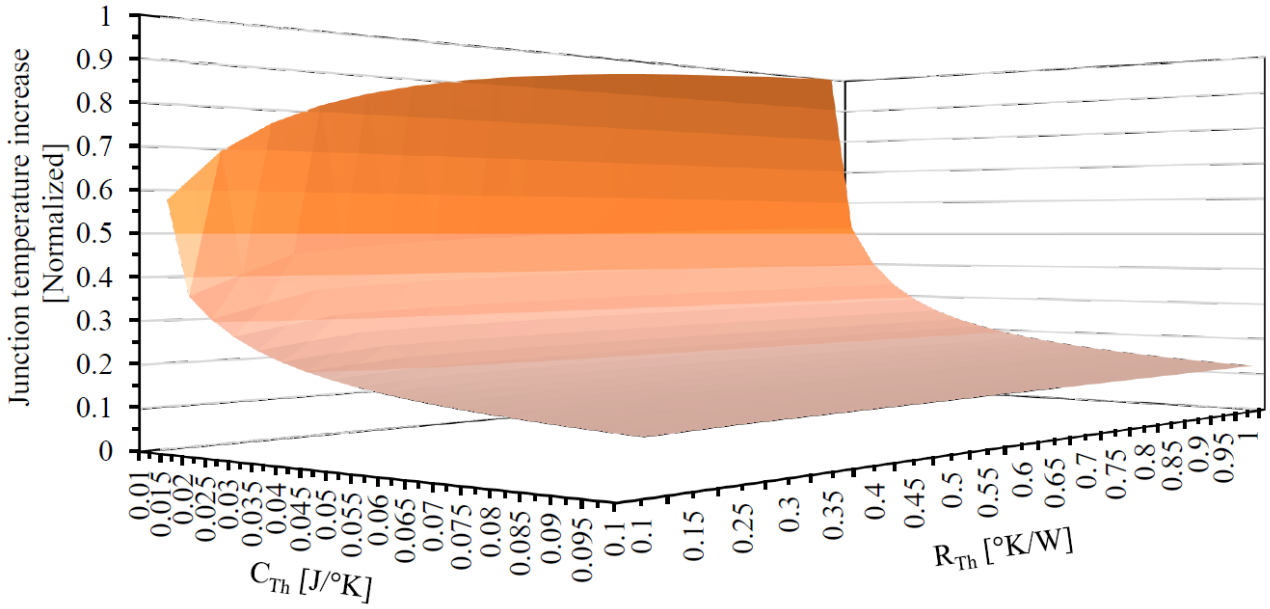
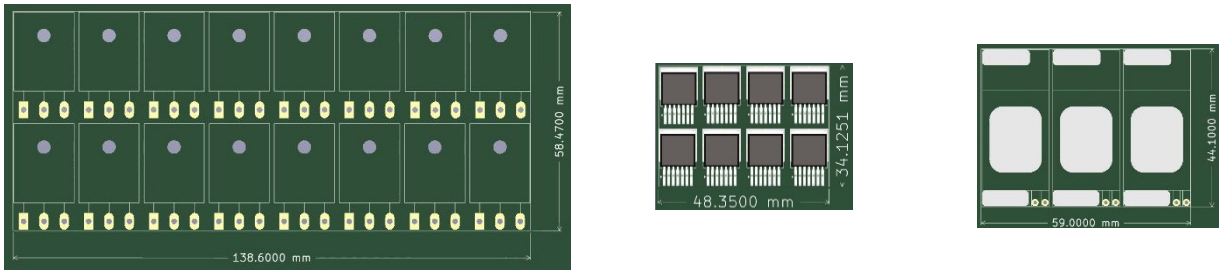


Fig. 4. Normalized junction temperature after limiting the current 1.5 ms for different R_{Th} and C_{Th}.

Final Configuration. As seen in Fig. 3, the thermal limits of the application force the parallelization of several devices. This affects both the required PCB area for each configuration, as well as the nominal operation losses. The dimensions of each device are shown in Fig. 2, but the required area of the PCB for each configuration is shown in Fig. 5, considering just the power stage. The control stage must be added to this area, but it is not discussed in this work. Table 2 summarizes all the relevant results of the three configurations.

The configuration with the Si devices requires 81 cm^3, while the configuration with SiC 1 only requires 16.5 cm^3, even considering the 8 parallel devices. That is an 80 % reduction in the required area. The configuration with SiC 1 uses half of the devices required by the Si configuration, and reduces the power losses in the nominal operation point from 215 W to just 7.5 W. The time before hitting the thermal limit under a fault is the same for both configurations, 1.6 ms, see Fig. 3. These results show a substantial improvement in the performance of the HP LCL by selecting SiC technology, mostly in terms of nominal operation performance, enabling the LCL based HP distribution systems with acceptable losses.

However, if the objective is to reduce the number of required parallel devices for the LCL, and maximize the time under fault the system can withstand, a HP package must be selected due to the higher C_{Th}, as seen in Fig. 4. To achieve these objectives, the configuration with SiC 2 is preferred, only requiring 3 parallel devices and being able to withstand a fault for over 2.3 ms, increasing the time under fault 0.7 ms when compared to the previous configurations. This is due to its extended $T_{j(\max)}$, but even if the thermal limit of SiC 1 was to be respected, the maximum time under fault for SiC 2 would be 1.83 ms, still 0.23 ms more. This again shows the benefits of using HP high C_{Th} packages. The power losses under nominal operation are 21.35 W, still significantly lower than the configuration with Si, but higher than the losses with SiC 1 due to the reduced number of parallel devices. The required area is 26 cm^3, 68 % less than for the Si, but higher than for the configuration with SiC 1.



(a) (b) (c)

Fig. 5. Minimum PCB area required for the power stage of the whole LCL with (a) Si P-MOSFET, (b) SiC 1 and (c) SiC 2, with a 6 to 10 scale.

Table 2. Final configuration relevant results.

Parameter	Si	SiC 1	SiC 2
Required parallel devices	16	8	3
Required PCB area [cm^2]	81	16.5	26
Nominal operation power losses [W]	215	7.5	21.35
Maximum time under fault [ms]	1.6	1.6	2.3

Conclusion

LCLs are not feasible in HP and HV distributions in space, in the range of tens of KWs, if Si P-MOSFET technology is used, because the losses are too high, the number of required parallel devices takes too much area and complicates the design. However, this paper shows a HP LCL for space is feasible if SiC N-MOSFET technology is used due to the higher current rating, the highly improved $R_{DS(on)}$ and the extended $T_{j(\max)}$.

If the power losses in the nominal operation are to be reduced, the SiC N-MOSFET with the lowest $R_{DS(on)}$ should be selected, and use parallel devices to distribute the losses until the thermal limit is met. The paralleling strategy will further reduce the power losses in the nominal operation. However, if the number of parallel devices is to be minimized, and the time under fault maximized, this study shows the C_{Th} of the package should be considered. Using HP packages with high C_{Th} slow down the thermal dynamics of the LCL, allowing to reduce the required parallel devices thus simplifying the design and increasing the time under fault. SiC technology will enable LCLs for the HP and HV distributions in space, providing designers with several optimized solutions depending on the objectives of the missions.

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